Zero Quiescent Current Startup Circuit with Automatic Turning-off for Low Power Current and Voltage Reference

Andre Mansano
Freescale Semiconductor
Rod. Anhanguera, km 104
Rua J. Clerk Maxwell, 400
Campinas - SP
+55 (19) 3783-8581
b12040@freescale.com

Andre Vilas Boas
Freescale Semiconductor
Rod. Anhanguera, km 104
Rua J. Clerk Maxwell, 400
Campinas - SP
+55 (19) 3783-8522
rab003@freescale.com

Alfredo Olmos
Freescale Semiconductor
6501 William Cannon Dr.
Austin, Texas 78735, USA
+1 (512) 895 1957
rao007@freescale.com

Jefferson Soldera
Laboratório de Sistemas
Integráveis Tecnológico
Rua Paes Leme, 524
São Paulo – SP
+55 (11) 3521-0801
jefferson.soldera@lsitec.org.br

ABSTRACT

A zero quiescent current startup circuit with automatic turning-off for low power current and voltage reference is presented. The proposed startup uses positive feedback to sense an internal bias voltage of the main current/voltage reference circuit and guarantees it properly achieves its desired steady state condition. After that, the start-up circuitry automatically turns off itself. Hence, there is no power consumption on start-up circuitry after start-up process. Also, its very robust architecture is compatible with standard CMOS processes and is able to operate down to sub-1V making it ideal for single battery applications. The circuit has been integrated in a 45nA current source implemented in TSMC 0.25um process. Transient response of the start-up circuitry has been measured as well as supply voltage variation has been evaluated to prove start-up operation.

Categories and Subject Descriptors

B.7.0 [**General**]: Integrated Circuits - microprocessors and microcomputers, VLSI, simulation.

General Terms

Design and Experimentation.

Keywords

Start-up, power-up, starter, initialization, current reference.

1. INTRODUCTION

Current and voltage reference with positive feedback (i.e., self-biased reference) need a start-up circuit to provide an initial condition that drives the circuit to a proper steady state value avoiding it to go to an unwanted operation point (usually, all internal currents equal to zero). Leakage currents help to take those kinds of circuits to the desirable operational point. However, at cold temperatures the start-up process becomes harder and most of the time it does not start due to very low leakage on the P-N junctions.

SBCCI'09, August 31st - September 3rd, 2009, Natal, RN, Brazil.

Several types of start-up circuits exist but most of them do not stop current consumption [1-4] after start-up phase, nor work at a sub-1V power supply voltage [5], neither have a robust architecture to support fab-to-fab transference and low part-to-part variation. There are several technical articles that show just simulation results without experimental data. In [6] it is shown a start-up circuit that has uW power consumption avoiding using it for low power circuits whereas [7] brings a circuit that strongly depends on a capacitor and on start-up pulse width provided by enable signals.

Nowadays, due to very low power constraints, reference circuits must be much more power efficient to significantly increase battery life-time. Additionally, when designing current references in the range of nA, the period of time required for charging the internal nodes may become extremely long, making the circuit enable process not enough to start-up the self-biased circuit in time. The start-up circuit architecture proposed here is suitable for low power current and voltage reference. It combines low voltage operation, power efficiency, robustness, fast start-up time, and simplicity.

The present paper is organized as follows. In Section 2 the circuit topology is presented. Once the principle of operation is discussed, silicon results are shown in Section 3. Finally, in Section 4 some conclusions are drawn from this work.

2. CIRCUIT TOPOLOGY

The proposed start-up architecture is presented in the Fig.1 and its timing diagram is shown in the Fig. 2. The main advantage of this topology is the use of a feedback signal to turn off all start-up circuitry power consumption after start-up process and ensure that the main circuit [8] has attained its steady state DC condition at the end of this process.

Before initializing the start-up process through of a power down signal (**en**/**enb**), the **en** signal (enable) is low and the **enb** signal (negated enable) is high. Thus **a** node on start-up circuit is pulled up and the stray cap **Ca** (representing all capacitances for that node) is pre-charged with power supply value. As a result, **b** node is kept down and M6 capacitances are pre-charged likely **Ca**. There is no power consumption and start-up circuit is preset in waiting mode (t0).

The start-up process is initialized when power down signals state is changed, **en** goes high and **enb** goes down (t1). M1 is cut off, M2 still remains off and **a** node is maintained high by stray cap **Ca**. M1 and M2 perform a dynamic inverter and **a** node stays high as long as **nbias** is down. Therefore, **b** node is kept down and **c** node goes high through M5 and M6 pulling down devices Mst1 and Mst2 forcing **pbias1**/**pbias2** biasing nodes to ground.

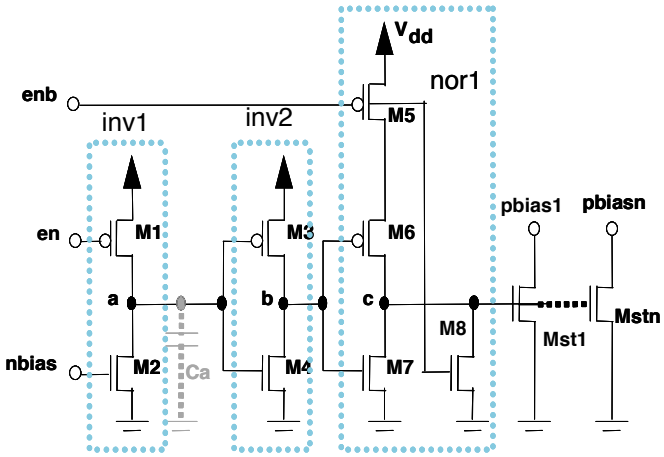

Figure 1. Start-up circuit stand alone.

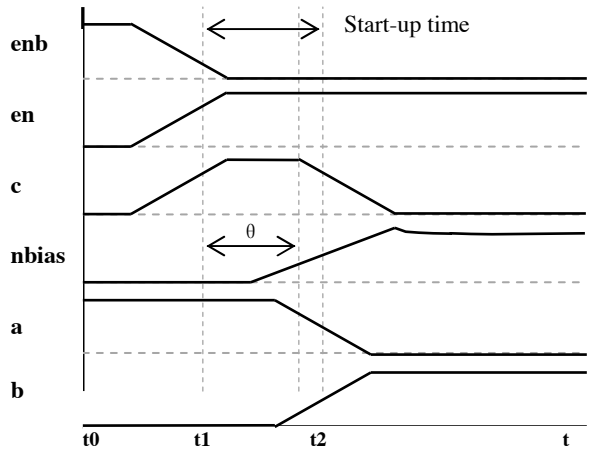

Figure 2. Start-up timing diagram.

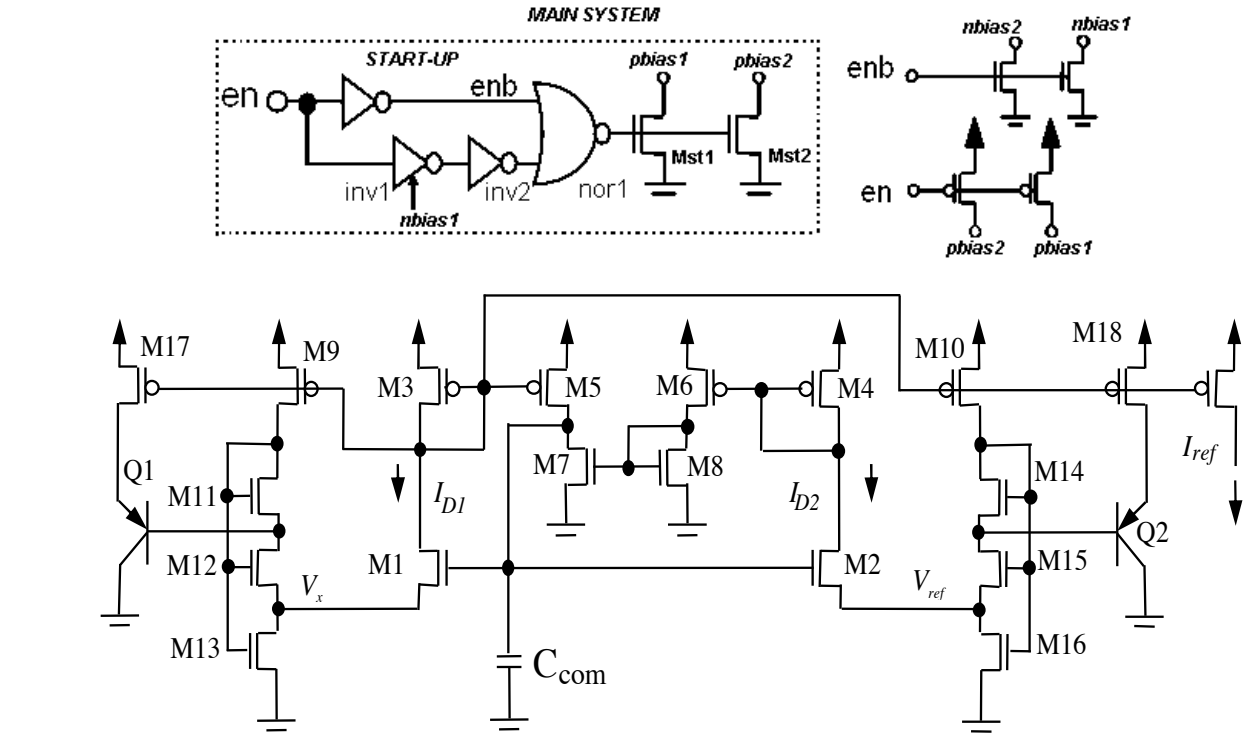

Figure 3. Start-up circuit connected to a resistor-less low power current source [8].

Fig. 3 illustrates the main resistor-less current reference [8]. Note this resistor-less current reference is merely an example of application for the proposed start-up topology. Also note the resistor-less current reference in Fig. 3 has **pbias1~pbias2** signals as well as **nbias** signal needed to sense if main circuit reaches the desirable steady state condition. For the circuit in Fig. 3, the start-up current is mirrored to the **nbias** node and it drives the current source to desired steady state operating point. As soon as **nbias** voltage goes up (t_2), inv1 output goes to ground, so Ca is discharged through M2 forcing **b** node to V_{dd} that makes M7 on, and both M6 and Mst1/Mst2 off.

For suitable operation some few design advices are necessary for a good circuit behavior and performance. The impedance seen through the drain of M2 (in Fig. 1) must be high enough to guarantee that the positive feedback signal (**nbias**) reaches the desirable DC value before turning off the start-up circuit.

This device can increase or decrease the time which Mst1 is on. Signals **en** and **enb** need to be generated with small delay from each other (in the order of ns). Besides, to avoid significant current leakage the start-up transistors channel length must be not minimal, especially for Mst1~Mstn.

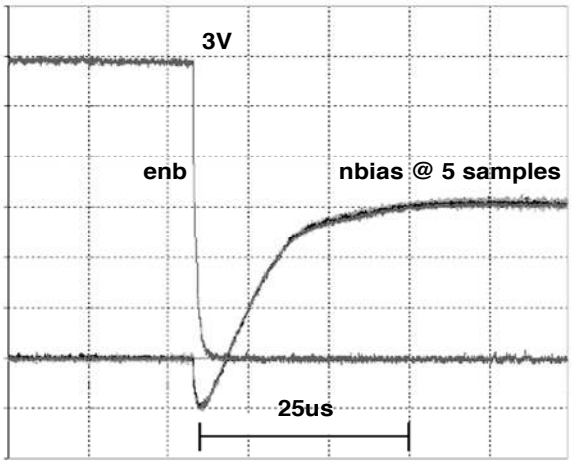

Figure 4. nbias signal during start-up time.

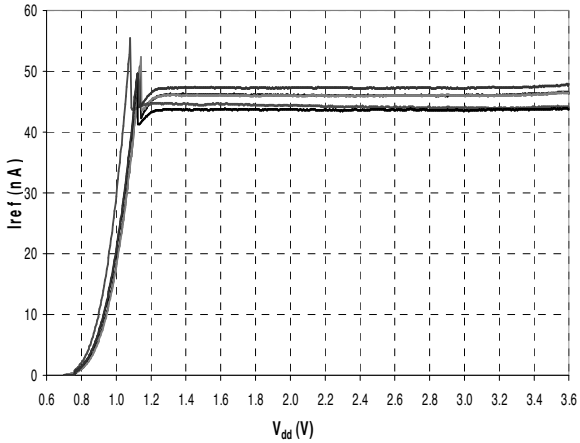

Figure 5. Main system behavior vs power supply

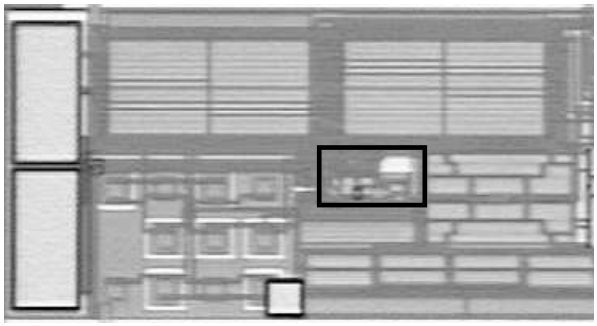

Figure 6. Die photograph of current source including startup circuit.

3. EXPERIMENTAL RESULTS

In this section, the proof of concept is presented. Silicon data is available to demonstrate circuit workability regarding power supply voltage and transient response. Fig. 4 exhibits **nbias** signal behavior when **enb** signal becomes low. The NMOS bias signal starts growing until it achieves its DC operating point. Fig. 4 demonstrates that start-up circuit properly works to make main reference circuit converge to the designed value.

After reaching its DC steady state condition, the dynamic inverter **inv1** pulls down "a" node (see Fig. 1) through M2 transistor controlled by **nbias** signal. "a" node pulling down characterizes the start-up current cut-off. The start-up time shown in Fig. 4 is increased due to probing parasitic capacitance introduced during the measurements, so the figure does not show the real startup time of the circuit.

Fig. 5 depicts the main system (Fig. 3 from [8]) behavior over power supply voltage sweep.

The start-up circuit enables the current source at 3.6V driving the main circuit to the designed operating point. After start-up process finishing, the power supply voltage is swept down and startup circuit does not disturb the main system that properly works until power supply achieves 1.1V. The minimum supply voltage of main reference current is 1.1V, hence below 1.1V current reference is out of nominal value (45nA).

4. CONCLUSIONS

A zero quiescent current start-up circuit for reference circuits has been presented. The circuit is simple to design and is compatible with standard CMOS processes. It senses when main reference operating point is achieved monitoring an internal bias voltage and automatically turns off start-up current consumption. It starts the reference circuit even at cold temperature and does not interfere on reference operating point even at hot temperatures. Also, as shown in experimental results, the part-to-part deviation is very small as expected, due to very simple circuit implementation with logic gates and switches, demonstrating circuit robustness. The circuit is suitable for low current self-biasing references operating in low voltage and large temperature range condition where power-down states are necessary.

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