1.0 µm Process Family:

XDH10

Modular 1.0µm 650V Trench Insulated BCD Process

MIXED-SIGNAL FOUNDRY EXPERTS

DESCRIPTION

XDH10 is X-Fab´s dielectric trench insulated smart power technology. Main target applications are analog switch ICs, driver ICs for capacitive, inductive and resistive loads and EL / piezo driver ICs for applications using 220V net supply. The typical breakdown voltage of the HV DMOS devices is >350V or >650V. The modular process combines DMOS, bipolar and CMOS processing steps that are compatible with dielectric insulation to provide a wide variety of MOS and bipolar devices with different voltage levels within a dielectric bi-directional high voltage trench insulation on the same die. The 14 layers core process module is available for 650V breakdown voltage of the HV DMOS. This process module provides trench insulation, single level poly with thick gate oxide, a third level metal with power metal. With this core module an optimised self-aligned poly-gate n-channel quasi-vertical DMOS transistor and some bipolar transistors can be made, other process modules can be added to integrate CMOS transistors, high voltage PMOS transistors, further bipolar elements and a third poly for poly-poly capacitors and high value resistors.

KEY FEATURES OVERVIEW

Trench (dielectric) insulated thick 6 inch SOI wafers are the base for the XD10 process. With the dielectric insulation the necessary area needed for 650V insulation is significantly smaller then with junction insulation (especially for high voltage applications) leading to smaller chip sizes. Use of dielectric insulation insures a bi-directional insulation between adjacent components. The quasi vertical DMOS transistor is the basic HV component of the XD10 technology. The device structure and process parameters are optimized to obtain a drain breakdown voltage of >350V and >650V respectively and maximum drain saturation current with a low on-resistance. The electrical characteristics depend on channel width and length, drift-layer length, drift-layer doping and extended source field-plate effect. The DMOS device is fabricated with a double-diffused process with a deep p-tub to prevent secondary breakdown.
A wide variety of different voltage levels is possible on the same die.

A high number of different devices are available:

- High and medium voltage n-channel DMOS
- Medium voltage PMOS
- CMOS transistors with different voltage levels
- NPN and PNP transistors with different voltages
- DEPLTRA module (N channel CMOS depletion transistors), PODCAP module (Poly on diffusion resistor)
- Scaleable DMOS & PMOS transistors with different numbers of centrepiece
- NEW: **IGBT transistors**
- NEW: **HV depletion DMOS transistors**
- NEW: **Handle wafer contact resistor**
- OTP option: Zener Zap
- High voltage and zener diodes
- Gate oxide and high voltage capacitors
- Poly resistors with different sheet resistivity
- Triple level metal, third metal 2.3µm
- Optional third poly for high value resistor or poly-poly capacitor
- Doped oxide / polyimide passivation
- 1µm design rules enable the integration of complex CMOS logic

APPLICATIONS

- Driver ICs for capacitive
- Inductive and resistive loads
- Analog switch ICs
- Driver ICs for EL and piezo elements
- High voltage DMOS arrays
- Half and full bridges with driver and logic
- High input voltage linear regulators

QUALITY ASSURANCE

X-FAB spends a lot of effort to improve the product quality and reliability and to provide competent support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by strict quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, QS 9000, VDA 6, ISO TS 16949 and other standards.

DELIVERABLES

- PCM tested wafers
- Optional engineering services: Multi Project Wafer (MPW) and Multi Layer Mask Service (MLM)
- Optional design services: feasibility studies, Place & Route, synthesis, custom block development

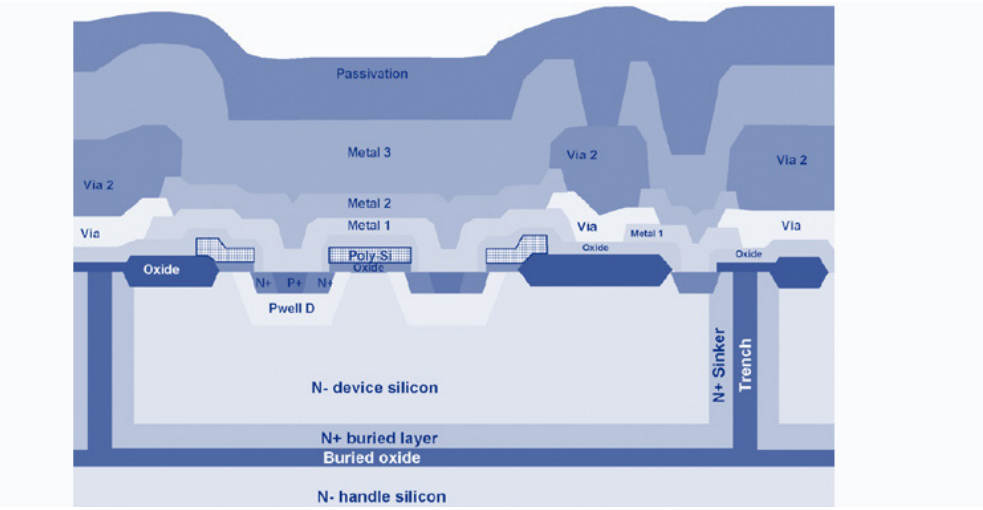
PRIMITIVE DEVICES

- Pre-defined 650V and 350V n-channel DMOStransistors with different on-resistances
- Scaleable 5V, 7V and 20V CMOS transistors
- Pre-defined medium voltage PMOS for different voltages
- Pre-defined bipolar transistors for different voltages up to 80V
- Poly silicon resistors (low TC and high value resistor)
- Implanted resistors
- Poly-Poly and gate oxide capacitor
- 650V sandwich capacitor
- Zener diode and protection diodes for different voltages

XDH10 BASIC DESIGN RULES

Mask	width [µm]	Spacing [µm]
TRENCH	= 4.0	10.0
DIFFD	4.0	3.0
POLYD	1.0	1.2
DIFF	0.8	2.0
POLY1	1.0	1.2
CAPRES	2.0	2.4
CONT	1.2	1.0
MET1	1.1	1.5
VIA	1.7	1.6
MET2	1.4	1.7
VIA2	4.0	4.0
MET3	3.0	3.0

XDH10 CORE CROSS SECTION



XDH10 PROCESS FLOW

SITIRS / MUTRIS Module	Additional Modules	
Thick SOI Wafer		
Trench		
	Handle wafer contact	HWCNT
Trench Cover		
DMOS Active Area		
	ND Implant	HVDDMOS
DMOS Polysilicon		
DMOS Pwell		
	n-well	CMOS
	p-well	
	CMOS active area	
	B Implant	
	ND Implant	DEPLTRA
	P Implant	PODCAP
	CMOS polysilicon 1	CMOS
	CMOS polysilicon 2	CAPRES
	B Implant	IGBT
N+ implant		
P+ Implant		
Contact		
Metal 1		
Via		
Metal 2		
Via 2		
Metal 3		
Pads		
PCM test		
Back side grinding (on customer request)		
Final control		mask steps

XDH10 CORE MODULE

Module Name	Descriptions	Masks No.
SITRIS	DIMOS module up to 650V, single trench	14
MUTRIS	DIMOS module up to 650V, multiple trenches	14

XDH10 ADDITIONAL MODULES

Module Name	Descriptions	Masks No.
CMOS	CMOS module	5
CAPRES	Capacitor / resistor module	1
DEPLTRA	Depletion transistor module	1
PODCAP	Polysilicon on diffusion capacitor module	1
HVDDMOS	High voltage depletion module	1
HWCNT	Handle wafer contact module	1
IGBT	IGBT devices module	1

XDH10 RESTRICTIONS FOR MODULE COMBINATIONS

Module name	Use of the module also requires use of the following module(s)	Use of the module is not available with the use of the following module(s)
SITRIS		MUTRIS
MUTRIS		SITIRS
CAPRES	CMOS	
DEPLTRA	CMOS	
PODCAP	CMOS	
HVDDMOS	SITRIS	
IGBT	CMOS+SITRIS	

Active Devices

XDH10 MOS CORE TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	BVDS [V]	Max. |VDS| [V]	Max VGS [V]
5V NMOS	ne	CMOS	0.80	150	16	5.5	15
7V NMOS	nea	CMOS	0.80	150	16	7.0	15
5V PMOS	pe	CMOS	0.95	65	16	5.5	15
7V PMOS	pea	CMOS	0.95	65	16	7.0	15

XDH10 MEDIUM VOLTAGE TRANSISTORS

Device	Name	Available with module	|VT| [V]	BVDS [V]	RON [kΩ.µm]	Max. |VDS| [V]	Max VGS [V]
20V NMOS	nme	CMOS	0.8	50	19	20	18
20V PMOS	pme	CMOS	0.75	45	60	20	15
15V NMOS	nmea	CMOS	0.78	28	15	15	18
20V PMOS	pmea	CMOS	0.62	50	45	20	18
32V NMOS	nmeb	CMOS	0.8	60	21	32	15

Active Devices *(Continued)*

XDH10 HV CMOS TRANSISTORS

Device	Name	Available with module	|VT| [V]	BVDS [V]	RON [Ω]	Max. |VDS| [V]	Max. VGS [V]
300V PMOS	pha	CMOS	0.85	330	5300	250	15
350V PMOS	phb, phds*	CMOS	0.85	375	6200	300	15
600V PMOS	phfs*	CMOS+SITRIS	0.85	680	3500	560	15

* The phds are scalable devices, where the number of centrepieces can be varied. Please refer to process specification documents for details.
* The value shown here are for phfs with 32 centrepieces

XDH10 DMOS TRANSISTORS

Device	Name	Available with module	|VT| [V]	RON [Ω]	BVDS [V]	Max. |VDS| [V]	Max. VGS [V]	Max ID [mA]
650V DMOS, 700Ω	nd65a, nd65a1	MUTRIS, SITRIS	1.65	800	>680	625	20	20
650V DMOS, 180Ω	nd65b	MUTRIS	1.20	190	>680	625	20	120
650V DMOS, 130Ω	nd65c, nd65c1	MUTRIS, SITRIS	1.5	140	>680	625	20	120
650V DMOS, 75Ω	nd65d	MUTRIS	1.1	75	>680	625	20	120
650V DMOS, scalable	nd65es, nd65es1*	MUTRIS, SITRIS	-	-	-	625	20	-
350V DMOS, 3.5kΩ	nd35a, nd35a1	MUTRIS, SITRIS	1.65	4500	>400	300	20	2.8
350V DMOS, 1.1kΩ	nd35b	MUTRIS	1.6	1200	>400	300	20	7.5
350V DMOS, 270Ω	nd35c	MUTRIS	1.5	300	>400	300	20	70
350V DMOS, scalable	nd35ds, nd35ds1*	MUTRIS, SITRIS	-	-	-	300	20	-
650V DMOS	nd65g	SITRIS	1.7	750	> 680	625	20	31.5
650V DMOS, scalable	nd65fs*	SITRIS	1.0	65	> 680	625	20	150
650V DMOS, scalable, wide metal connection	nd65fsw*	SITRIS	-	-	-	625	20	425
540V DMOS	nd54a	SITRIS	1.85	1800	> 600	500	20	31.5
540V DMOS, scalable	nd54bs*	SITRIS	1.0	57	> 580	500	20	150
540V DMOS, scalable, wide metal connection	nd54bsw*	SITRIS	-	-	-	500	20	275
330V DMOS scalable	nd33as	SITRIS	1.75	520	> 390	300	20	-

* The nd65es,nd65es1, nd35da, nd35ds1 are scalable devices, where the number of centrepieces can be varied. Please refer to process specification documents for details.
* The values shown here are for nd65fs with 12 centrepieces, nd54bs with 20 centrepieces & nd33as with 32 centrepieces respectively.
* The parameter values of nd65fsw, nd54bsw with x centerpieces is equivalent to the nd65fs, nd54bs with x+4 centerpieces respectively. These devices features a wider source metal connection in order to allow for a higher drain current operating condition.

XDH10 DEPLETION TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	|BVDS| [V]	Max. |VDS| [V]	Max. VGS [V]	Max ID [mA]
N-Depletion NMOS	ndep	DEPLTRA	1.1	100	16	7.0	5.5	-
600V depl DMOS, scalable	ndd60as*	HVDDMOS	1.5		> 680	570	20	150
500V depl DMOS, scalable	ndd50as*	HVDDMOS	1.5		550	470	20	150

* with 5 centrepieces

Active Devices *(Continued)*

XDH10 IGBT TRANSISTORS

Device	Name	Available with module	|VT| [V]	BVCE [V]	ICE leak [nA]	Max. VCE [V]	Max. VGE [V]	Max IC [mA]
600V IGBT	ni65a	IGBT	1.7	> 700	< 0.5	600	20	220
600V IGBT	ni65b	IGBT	1.7	> 700	0.25	600	20	220

XDH10 BIPOLAR TRANSISTORS

Device	Name	Available with module	BETA	VA [V]	BVCEO [V]	VBE [mV]	max. VCE [V]
80V vertical NPN	qna	SITRIS, MUTRIS	70	1200	> 120	690	80
20V lateral PNP	qpc	SITRIS, MUTRIS	1600	19	> 26	580	20
50V high gain vertival NPN	qnb	CMOS	1000	110	> 50	625	50
80V lateral PNP	qpd	CMOS	210	45	> 100	525	80
5.5V vertical NPN	qnvc	CMOS	800	70	> 20	585	5.5
600V vertical	qnvd	SITRIS	75	-	-	625	600

Passive Devices

XDH10 DIFFUSION RESISTORS

Device	Name	Available with module	RS[Ω/□]	Temp. Coeff. [10^{-3}/K]	Max VTB [V]
PWELL	rpwd	SITRIS, MUTRIS	1500	6.0	50
N+	rdiffn	CMOS	26	1.6	8
P+	rdiffp	CMOS	120	0.9	13
PWELL	rpw	CMOS	3300	6.1	25

XDH10 HIGH RESISTIVE RESISTORS

Name	Device	Available with module	RS[Ω/□]	Temp. Co-eff. [10^{-3}/K]	Max VTB [V]
POLYD, P+ impl.	rpd, rpd_3*	SITRIS, MUTRIS	190	0.4	650
POLY1, N+ impl.	rp1, rp1_3*	SITRIS, MUTRIS	22.5	1.2	50
High resistive POLY2	rp2hr, rp2hr_3*	CAPRES	10000	-4.4	50
HV high resistive POLY2	rp2hrhv, rp2hrhv_3*	CAPRES	10000	-4.4	320

* Improved decription of bulk voltage dependency

XDH10 LOW TC RESISTORS

Name	Device	Available with module	RS[Ω/□]	Temp. Coeff. [10^{-3}/K]	Max VTB [V]
Low TC POLY2	rp2ltc rp2ltc_3*	CAPRES	335	-0.23	50

* Improved decription of bulk voltage dependency model

Passive Devices *(Continued)*

XDH10 METAL RESISTORS

Device	Name	Available with module	RS [Ω/ □]	Thickness [µm]	Max J/W [mA/µm]	Temp. Co-eff. [10^{-3}/K]	Max VTB [V]
Metal 1	rm1	SITRIS, MUTRIS	0.047	0.7	0.8	3.7	100/350/650*
Metal 2	rm2	SITRIS, MUTRIS	0.045	0.7	0.8	3.6	100/350/650*
Metal 3	rm3	SITRIS, MUTRIS	0.0135	2.3	7.0	3.7	100/350/650*

* MET/MET_MV/MET_HV values

XDH10 PIP CAPACITORS

Device	Name	Available with module	Area Cap [fF/µm²]	Perimeter Cap [fF/µm]	|BV| [V]	Max. VCC [V]
Poly1 gate oxide		CMOS	0.89		> 22	12
PolyD gate oxide		SITRIS, MUTRIS	0.42		> 30	-
Poly1-Poly2	cpp	CAPRES	0.39	0.095	> 22	15

XDH10 SANDWICH CAPACITOR

Device	Name	Available with module	|BV| [V]	Area Cap [fF/µm²]	Perimeter Cap. [fF/µm]	Max. VTB [V]	Max. VCC [V]
PolyD-M2-M3 Sandwich	csandwt	SITRIS, MUTRIS		0.037	0.045	650	650

XDH10 POD CAPACITOR

Device	Name	Available with module	Area Cap [fF/µm²]	Perimeter Cap [fF/µm]	Temp coeff [10^{-3}/K]	Max. VCC [V]
Poly1-gate oxide-N+	cpod	PODCAP	0.69	0.076	0.01	20

XDH10 PROTECTION DIODE

Device	Name	Available with module	BV [V]	Forward Voltage [V]	V temp co-eff [mV/K]	Max. Ibd[mA]
4.8V zener	dzeb	SITIRIS, MUTRIS	4.95	0.85	0.5	1
10V protection	dnda	SITIRIS, MUTRIS	20	0.95	10	1
45V protection	dpda	SITIRIS, MUTRIS	90	0.76	70	0.3
200V protection	dpwda	SITIRIS, MUTRIS	> 200	0.76	55	0.2
720V	dpwdb*	SITRIS	720	0.65	880	0.7
700V	dpwdc*	SITRIS	700	0.66	880	0.7

* with 2 centerpieces

XDH10 SCHOTTKY DIODES

Device	Name	Available with module	Forward Voltage [V]	I leakage [nA]	|BV| [V]	Max. Vreverse[V]
35V Schottky	dsa	SITRIS, MUTRIS	0.72	< 0.1	54	35
7V Schottky	dsb	CMOS	0.74	< 0.01	24	5

Passive Devices *(Continued)*

XDH10 DIFFUSION DIODES

Device	Name	Available with module	Area junc. cap. [fF/µm²]	Sidewall Cap. [fF/µm]	|BV| [V]	Junc. Potential [V]	Max. Vreverse [V]
NDIFF/PWELL	dn	CMOS	0.260	0.48		0.87	13
PDIFF/NWELL	dp	CMOS	0.320	0.43		0.83	16
PWELL/NSUB-NWELL	dpw	CMOS	0.050	0.35		0.50	27
PDIFFD/NSUB	dpd	SITRIS, MUTRIS	0.047	0.24	45	0.50	22
PWELLD/NSUB	dpwd	SITRIS, MUTRIS	0.040	0.68	130	0.50	100

XDH10 PROGRAMMABLE DEVICES

Device	Name	Available with module	BV, unzap [V]	Ileak, unzap [nA]	Rzapped [Ω]	Max Iread [mA]
Zener Zap	dzap	CMOS	4.8	50	50	1

Standard Cells Libraries

XDH10 STD CELLS LIB

Device	Voltage range	Category	Density *	r_factor **	Main features
D_CELLS	5.0V	standard	ML2: 0.5	ML2: 2.86	high speed

* library density: kGE/mm² at given routing factor (GE = NAND2 Gate Equivalent) ML2: 2 metal layer routing
** r_factor = Routing_factorPlace&Route_area = Cell_area * Routing_factor(averaged value: because routing factor, means wiring overhead, is netlist dependent)Utilization [%] = 1/routing_factor * 100, e.g. r_factor = 2.68; utilization = 1/2.86 * 100 = 35%

I/O Libraries

XDH10 I/O CELLS

Device	Library Feature	Voltage Range	Application benefits
IO_CELLS	Standard	3.3V & 5V	Core limited (x > y)

Analog Libraries

XDH10 OPERATIONAL AMPLIFIERS

Name	VOL [V]	VOH [V]	VICR [V]	VIO [mV]	AVD [dB]	B1 [kHz]	SR [V/µs]	PHM [°]	IDD [µA]	max. Load	Required modules
aopac01	0.35	VDD-1.15	0.35 ...VDD-1.7	<10	102	590	0.6/0.6	80	80	50pF/50kOhm	CORE, CMOS, CAPRES

Note: All Parameters are typical, VDD: 4.5V to 5.5V, T: -40 ....85 °C, all Opamps feature a standby mode

XDH10 COMPARATORS

Name	VICR [V]	TPD for 50mV Overdrive [ns] L->H/H ->L	Conditions CL [pF]; RL [kΩ]	Input Off-set Voltage [mV]	Supply Current [µA]	Required Module
acmpc01	0.2...VDD-1.55	810/880	1; 1000	< 10	5	CORE, CMOS
acmpc02	1.5...VDD-0.2	770/730	1; 1000	< 10	3	CORE, CMOS
acmpc03	0.1...VDD-0.1	270/240	1; 1000	< 20	65	CORE, CMOS
acmpc04	0.1...VDD-0.1	950/1150@1µA IBIAS	1; 1000	< 25	5 @1µA IBIAS	CORE, CMOS

Note: All Parameters are typical, VDD: VDD: 4.5V to 5.5V, T: -40 ....85 °C, all Comparators feature a standby mode

XDH10 POWER-ON-RESET

Name	DC-Current POR IDDL [µA]	High TresholdVoltage[V] (min/typ/max)	TDEL [µs]Delay VDD -> H to POR -> L(Voltage Rise Faster than 1V/µs) typical	Required Module
aporc01		2.5	16	CORE,CMOS
aporc02	1.3	2.6	13	CORE,CMOS
aporc03	1.3	2.5	13	CORE,CMOS

Note: All Parameters are valid for VDD: 4.5V to 5.5V, T: -40 ....85 °C

XDH10 RC OSCILLATORS

Name	Frequency [kHz]	Conditions	Supply Current (specified @ T=25°C) [µA]	Required Module
arcoc01	1000	@VDD=5.0V; T=25°C	37	CORE,CMOS,CAPRES
arcoc02	690/1000/1770	@VDD=5.0V; T=25°C, dig. code=1Fh/Fh/0Fh	36	CORE,CMOS,CAPRES
arcoc03	100	@VDD=5.0V; T=25°C	13	CORE,CMOS,CAPRES
arcoc04	69/100/175	@VDD=5.0V; T=25°C dig. code=1Fh/Fh/0Fh	13	CORE,CMOS

XDH10 ANALOG-TO-DIGITAL CONVERTERS

Name	Principle	Resolutions [Bits]	Accuracy [LSB] INL/DNL	Conversion Time [Clock Cycles]	Conversion Rate [kS/s]	Required Module
aadcc01	successive approximation	10	± 1.0 / ± 0.5	12	90	CORE, CMOS, CAPRES

Note: All Parameters are valid for VDD: 4.5V to 5.5V, T: -40 ....85 °C

Analog Libraries *(Continued)*

XDM10 DIGITAL-TO-ANALOG CONVERTERS

Name	Principle	Resolutions [Bits]	Accuracy [LSB] INL/DNL	Conversion Time [µs]	V Ref [V] (max)	Required Module
adacc01	voltage-scaling	10	±1.0/±0.5	1 @CL=5pF	VDDA	CORE, CMOS, CAPRES
adacc02	R-2R	8	±0.3/±0.4	0.5 @CL=1pF	VDDA	CORE, CMOS, CAPRES
adacc03	R-2R	10	±1.0/±2	0.5 @CL=1pF	VDDA	CORE, CMOS, CAPRES

Note: All Parameters are valid for VDD: 4.5V to 5.5V, T: -40 ....85 °C

XDH10 BIAS CELLS

Name	Bias Voltage VBP for PMOS [V]	Temperature Coefficient IVBP [ppm/°C]	Bias Voltage VBN for NMOS [V]	Temperature Coefficient IVBN [ppm/°C]	Supply Current [µA]	Required Module
abiac02	VDD-1.33	±500	1.24	±600	12	CORE, CMOS
abiac04	VDD-1.54	600	1.36	550	22	CORE, CMOS
abiac06	VDD-1.03	2400	1.05	2100	0.49	CORE, CMOS, CAPRES

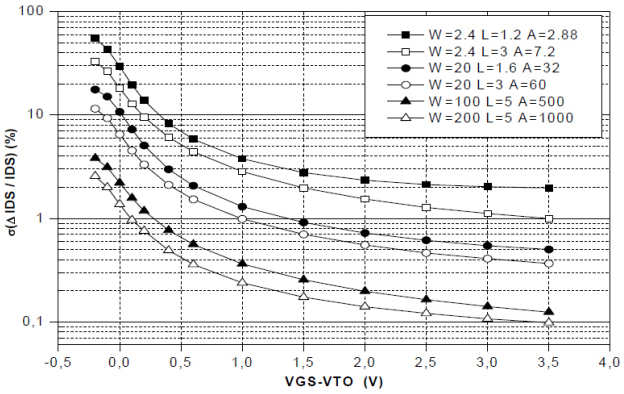
Note: All Parameters are typical, VDD: 4.5V to 5.5V, T: -40 ....85 °C, all Bias Cells feature a standby mode

XDH10 BIAS CELLS

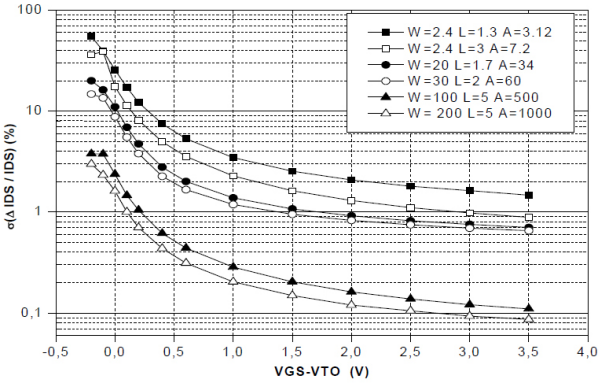
Name	Output Current IOUT [µA]	Temperature Coefficient IOUT [ppm/°C]	Supply Current [µA]	Required Module
acsoc02	1, 2, 4, 8	±1000	8.5	CORE, CMOS

Note: All Parameters are typical, VDD: 4.5V to 5.5V, T: -40 ....85 °C, all Bias Cells feature a standby mode

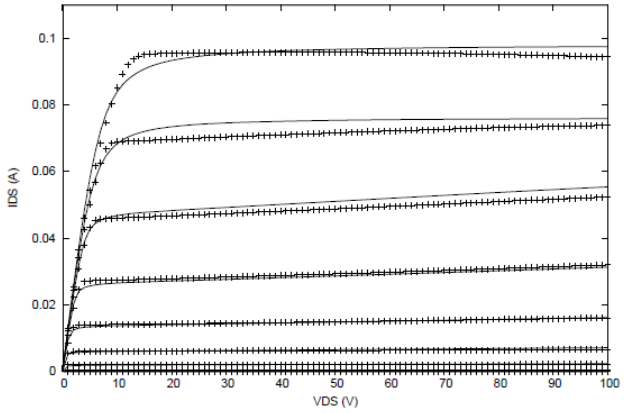
EXAMPLES FOR MEASURED AND MODELED PARAMETER CHARACTERISTICS



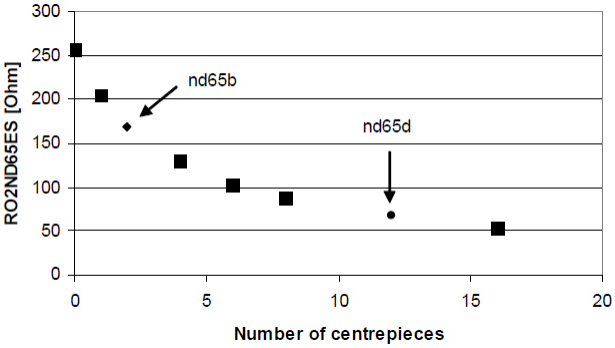
Device ne: drain current matching vs. VGS (typical value) legends show the drawn transistor lengths and widths



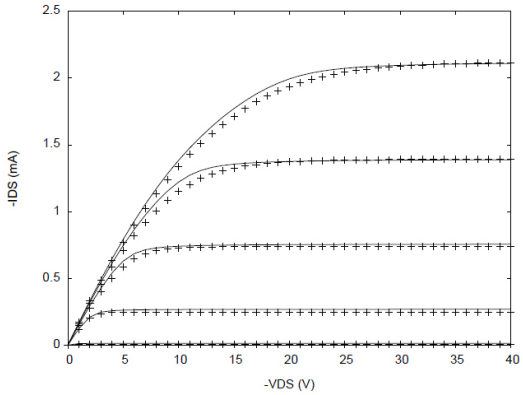
Device pe: drain current matching vs. VGS (typical value) legends show the drawn transistor lengths and widths



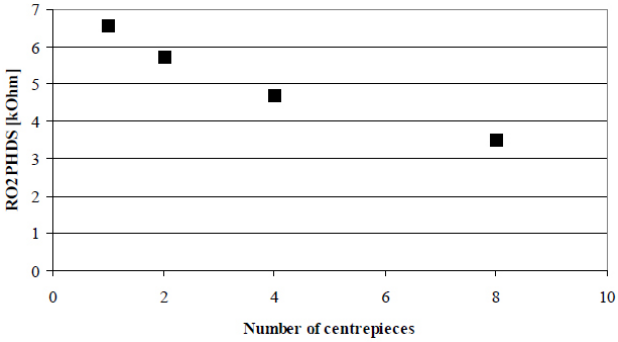
Output characteristic of a typical wafer (nd65d) VGS = 1.0, 1.2, 1.4, 1.6, 1.8, 2.0, 2.2, 2.4, 2.6, 2.8, 3.0V
+ = measured, solid line = SPICE model



On resistance Vs. Number of centrepieces of a typical wafer for device nd65es

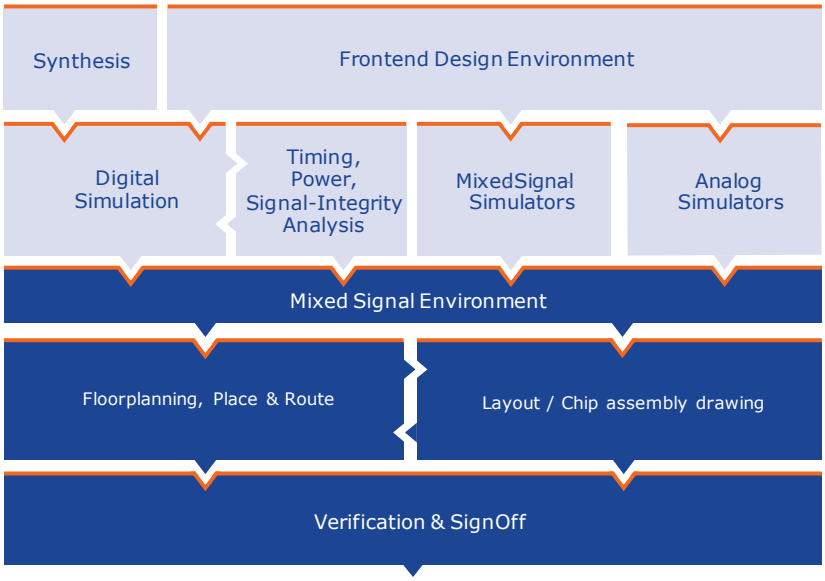


Output characteristic of a typical wafer (pha)
-VGS = 1.0, 2.0, 3.0, 4.0, 5.0V, VSB = 0V
+ = measured, solid line = SPICE model



On resistance Vs. Number of centrepieces of a typical wafer for device phds

XP018 SUPPORTED EDA TOOLS



Note: Diagram shows overview of reference flow at X-FAB. Detailed information of supported EDA tools for major vendors like Cadence, Mentor and Synopsys can be found on X-FAB's online technical information center X-TIC.

X-FAB'S IC DEVELOPMENT KIT "THEKIT"

The X-FAB IC Development Kit is a complete solution for easy access to X-FAB technologies. TheKit is the best interface between standard CAE tools and X-FAB's processes and libraries. TheKit is available in two versions, the Master Kit and the Master Kit Plus. Both versions contain documentation, a set of software programs and utilities, digital and I/O libraries which contain full front-end and back-end information for the development of digital, analog and mixed signal circuits. Tutorials and application notes are included as well. The Master Kit Plus additionally provides a set of general purpose analog functions mentioned in section "Analog Library Cells" and is subject to a particular license.

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