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Increasing MOS gate area reduces most variations, and experimental data confirms lower relative drain current mismatch, $\Delta I_D/I_D$, with increasing gate area.

In [183], MOS mismatch was separated into threshold-voltage, V_T , and transconductance factor, $\mu C'_{OX}(W/L)$, components. These were plotted separately against the inverse square root of gate area, $(WL)^{-1/2}$, showing a linear increase in mismatch with increasing $(WL)^{-1/2}$, which corresponds to decreasing gate area. These plots, which were developed further in [185], are commonly referred to as “Pelgrom” plots where both threshold-voltage and transconductance factor mismatch are proportional to the inverse square root of gate area, at least when area mismatch effects are dominant.

In [185], mismatch in the body-effect parameter, γ , was included and also shown to be proportional to the inverse square root of gate area through experimental “Pelgrom” plots. Variations in substrate doping, gate-oxide capacitance, and device geometry give rise to mismatch in γ . In the presence of non-zero V_{SB} , mismatch in γ results in additional threshold-voltage mismatch. This is discussed later in Section 3.11.1.5.

Threshold-voltage mismatch is usually the largest contributor to gate–source voltage and drain current mismatch as described later in Section 3.11.1.6. Threshold-voltage mismatch results from variations in threshold-voltage components, which include the gate–semiconductor work function difference, the substrate or body Fermi potential, and the depletion, fixed-oxide, surface-state, and implant charge densities divided by the gate-oxide capacitance [182, 183].

Variations in depletion charge caused by variations in the number of active dopant atoms under the gate usually dominate threshold-voltage mismatch [190, 206, 208, 227, 231, 236]. Threshold-voltage mismatch between two devices is then proportional to the mismatch in depletion charge density, $\Delta Q'_B$, divided by the gate-oxide capacitance, C'_{OX} , as expressed by

$$\Delta V_T \propto \frac{\Delta Q'_B}{C'_{OX}} \quad (3.133)$$

Threshold-voltage mismatch is then proportional to the relative mismatch in the number of active dopant atoms as expressed by

$$\Delta V_T (1\sigma) \propto \frac{Q'_B}{C'_{OX}} \left(\frac{\Delta n_{dop}}{n_{dop}} \right) = \frac{Q'_B}{C'_{OX}} \left(\frac{\sqrt{2}\sqrt{n_{dop}}}{n_{dop}} \right) = \frac{Q'_B}{C'_{OX}} \left(\frac{\sqrt{2}}{\sqrt{n_{dop}}} \right) \quad (3.134)$$

Q'_B is the average depletion charge density, n_{dop} is the average number of active dopant atoms under each gate, and $\Delta n_{dop} = \sqrt{2}\sqrt{n_{dop}}$ is the standard deviation or 1σ value of the number difference of dopant atoms between two MOS devices. The $\sqrt{2}$ term considers the additional standard deviation associated with two devices, where the standard deviation of the number of dopant atoms for a single device is equal to $\Delta n_{dop} = \sqrt{n_{dop}}$.

The rightmost expression in Equation 3.134 shows that threshold-voltage mismatch is inversely proportional to the square root of the average number of active dopant atoms under the gate. This makes intuitive sense as lower threshold-voltage mismatch would be expected from large devices having a large number of dopant atoms compared to small devices having a small number where the variability in the number is greater. The average number of dopant atoms under the gate is equal to the doping concentration in the substrate or body, N_B , multiplied by the depletion volume under the gate, WLt_{dep} , where t_{dep} is the depletion-region thickness under the gate. This gives

$$n_{dop} = N_B WL t_{dep} \quad (3.135)$$

Here, the body doping concentration N_B is assumed constant or average through the depletion region.

The average depletion charge density is given by the average dopant density under the gate, $N_B t_{dep}$, multiplied by the unit of electronic charge, giving

$$Q'_B = q N_B t_{dep} \quad (3.136)$$

Substituting Equations 3.135 and 3.136 into the rightmost expression in Equation 3.134 gives

$$\begin{aligned}\Delta V_T(1\sigma) &\propto \frac{q}{C'_{OX}} \left(\frac{\sqrt{2N_B t_{dep}}}{\sqrt{WL}} \right) = \sqrt{2\sqrt{2}} \frac{t_{ox}}{\epsilon_{SiO_2}} \frac{(q^3 \epsilon_{Si} \phi_s N_B)^{1/4}}{\sqrt{WL}} \\ &= \frac{A_{VTO} (V_{SB} = 0 \text{ V})}{\sqrt{WL}}\end{aligned}\quad (3.137)$$

In the top expression, $C'_{OX} = \epsilon_{SiO_2}/t_{ox}$ and $t_{dep} = (2\epsilon_{Si}\phi_s/(qN_B))^{1/2}$ are substituted from the expressions in Table 3.1 where t_{ox} is the gate-oxide thickness, ϵ_{SiO_2} is the permittivity of silicon dioxide, ϵ_{Si} is the permittivity of silicon, and ϕ_s is the silicon surface potential.

The top expression in Equation 3.137 is directly equal to the 1σ , threshold-voltage mismatch given in [208]. However, this expression is not directly equal to threshold-voltage mismatch given in [16, p. 129, 190, 231], but is larger by a constant factor resulting from differences in referring depletion charge mismatch to the gate. The top expression in Equation 3.137 is intended to illustrate mismatch trends with actual estimates of mismatch found from the bottom expression using the extracted threshold-voltage mismatch factor, A_{VTO} . A_{VTO} , summarized later with other local-area mismatch factors in Table 3.38, corresponds to the zero- V_{SB} , 1σ , threshold-voltage (ΔV_{TO}) mismatch between two identically laid-out devices having gate areas of $1 \mu\text{m}^2$ each.

From Equation 3.137, A_{VTO} is proportional to process parameters as given by

$$A_{VTO} (V_{SB} = 0 \text{ V}) \propto \frac{q}{C'_{OX}} \sqrt{2N_B t_{dep}} = \sqrt{2\sqrt{2}} \frac{t_{ox}}{\epsilon_{SiO_2}} (q^3 \epsilon_{Si} \phi_s N_B)^{1/4} \quad (3.138)$$

For a $0.18 \mu\text{m}$ CMOS process having $N_B = 7 \times 10^{17}/\text{cm}^3$ ($7 \times 10^5/\mu\text{m}^3$), the depletion region thickness is $t_{dep} = 0.043 \mu\text{m}$. This assumes $V_{SB} = 0 \text{ V}$, $PHI = 2\phi_F = 0.913 \text{ V}$ at $T = 300 \text{ K}$, and an approximate strong-inversion surface potential of $\phi_s = \phi_0 \approx 2\phi_F + 4U_T \approx 1 \text{ V}$ from the expressions given in Table 3.1. The average doping density under the gate is then equal to $N_B t_{dep} = 30000/\mu\text{m}^2$. For $t_{ox} = 4.1 \text{ nm}$, which gives $C'_{OX} = 8.41 \text{ fF}/\mu\text{m}^2$ from the expression in Table 3.1, $A_{VTO} = 4.7 \text{ mV} \cdot \mu\text{m}$ when directly evaluated from Equation 3.138. This is close to $A_{VTO} = 5 \text{ mV} \cdot \mu\text{m}$ listed in Table 3.3 for the example $0.18 \mu\text{m}$ process, but is above A_{VTO} values estimated from threshold-voltage mismatch given in [16, p. 129, 190, 231] because of differences in constant factors mentioned earlier. As described later in Section 5.5.2.5, measured input-referred offset voltages for example $0.18 \mu\text{m}$ CMOS operational transconductance amplifiers are well predicted using the value of $A_{VTO} = 5 \text{ mV} \cdot \mu\text{m}$.

Equations 3.137 and 3.138 suggest that threshold-voltage mismatch decreases directly as t_{ox} decreases in smaller-geometry processes. However, mismatch is proportional to $N_B^{1/4}$, which increases in smaller-geometry processes and partially counters the mismatch decrease associated with decreasing t_{ox} [208]. As a result, threshold-voltage mismatch decreases less rapidly than t_{ox} decreases in new processes as shown in reported mismatch factors in the next section. Additionally, as described in the next section and Section 3.11.1.3, gate non-uniformity [227], inversion layer quantization [229], and other effects may contribute to threshold-voltage mismatch and affect technology trends.

Threshold-voltage mismatch is usually assumed to be independent of the inversion level or $V_{EFF} = V_{GS} - V_T$. Equations 3.137 and 3.138 suggest only a small mismatch increase as t_{dep} increases slightly in strong inversion through the slight increase in ϕ_s . ϕ_s increases from approximately $\phi_s = PHI = 2\phi_F$ at the boundary of weak and moderate inversion [15, p. 87] to a nearly “pinned” value of $\phi_s = \phi_0 \approx 2\phi_F + 4U_T$ in strong inversion.

Threshold-voltage mismatch increases for non-zero V_{SB} in the usual, reverse-biased direction [185, 188, 192, 196, 209]. Equations 3.137 and 3.138 predict a mismatch increase through the increase in t_{dep} associated with adding V_{SB} to the value of ϕ_s . In the less usual case when V_{SB} is slightly forward biased, mismatch is reported to decrease as the result of gated lateral bipolar transistor action [192, 196]. The V_{SB} component of threshold-voltage mismatch is not included in the value of A_{VTO} , which,