

Status of the Low-Power A/D-Converter cell for the ALICE-TRD

David Muthers
Reinhard Tielert

Institute of Microelectronics
University of Kaiserslautern

Overview:

- ADC Requirements
- Cyclic AD-Conversion
- ADC-System
- Improving the accuracy
- Analog Interface
- Timing of the digital signals
- Layout views
- Measurements
- Sources of error
- Improvements for ADC2

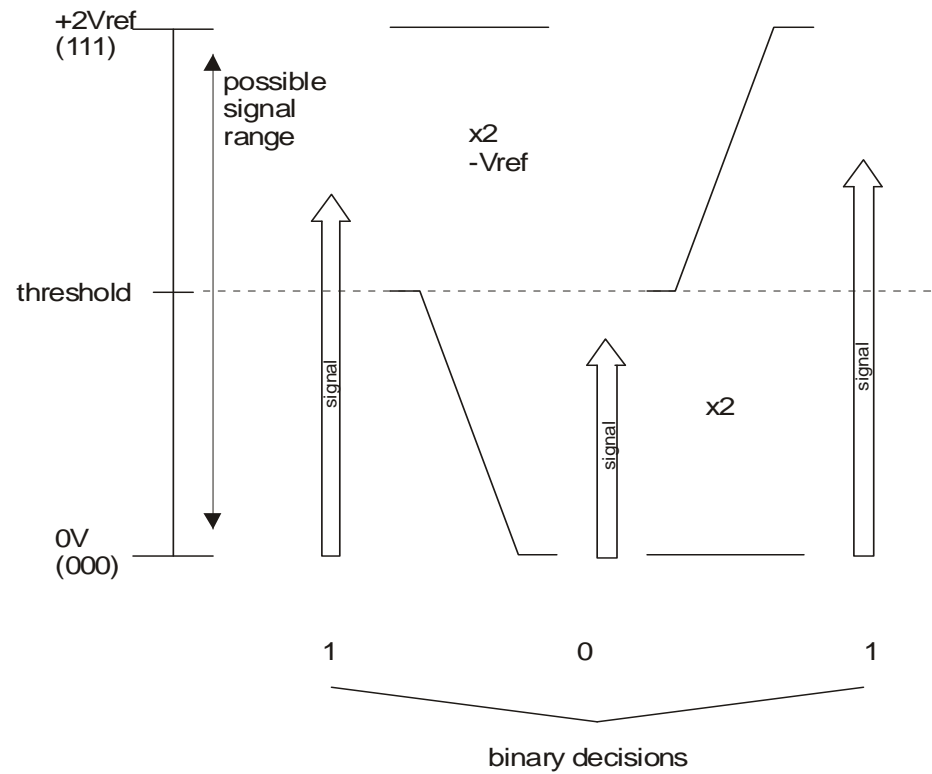
ADC-Requirements:

Table 5.3: ADC requirements

Parameter	Value
Resolution	10 Bit
Digitization rate	10 MHz
Max Power consumption	20 mW
Input	2 V differential (+/- 1 V)
Input bandwidth	5 MHz
Max. differential non-linearity	0.7 LSB for channels [0, 511] 1.5 LSB for channels [512, 1023]
Max. integral non-linearity	1.0 LSB for channels [0, 511] 2.0 LSB for channels [512, 1023]
Effective Number of Bits	> 9 Bit
Max. latency	5.5 clocks
Min. input impedance	100 k Ω
Max. input capacity	7 pF
Max. area	2 mm ²
Max. channel to channel variations on same die	0.5 %

Principle of Cyclic AD-Conversion:

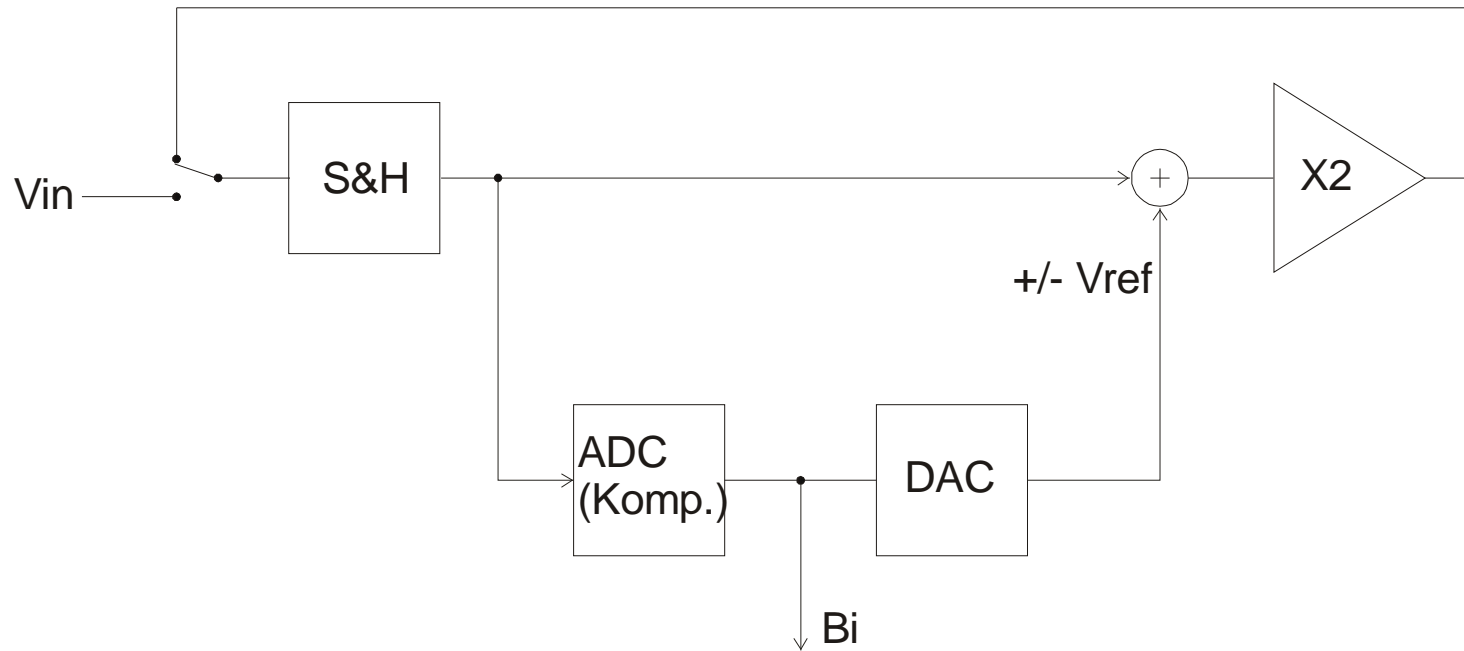
Example of quantization process:



essential Operations:

- comparison
- $\pm V_{ref}$
- x2
- (Sample&Hold)

ADC-Stage:



Pipeline Converter: for n Bit quantization n stages, settling time for each stage $t = \frac{1}{f_{sample}}$

Cyclic Converter: one stage, settling time

$$t = \frac{1}{n \times f_{sample}}$$

Settling time depends mainly on speed of amplifier

Unity-gain frequency (f_T):

$$f_{T,zyk} = \frac{1}{2\pi} \frac{g_{m,zyk}}{C} = n \frac{1}{2\pi} \frac{g_{m,pipel}}{C}$$

(g_m : Transconductance of amplifier; C: Loadcapacitance, fixed due to $\frac{kT}{C}$ -noise)

$$g_{m,zyk} = n \times g_{m,pipel}$$

With $P \sim g_m$ (const. $\frac{I}{W}$ of the MOS-Transistors)

$$P_{zyk} = n \times P_{pipel}$$

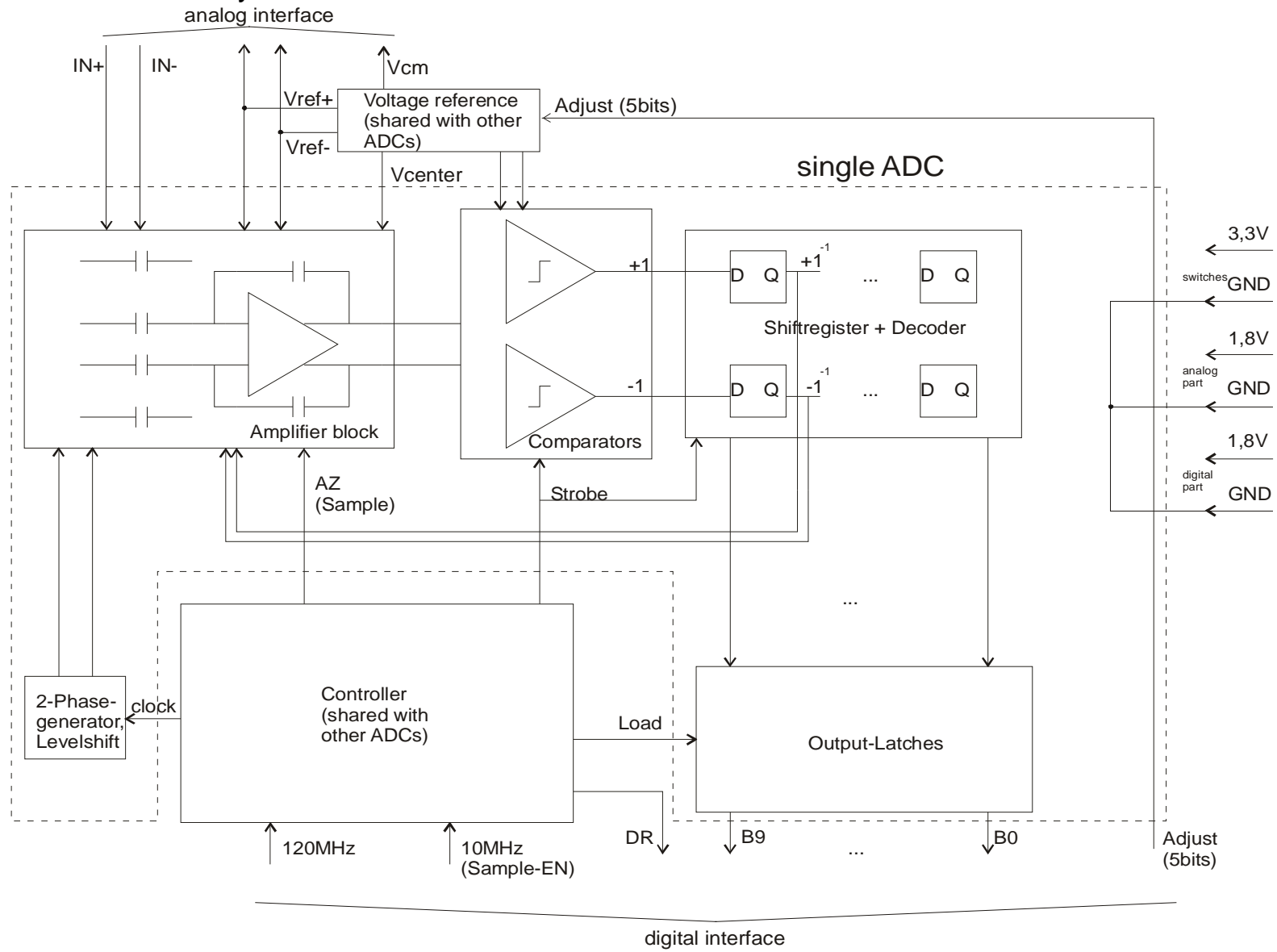
This equation is valid for each stage. With all n stages of the Pipeline-converter, we get:

$$P_{ges,pipel} = n \frac{1}{n} P_{zyk} = P_{zyk}$$

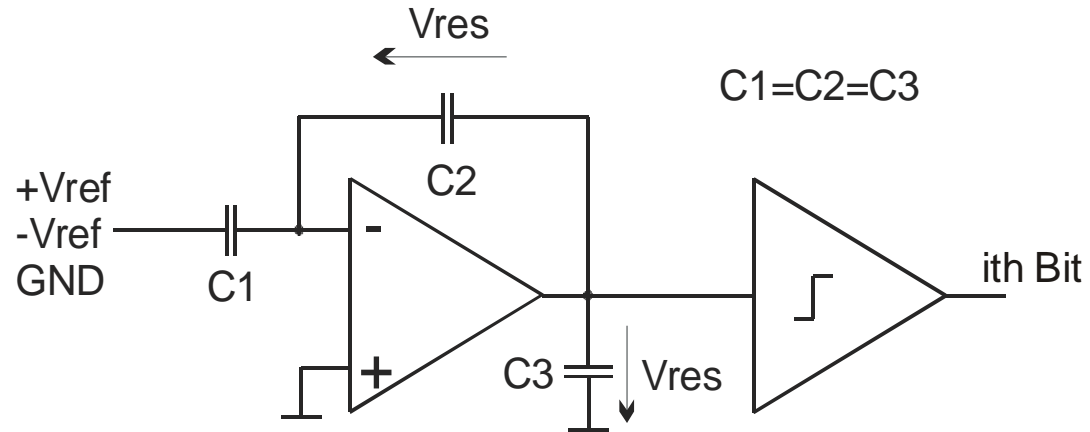
Powerconsumption of both converters approx. equal, required Area (one stage) of cyclic converter much lower

Choose cyclic converter, if design of an amplifier of appropriate speed is possible

System overview of the cyclic ADC



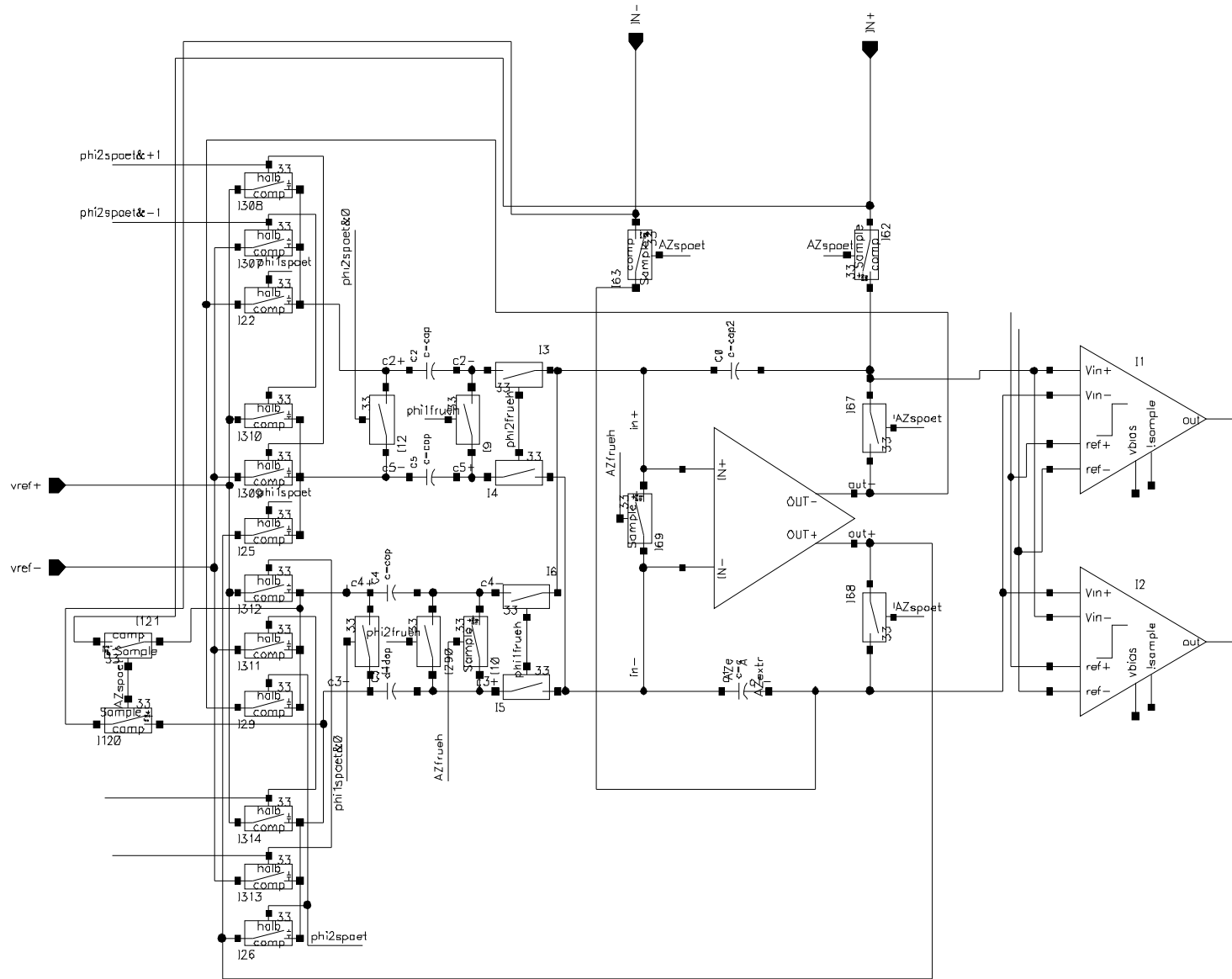
Function of amplification-block (only single-ended shown here):



Exchanging of C_1 and C_3 : $V_{res,i} = 2V_{res,i-1}$

$\pm V_{ref}$ to C_1 : $V_{res,i} = 2\left(V_{res,i-1} - \frac{V_{ref}}{2}\right)$

Schematic of differential amplification-block :



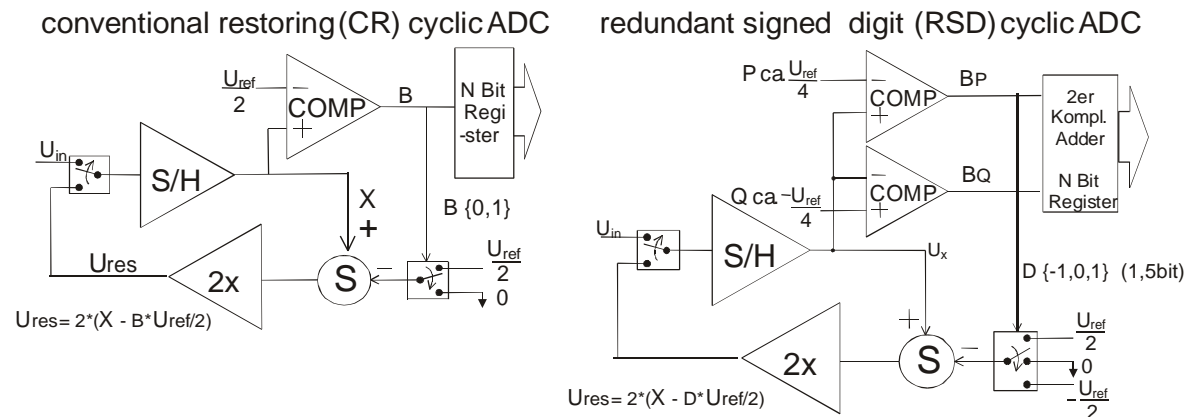
Improved accuracy of ADC:

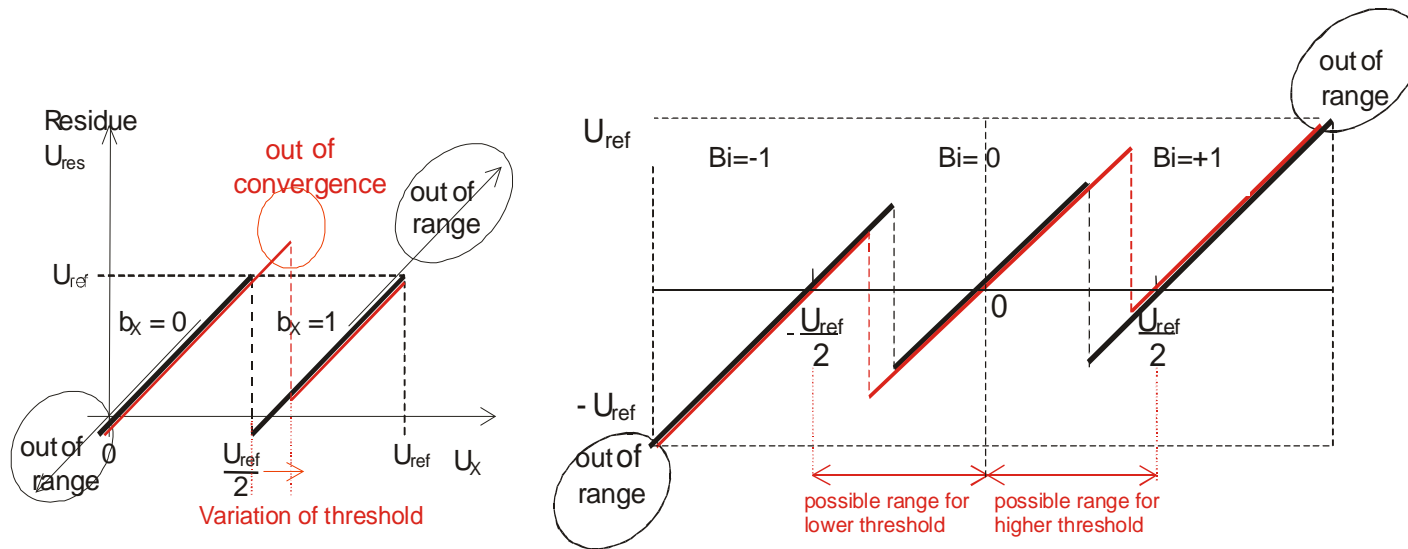
- use of redundant-signed-digit principle (RSD):

Offset of Comparator: too large residue can cause overflows

applying a second, redundant threshold solves this problem (RSD, redundant signed digit)

large offset of comparators possible, low-performance comparators sufficient





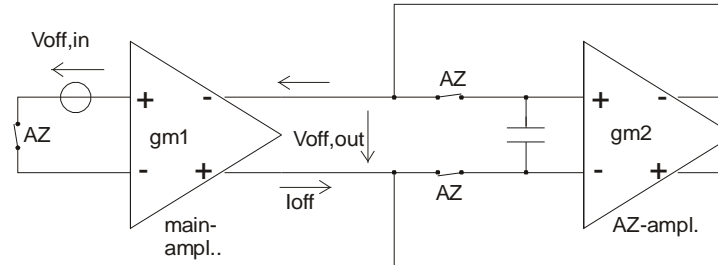
Transfer functions of one stage for conventional restoring and RSD-converter

RSD produces 2 bit strings, which have to be logically combined in the shift register. Comparator-offsets introduce no error, as long as $\pm V_{ref}$ is done correctly.

- Offset of Amplifier: shifts the transferfunction of the ADC by $\pm 2V_{off}$

Compensation necessary

in SC-circuits: Autozero (AZ) possible:



AZ-phase: (AZ-switches closed)

$$I_{off} = g_{m1} \times V_{off, in, uncomp}$$

$$V_{off, out} = -\frac{I_{off}}{g_{m2}} - V_{off, 2} = -\frac{g_{m1}}{g_{m2}} V_{off, in, uncomp} - V_{off, 2} \approx -V_{off, in, uncomp} - V_{off, 2}$$

$$V_{off, in, komp} = \frac{V_{off, out}}{a_{v1}} = \frac{-V_{off, in, uncomp} - V_{off, 2}}{a_{v1}} \approx -\frac{2V_{off, in, uncomp}}{a_{v1}}$$

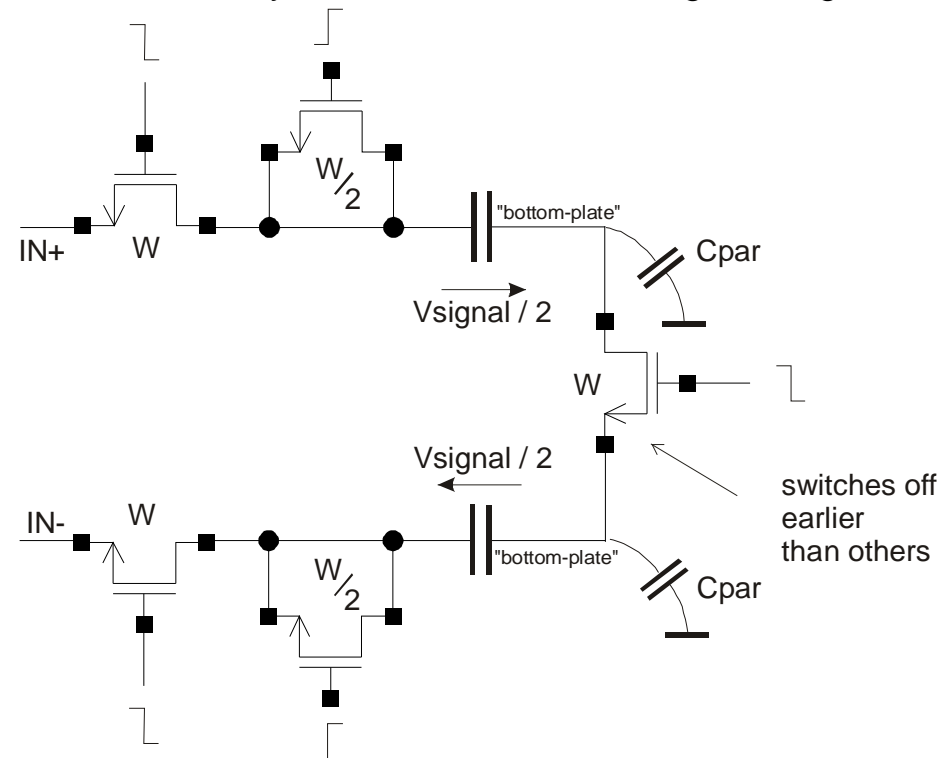
The input referred offset is reduced by $\frac{a_{v1}}{2}$.

AZ is done during Common-mode-setting, while the ADC samples, so no time is lost.

- Analog switches:

MOS-Transistoren inject charge in drain and source nodes when turning off. Charge is splitted by the ratio of the admittance at D and S (approx.).

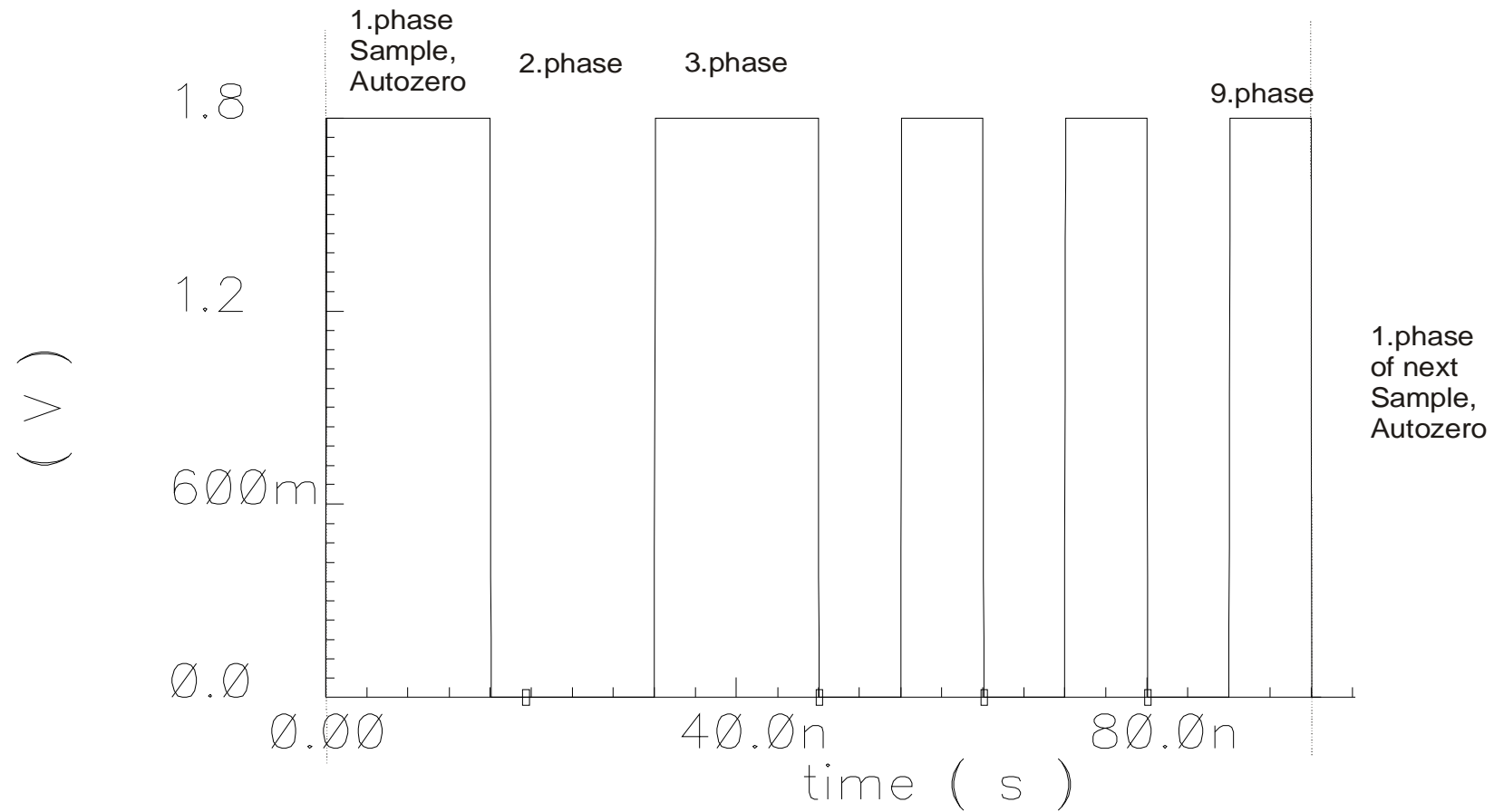
UMC-process offers 3,3V-Transistors, which are most suitable for the switches. 3,3V-power-supply is available on this chip, too. This allows to use NMOS-only switches for the 1,8V signal range.



„Bottom-Plate-Sampling“: appropriate sequence of turning off the switches minimizes perturbations. Rightmost switch turns off first, injecting only common-mode-charge. Other switches turn off later, injecting differential charge, but influence on signal voltages on capacitors is small due to capacitive voltage division with C_{par} . Influence is minimized further by compensation switches switching in opposite direction.

- Longer first cycles:

Conversion takes 9 cycles (due to RSD), 120MHz-clock offers 12 cycles per conversion: make first three cycles longer to improve settling.



Design approaches to minimize the power consumption:

- minimize capacitors:

Most power is used to charge the switched capacitors.

Noise must be kept well below 1 LSB, so working with an as large as possible signal range allows more noise and thus smaller capacitors. In this design the signal range is $\pm 1\text{V}$ with 1,8V power supply.

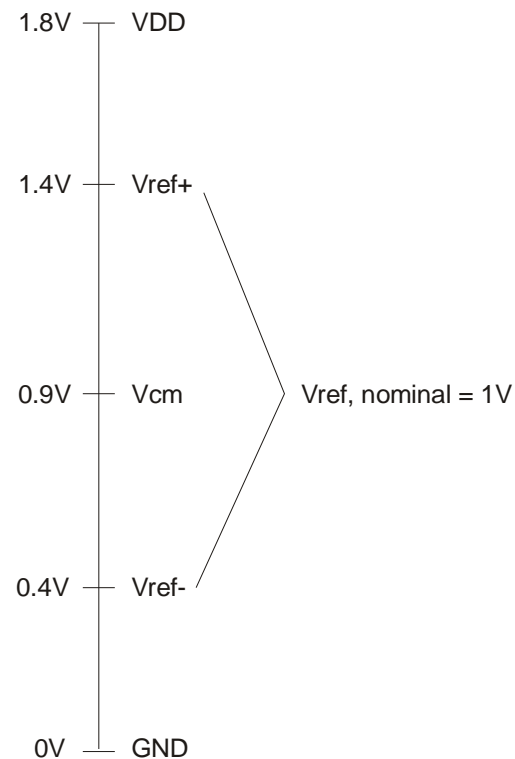
- waste no time:

timing diagram shows that there are no idle phases, sampling and Autozero happen simultaneously this makes settling times as long as possible, minimizing the necessary currents in the amplifier.

Analog Interface to Preamplifier:

IN+, IN-: differential Inputs of ADC, maximum differential voltage as large as V_{ref} , differential input capacitance 1.5pF. The Common-mode-voltage must not differ from 0,9V (half VDD).

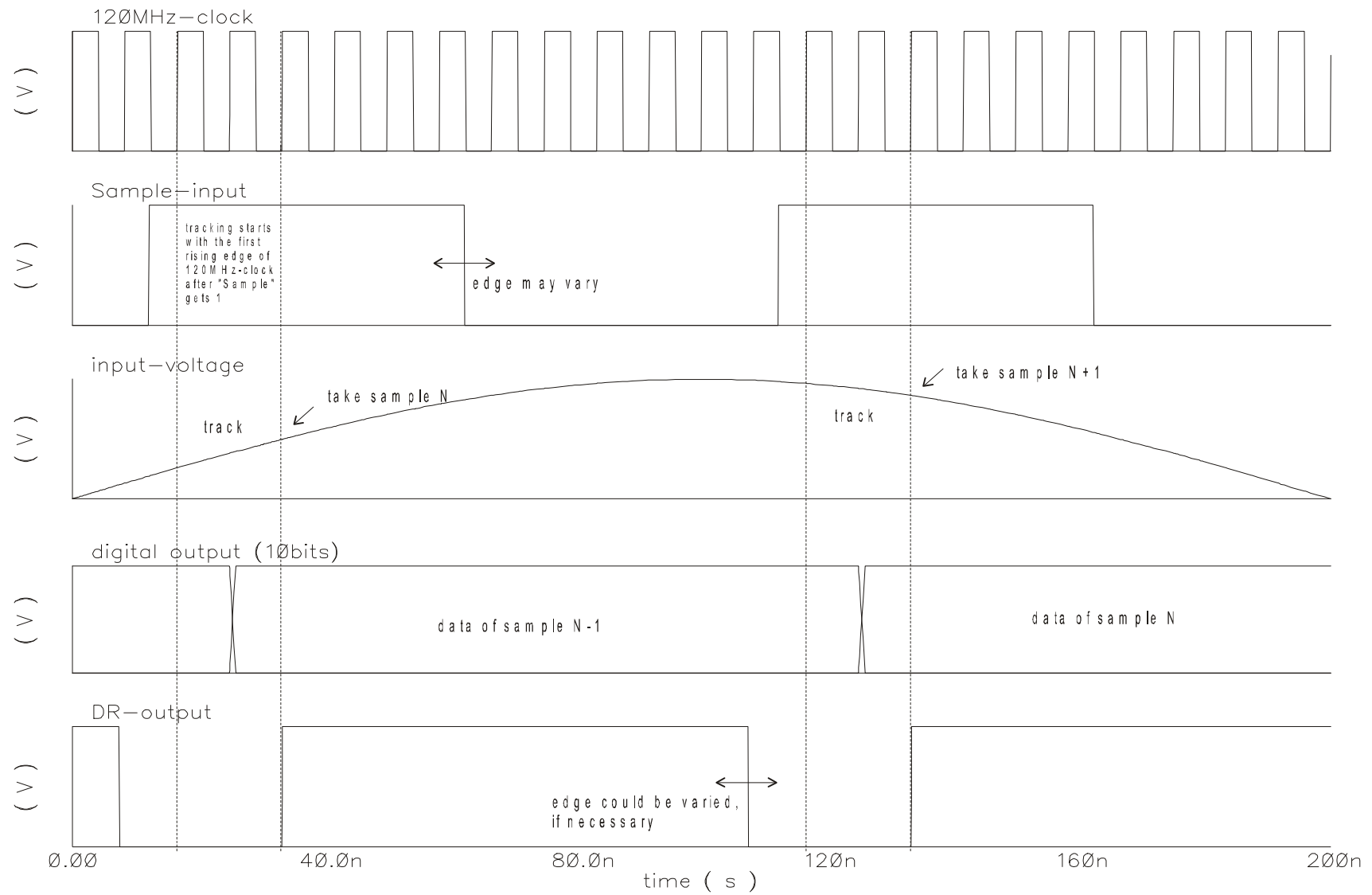
$V_{\text{ref+}}$, $V_{\text{ref-}}$, V_{cm} : Outputs of Voltage Reference



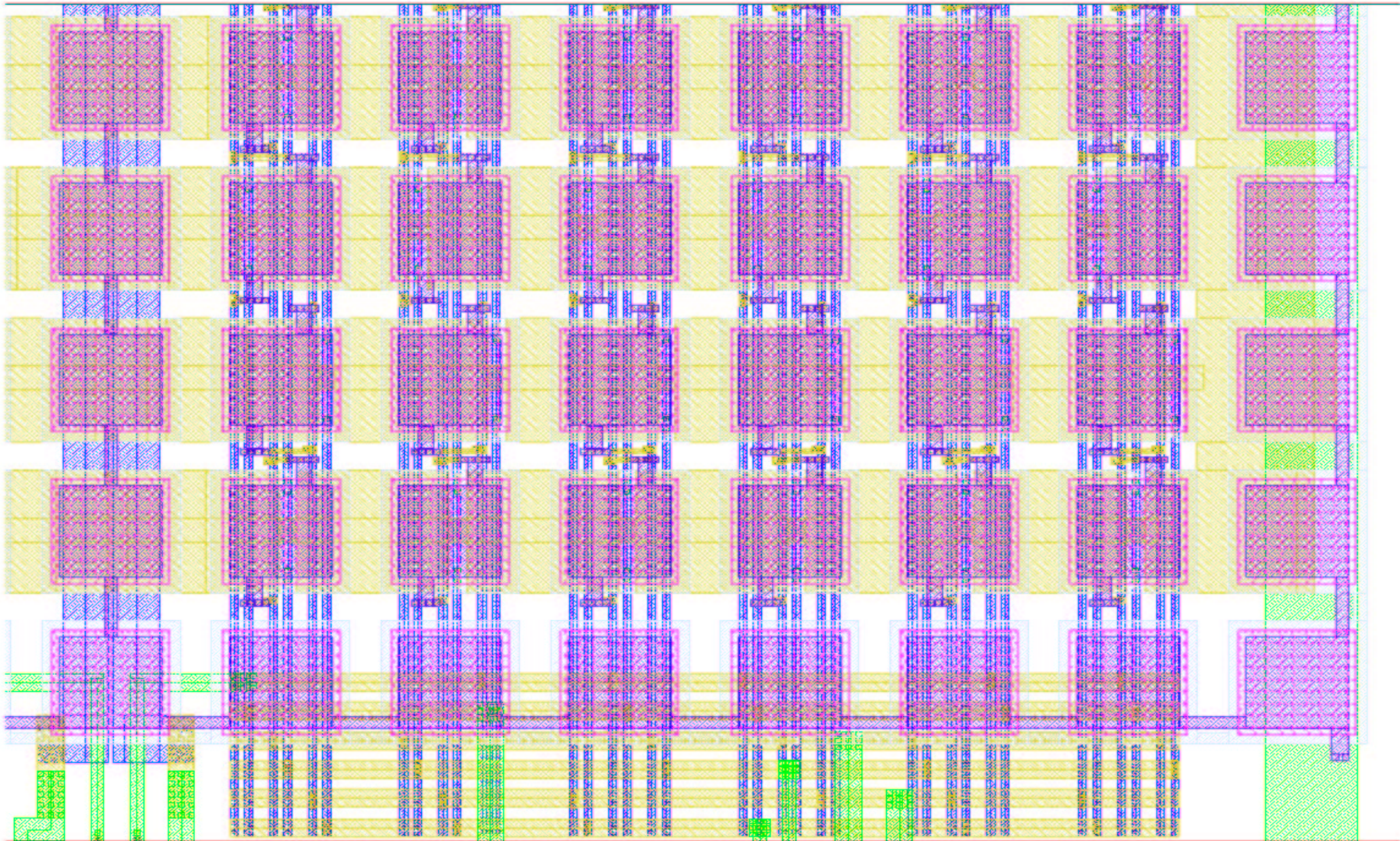
The nominal reference voltage is 1V, symmetrically around 0,9V. With the „Adjust“-bits the differential voltage of the reference can be varied in the range from 0.8V to 1.2V, symmetrically around 0,9V.

$V_{\text{ref+}}$, $V_{\text{ref-}}$, V_{cm} (Common-mode-voltage for Preamp) serve as Outputs to the Preamplifier. V_{cm} can be adjusted from 0.7 to 1.1V to equalize Common-mode-errors of the Preamplifier, caused by internal mismatches.

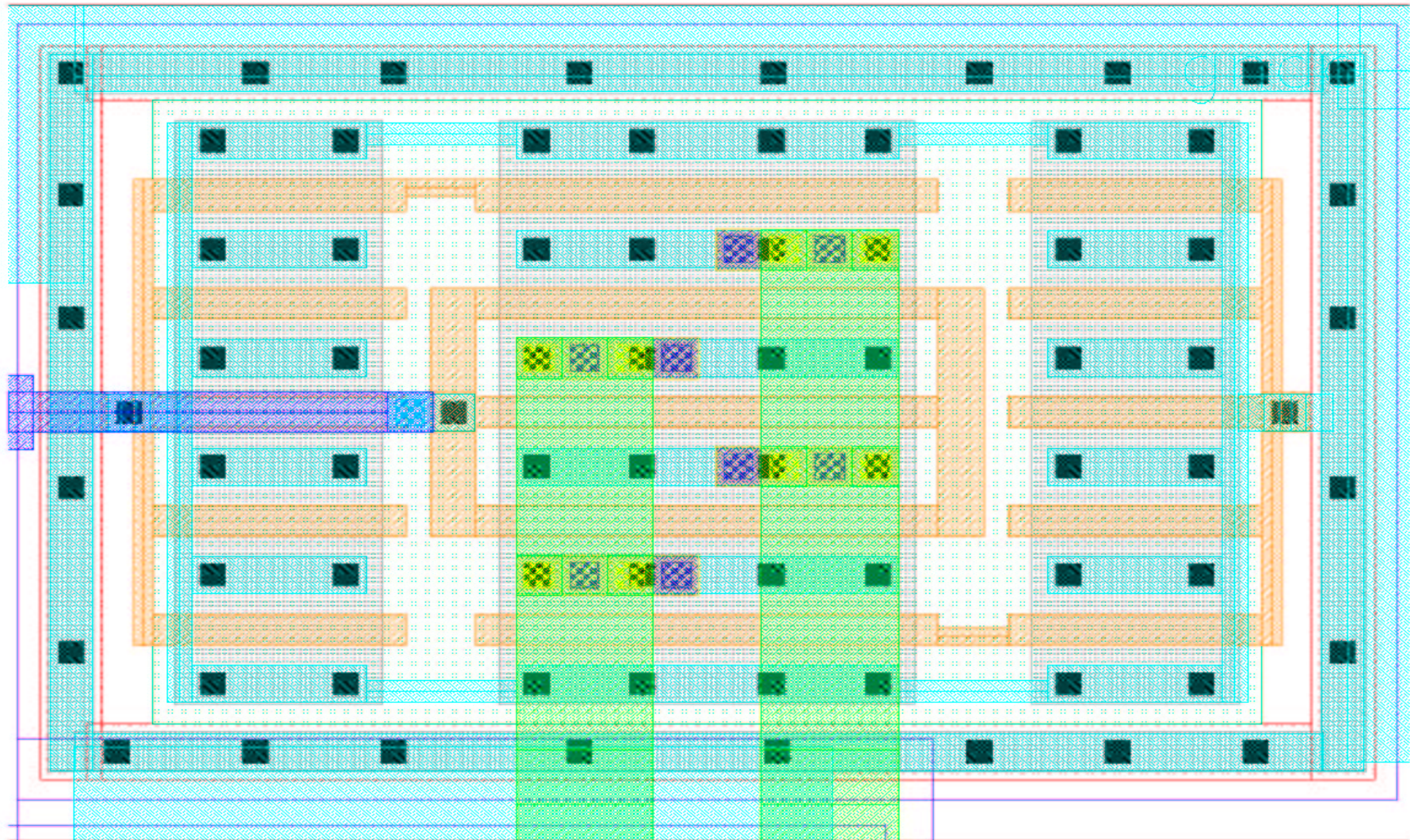
Timing of the digital signals:



Design pictures: array of matched capacitors with wiring



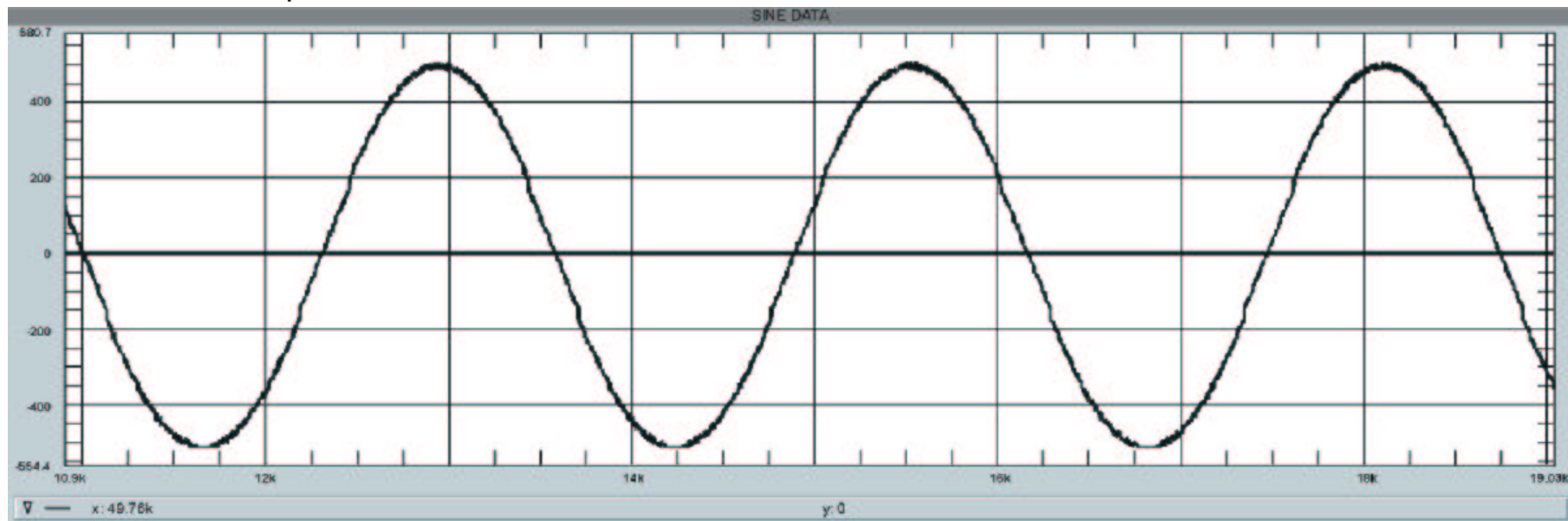
Switch with dummy devices:



Measured results:

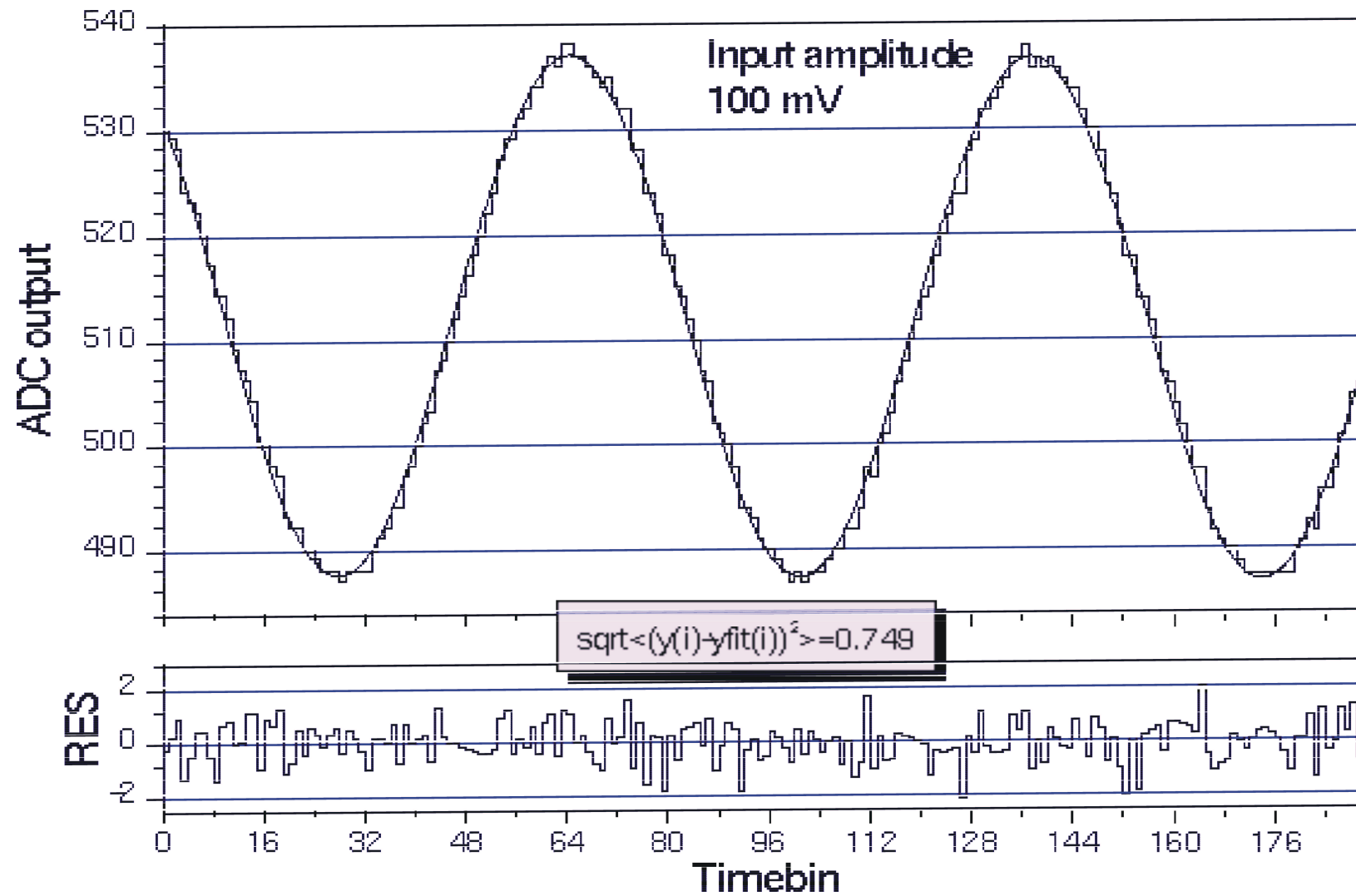
- first silicon is fully functionable and could be analyzed for the redesign
 - runs at 120MHz (up to ~140MHz), i.e. 10MSPS is obtainable
 - runs from 1.6V - 2.0V and 3.0V - 3.6V resp., i.e. fullfills supply-voltage specifications
 - power consumption of 5mW/6mW is correct (2 different versions were implemented), i.e. 3 times less than commercial cell
 - area consumption 0.1mm^2 , i.e. ~15 times smaller than commercial pipeline converter cell
- ADCs were implemented with test buffers to enable stand-alone tests. Unfortunately loaded test buffers disturb the measured signal noticeably due to current spikes.

1kHz sinewave, sampled at 5MSPS:



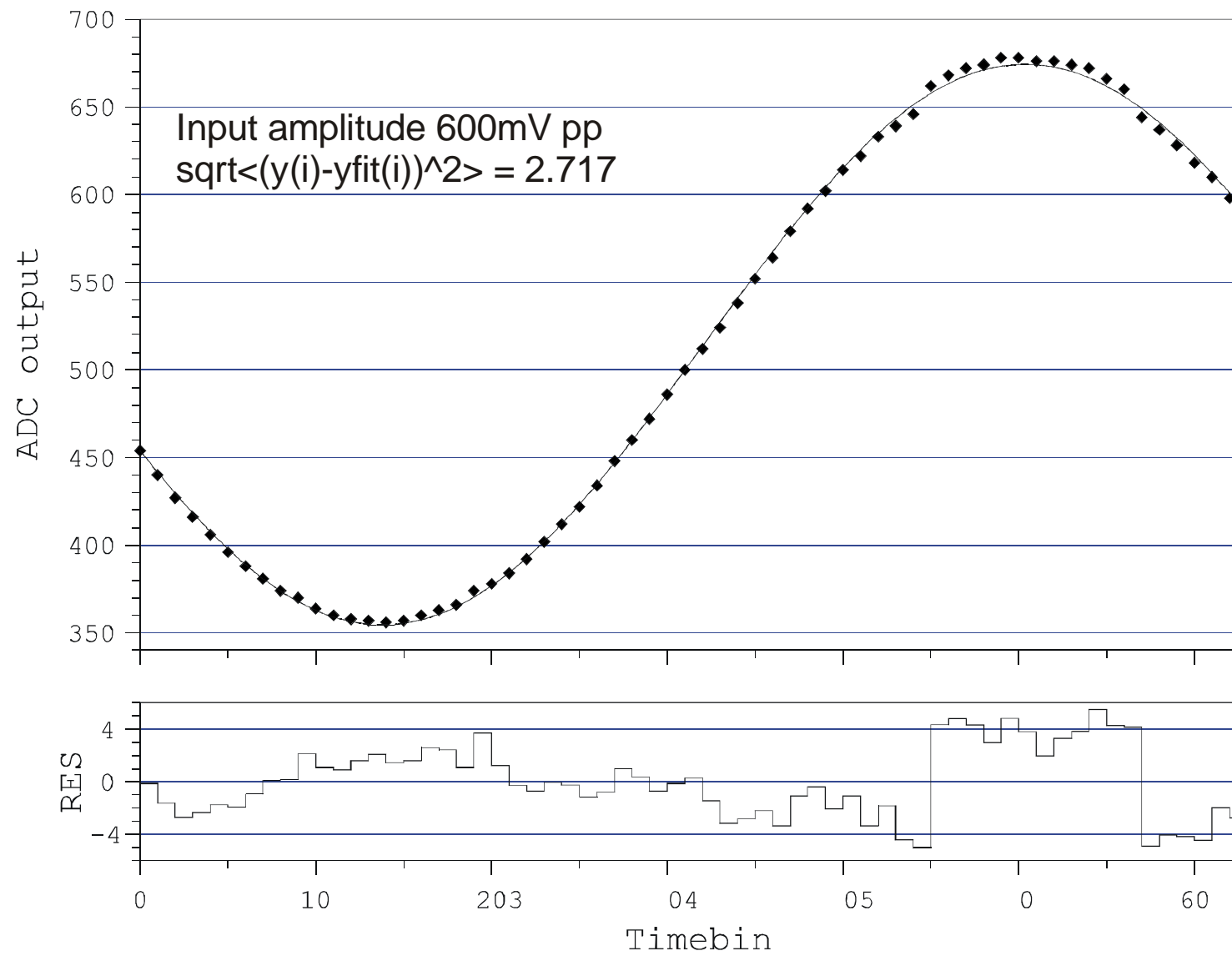
~15LSB peak to peak noise, coming from test buffers

Better measurements were possible using interface to digital part of testchip, no loads connected to the test interface.

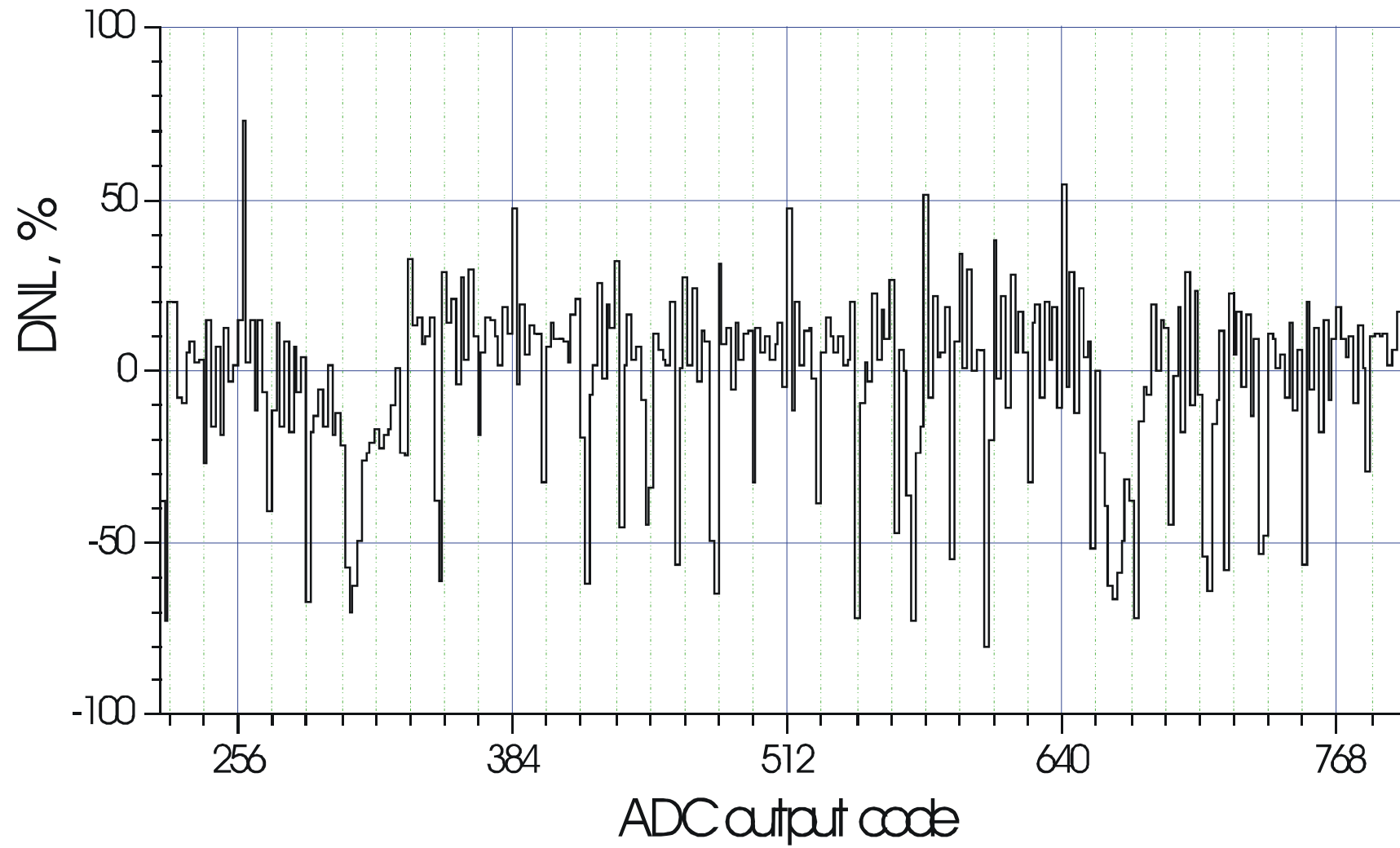


Number of samples is limited with this data acquisition method, digital part ran with 50MHz

Sampled 600mV(pp) sinwave:



DNL:



Measurement shows systematic errors in linearity:

- steps of 8 codes in measured waveform around codes $(512+128)$ and $(512-128)$

Discussion of reasons and possible solutions:

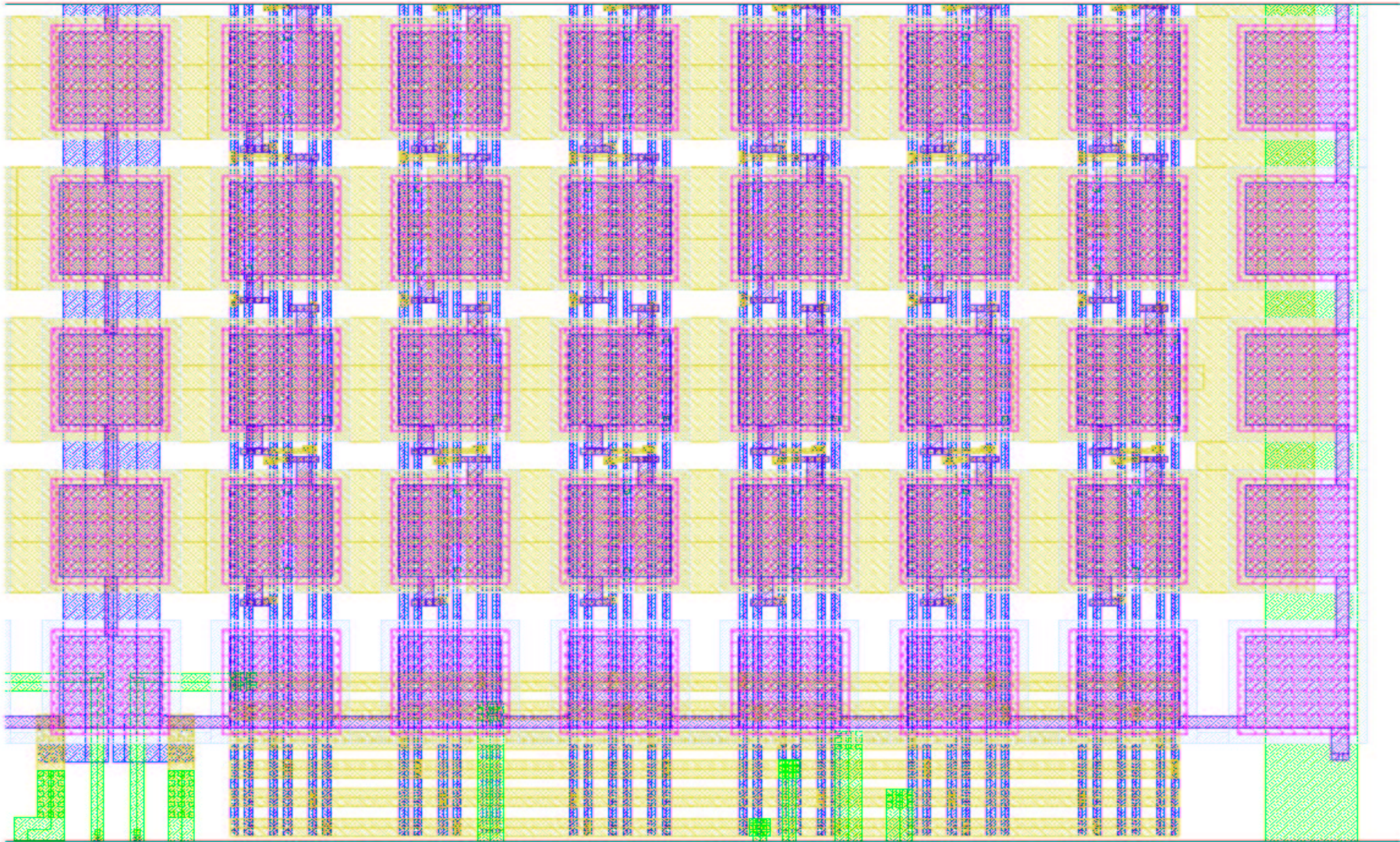
gain of internal amplifier is different from 2, but usual reasons (capacitor mismatch, insufficient loop gain, insufficient settling) are not responsible.

the ADC-layout employs some undesired parasitic capacitances in the capacitor field that lead to this wrong gain.

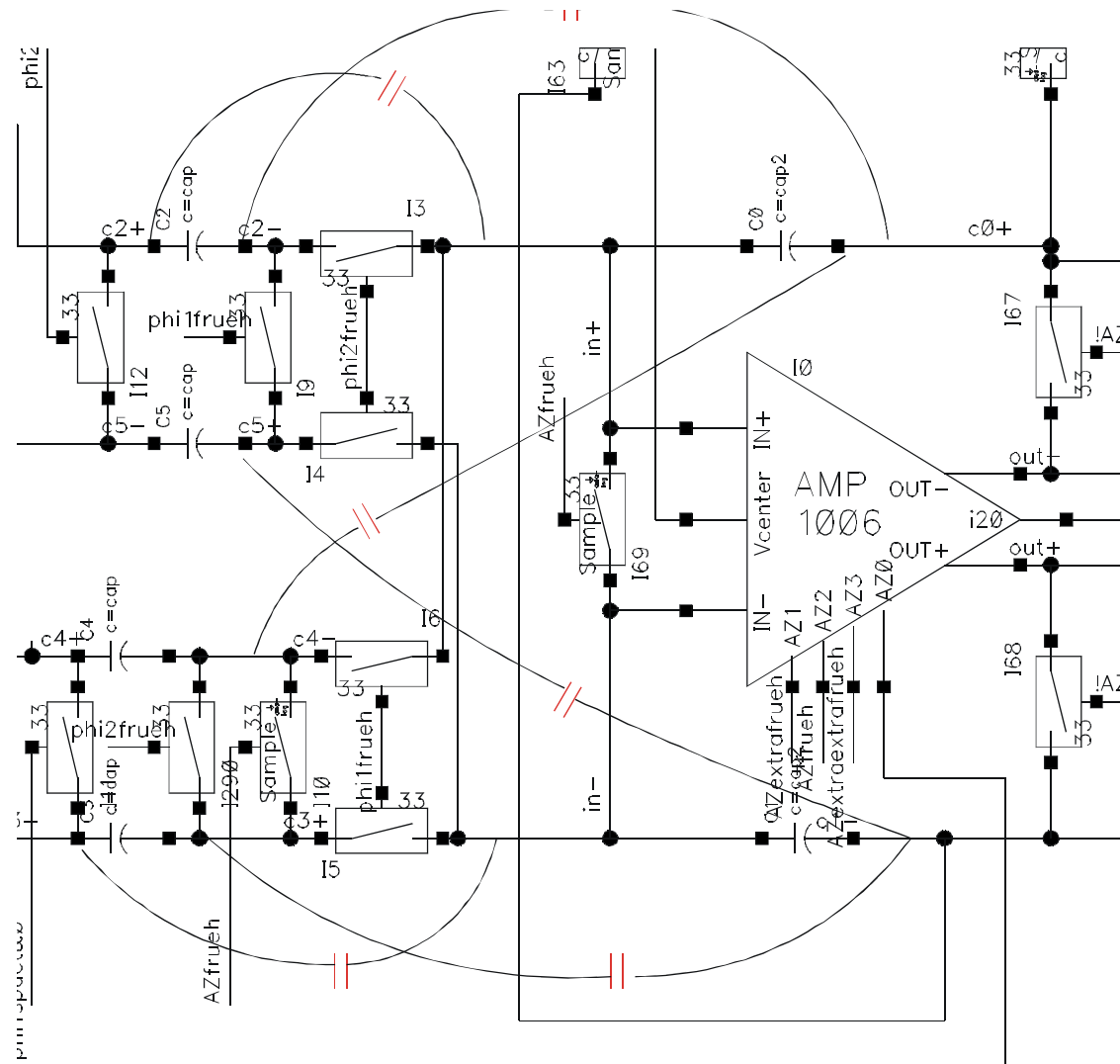
capacitors consist of metal5 and extra metal layer, wiring is done in metal2 below shield of metal3

coupling capacitors are between 15fF and 20fF, nominal capacitors are 1pF

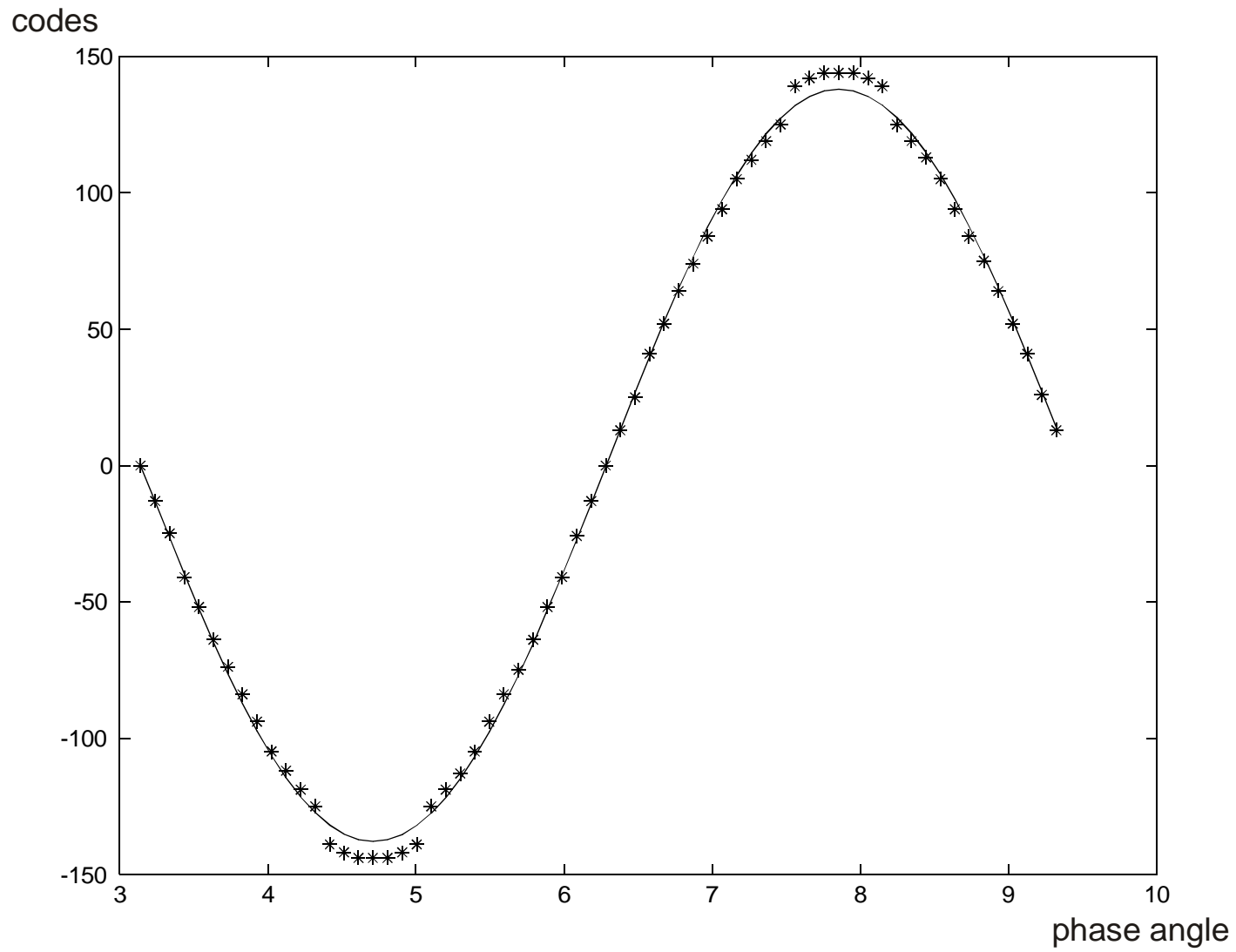
capacitor array with wires (blue, yellow)



the parasitic capacitances are marked in red:



MatlabSimulation of the ADC-behavior with this parasitic capacitors (600mVpp sine, 64 samples per period)



- some parts of ADC are sensitive to power supply noise, proven by the disturbance from the heavily loaded output drivers of the test interface and several measurements with different power connections and decoupling methods. Currently the internal reference-handling is not fully differential, this will be changed in the redesign.

- due to a non-optimal timing the comparator-decision for the last bit tends to be 0. The Autozero starts too early, zeroing the signal while the comparator has not yet fully latched.

The supply voltage has influence on this timing, lowering VDD eliminates this problem.

Table shows the relation VDD - 0/1-ratio (counted from 64-sample measurements)

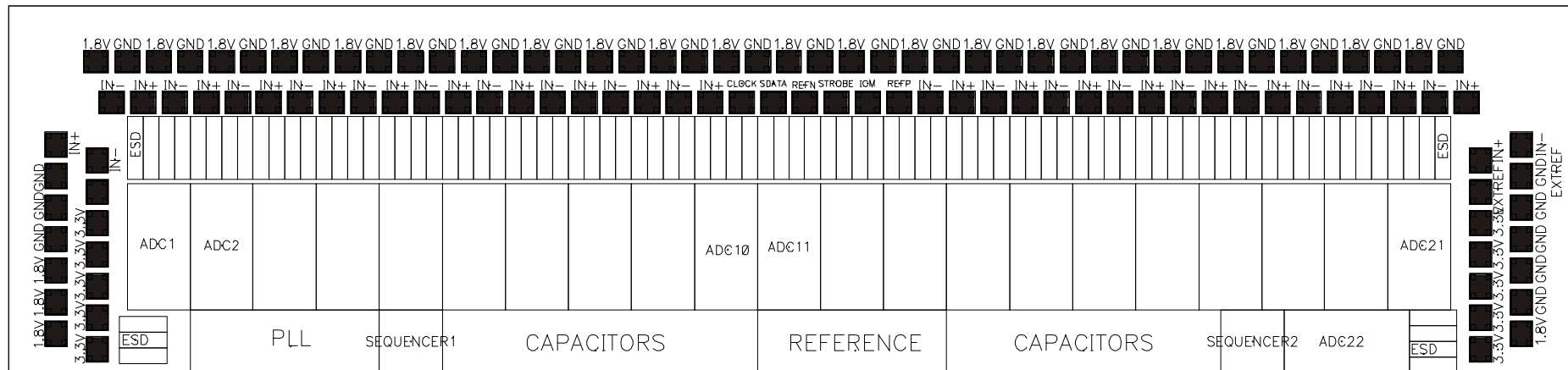
VDD	Ratio 0 / 1
1.9V	99% / 1%
1.8V	82% / 18%
1.7V	59% / 41%
1.6V	53% / 47%

Forseen changes in the design of ADC2 for TRAP2:

TRAP2 will have 22 ADCs, located in slices to connect directly to the PASA-Chip

ADC—placing of TRAP2

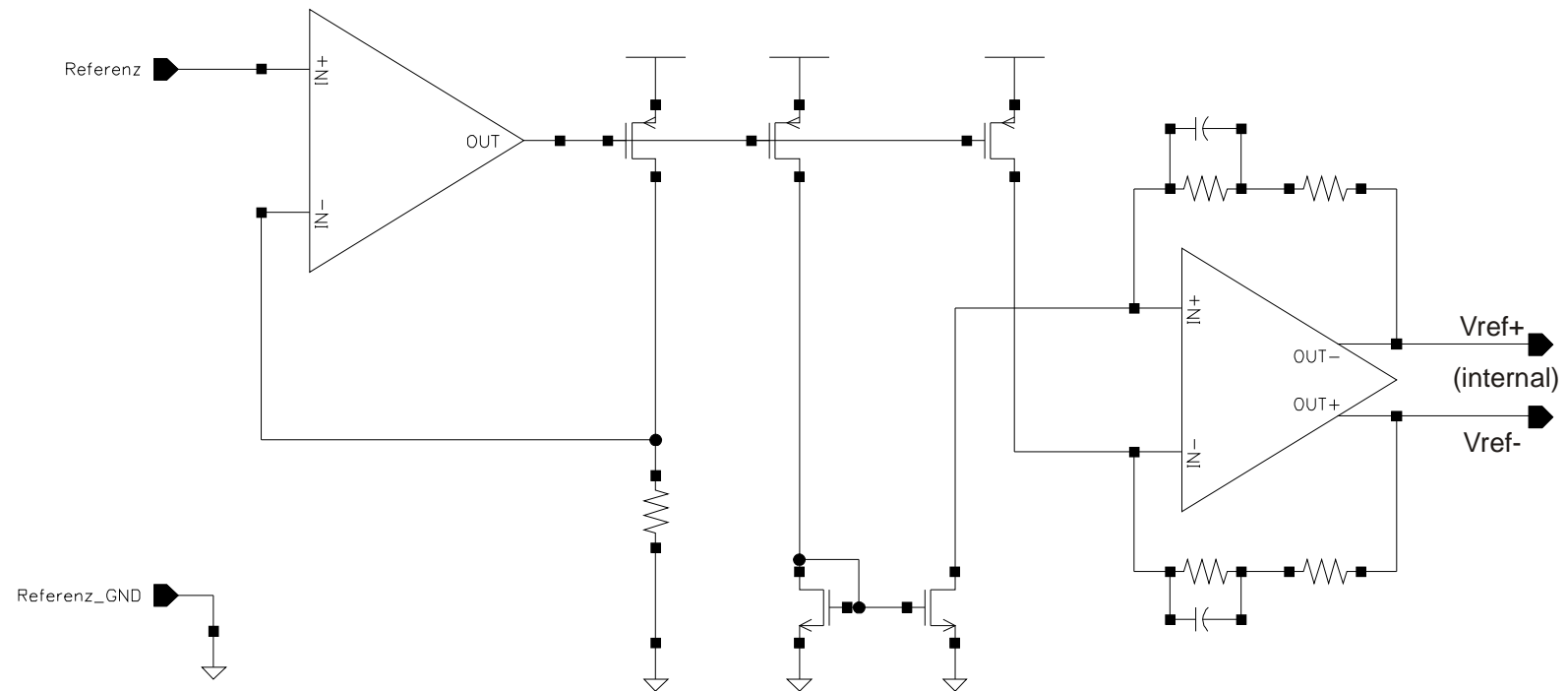
4.95mm



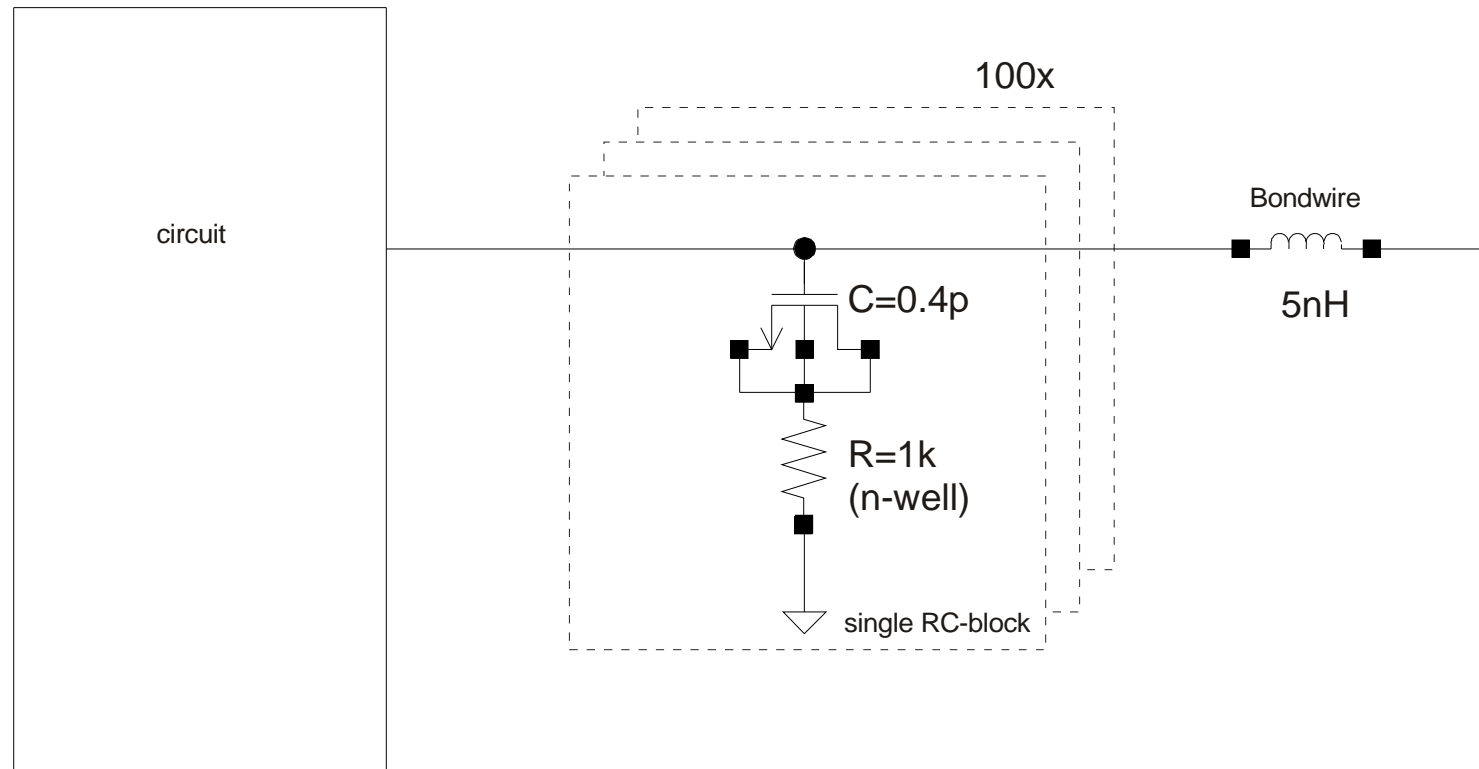
each ADC will have it's own power pads

- improved layout of the capacitor array to cancel the influence of the parasitic differential capacitance: more space between capacitors and grounded shields between all critical plates and wires.

- redesign of the internal reference voltage generation, employing only differential circuits and RC-filtered reference voltages.

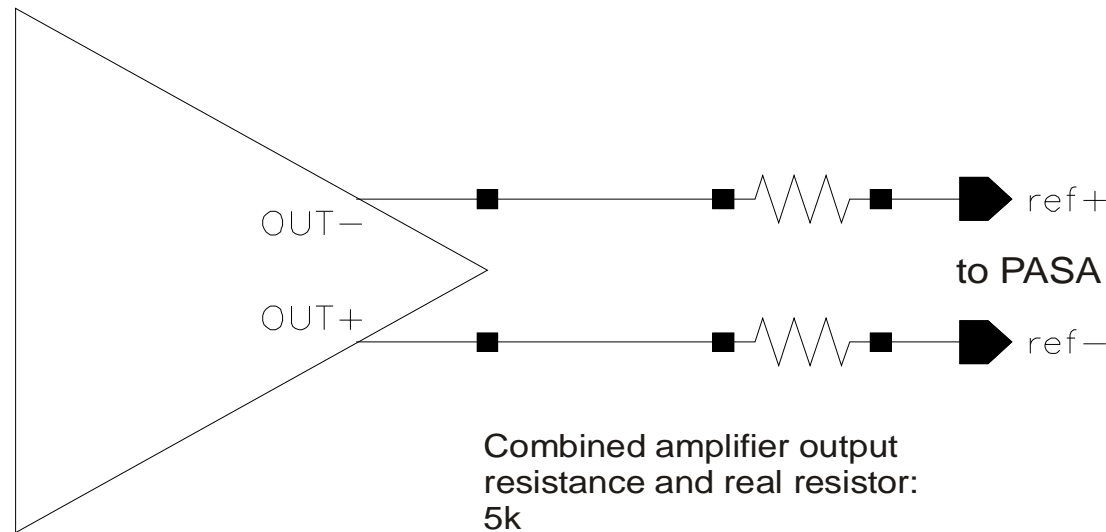


- more decoupling capacitors on chip, using cells of MOS-capacitors with some resistance to limit current in case of oxide breakdown



Parallel connection of single RC-blocks leads to $40pF$ and 10Ω . In case of breakdown of a single MOS-capacitor the current is limited to $1.8mA$.

- configurable bias currents for the amplifiers of the ADC, adjustment range $\sim \pm 50\%$ to compensate for variations of the integrated current source and to allow a reduced power consumption in idle periods (in fact most of the time) without completely turning off the ADCs. 3Bit (Power...) will control the current.
- configurable Autozero operation of the ADCs. Autozero is additional sampling of the own offset voltage, introducing additional $\frac{KT}{C}$ -noise. Two modes of operation will be possible: Autozero at every new sample (normal) and Autozero at specific points in time (only once before measurement-period of 2us). AZ_AUTO controls the operation.
- a possibility to test the ADCs already on wafer with some pins connected. Sampling of own reference voltage, producing full scale code and shorted inputs, producing code 0, allow a first separation of damaged devices.
- changes concerning the interfaces: Vref+ and Vref- will have a defined output resistance of 5kOhm. Beside from well defining the gain of the preamplifier this forms a low-pass-filter together with the input capacitance of the pre-amp of 100pF.



- concerning the digital interface: the data-out will be shifted in order not to disturb the sampling of the new data:

