

The slide features a red header with the Cadence logo. The background is a blue-tinted image of a circuit board with glowing points of light. The title 'UltraSim' is in large white font, followed by a subtitle in smaller white font. The speakers' names and the date are listed at the bottom in a small black font.

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**UltraSim**  
**The complete SoC Transistor-level  
Sign-off solution for Timing, Noise,  
Power and Reliability**

Robert Esterl & Robert Schweiger  
Custom IC  
Cadence Design Systems

June 10, 2003

**UltraSim The complete SoC Transistor-level Sign-off solution for Timing, Noise, Power and Reliability**

Are you using an accelerated SPICE simulator?

Polls are closed.

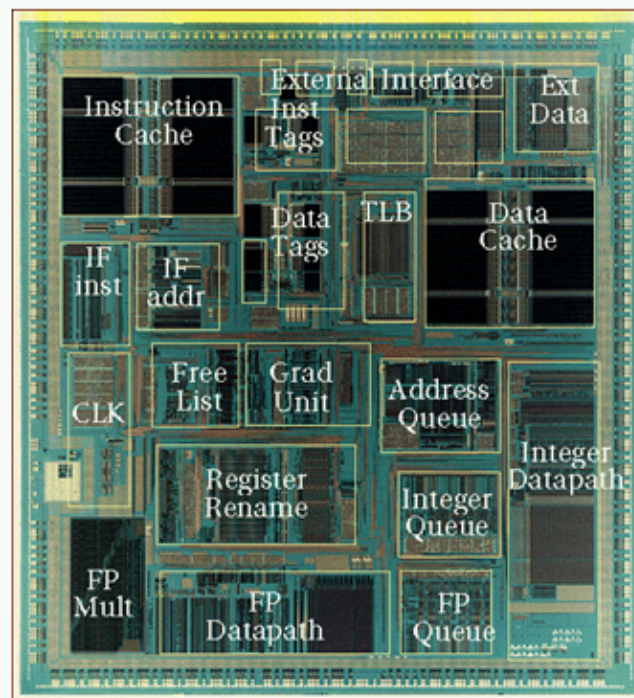
yes



no



**[ Poll A ]**



## UltraSim

The Complete  
SoC Transistor  
Level Sign-off  
Solution for  
Timing, Noise,  
Power and  
Reliability

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Slide 2

## Why Use a Fast Spice Simulator?

- **Historical reasons** ✓
  - Capacity limitations of SPICE (pre/post layout)
  - Reduction in simulation time
- **Mixed signal simulation**
  - Digital designs w/ some analog
  - Analog designs w/ some digital
  - Accuracy of A/D, D/A interfaces
  - Missing behavioral models (VerilogA/MS)
- **Rapid prototyping** ✓
  - Accuracy is close, but not perfect,
    - But neither are the device models
  - Shorten design cycle ✓

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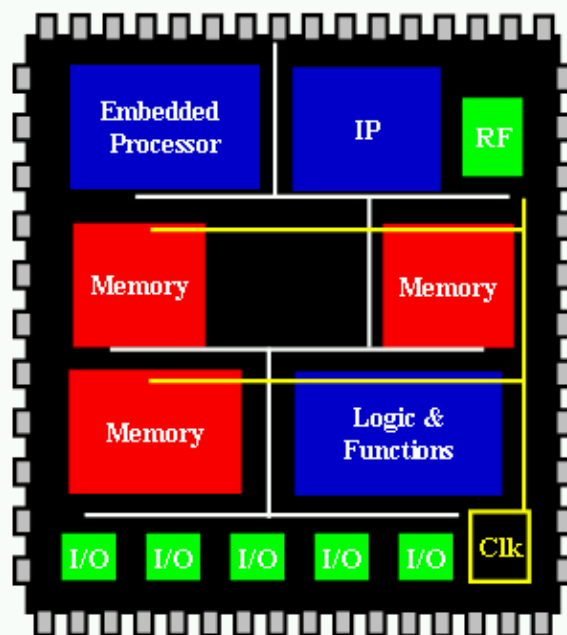
## Why Use a Fast Spice Simulator?

## Where Does Fast Spice Fit?

- **Large digital**
  - Verilog / VHDL is not accurate enough.
- **Memories**
  - Too large to simulate in SPICE
- **Mixed signal (PLL's, ADC's, DAC's)**
  - Too slow in SPICE due to digital portion
- **System on Chip (SoC)**
  - No other way without behavior models

Where Does Fast Spice Fit?

## Mixed Signal SoC Verification



- Predominantly digital
- Digital simulation
- Some A / MS blocks
- Analog simulation of individual blocks
- Full chip simulation is difficult, but necessary

## Mixed Signal SoC Verification

## UltraSim: The Full Chip Simulation Solution

*Hierarchical full-chip transistor-level simulator*

- **Memory, digital & mixed-signal applications**
  - Single pass power, timing, noise & reliability
- **Ultra-high capacity**
  - 10M+ transistor flat
  - 1B++ transistor hierarchical
  - Ideally suited for SoC's and memories
- **Ultra-accurate**
  - SPICE-like (within 1-3%) – timing, pwr, volt.
- **Ultra-high performance (vs SPICE)**
  - 10x to 1,000x faster for flat netlists
  - 1,000x or more for hierarchical netlists
- **Integrations with AMS Designer and ADE**

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**UltraSim: The Full Chip Simulation Solution**

## Complete Set of Analyses

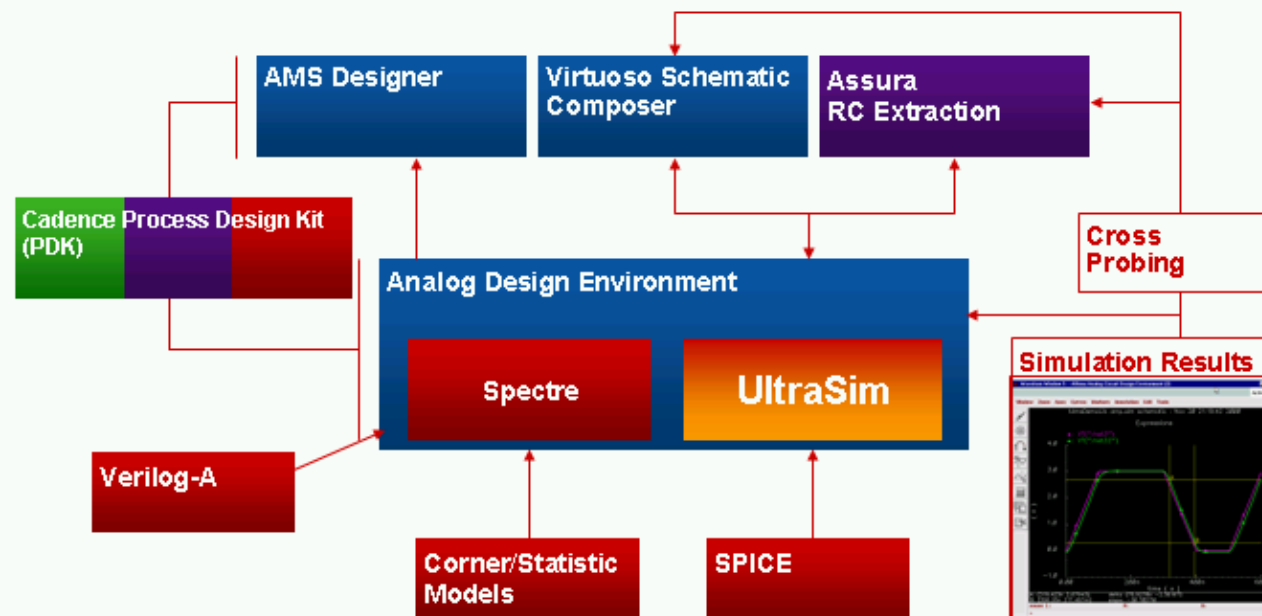
- **Reliability analysis**
  - Only fast simulator that supports (HCI,NBTI)
  - Critical at 130nm and below
- **Timing analysis**
- **Noise analysis including cross coupling**
  - Overshoot & undershoot (Both C and L)
- **Power analysis**
  - Element & subcircuit level power
  - IR drop (integration w/ VoltageStorm)

## Complete Set of Analyses



## Analog Integrated Circuit (IC) Design Solution

### The World's Most Widely Used Solution

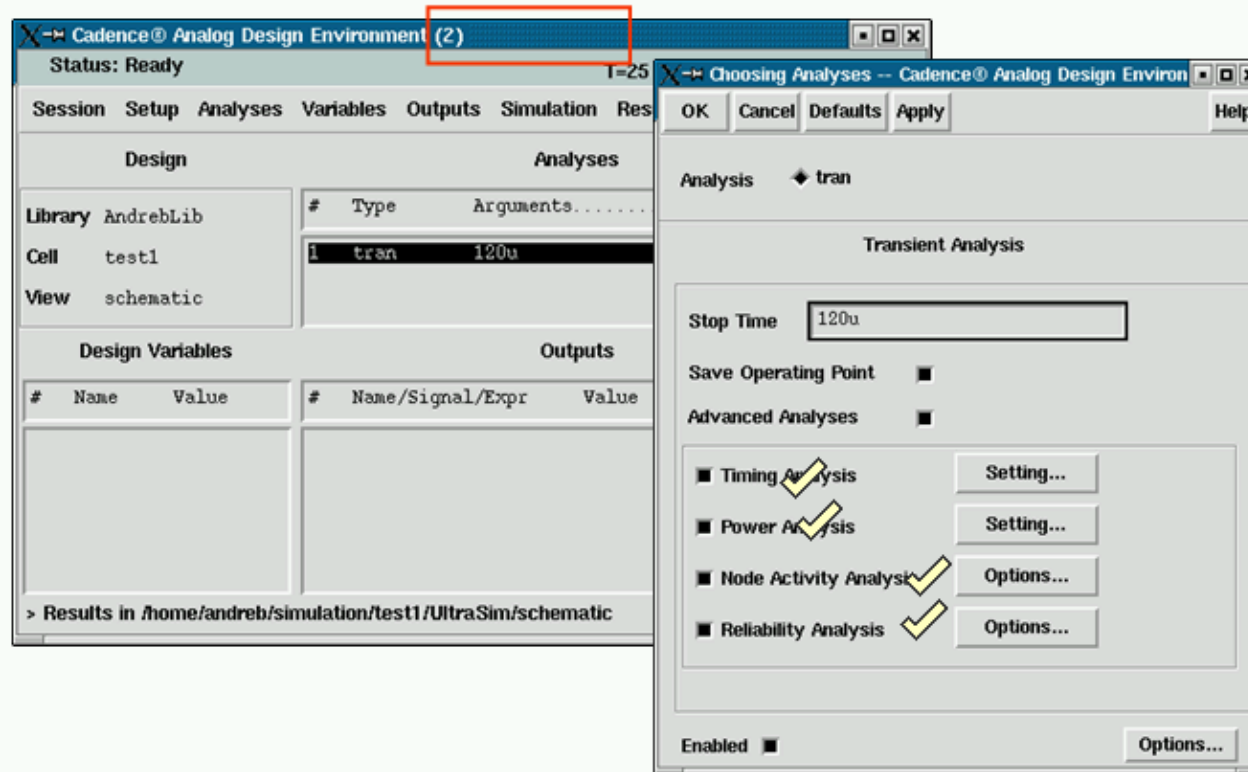


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Slide 8

## UltraSim inside Analog Design Environment (ADE)

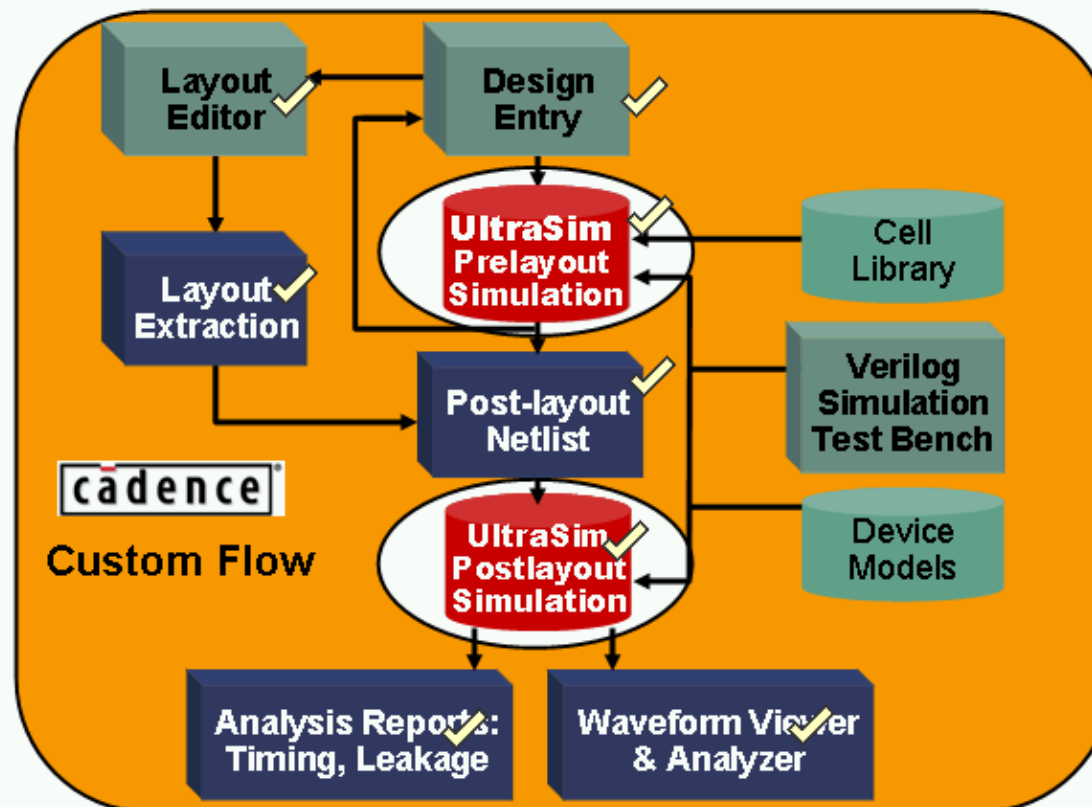


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### UltraSim inside Analog Design Environment (ADE)

## UltraSim in the Custom IC Flow



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## UltraSim in the Custom IC Flow

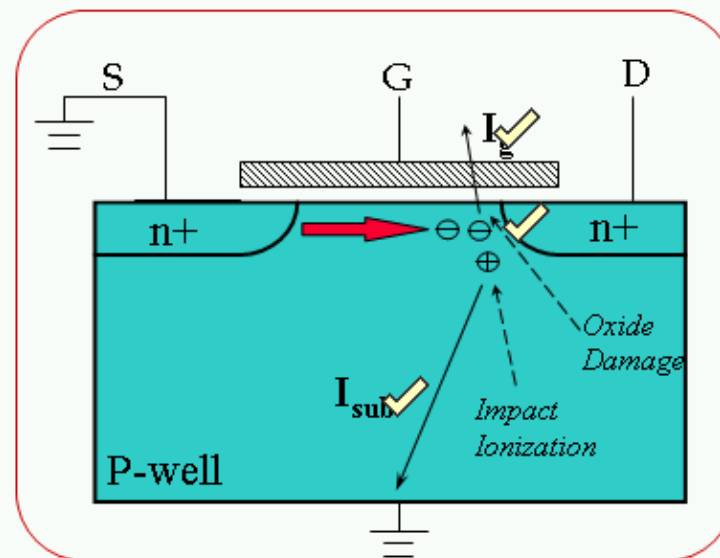
## Reliability: A Growing Concern

- **HCI and NBTI severely impact design**
  - Wasted performance with excessive guard bands
  - Yield reduction due to immediate failures
- **Must be addressed with design solutions** ✓
- **The only reliability commercial solutions** ✓
  - Cadence offers complete suite of services & tools ✓
  - Device, interconnect, sub-circuit, block to full-chip ✓
  - Experienced team with over 8 years of proven reliability solutions ✓

## Reliability: A Growing Concern

## Hot Carrier Effects

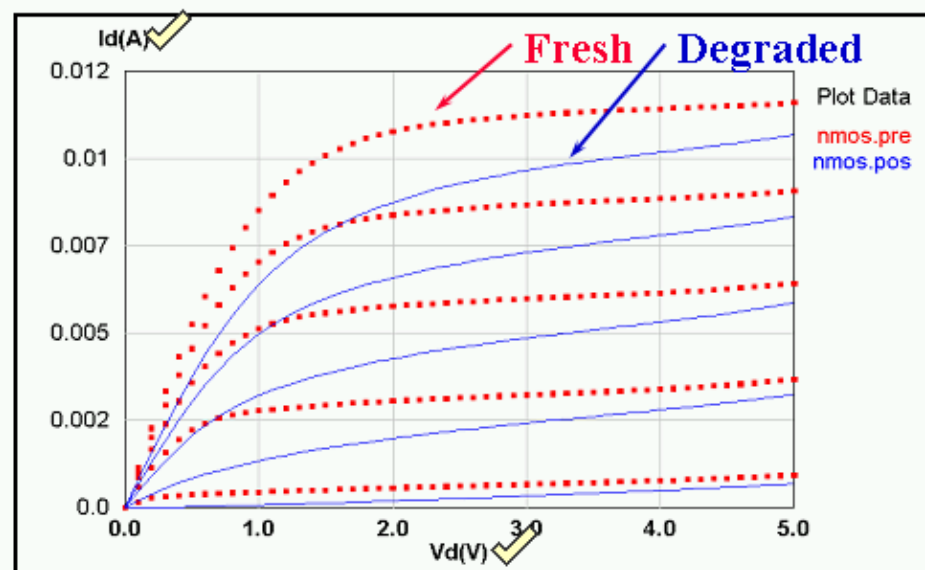
- $E_{\max}$  at drain corner causes hot carrier generation
- Hot carriers cause  $I_{\text{sub}}$ ,  $I_{\text{gate}}$  and oxide damages



## Hot Carrier Effects

## Hot Carrier Effects

- Current driving capability degradation
  - Causes longer time delay
  - “Degraded” also sometimes called “aged”



## Hot Carrier Effects

## 0.13 $\mu$ m CMOS Crisis = NBTI

- “Reliability problems scale up as CMOS scales down”

- By David Lammers, EE Times

- April 12, 2002 (on-line at EETimes.com)

- April 14, 2002 (EETimes print edition cover story)

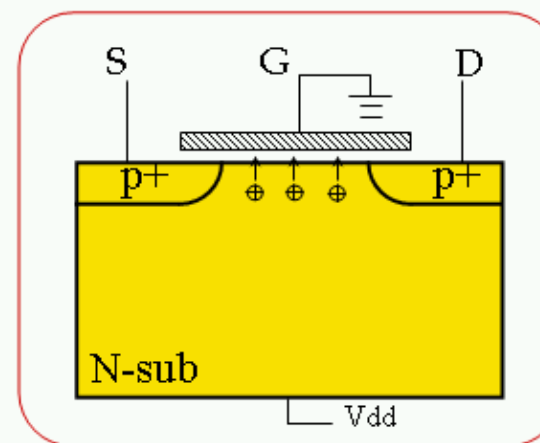
- **NBTI = Negative Bias Temperature Instability**

- Degrades performance & yield of PMOS devices ✓

- Critical @  $t_{ox} < 50$  angstroms ✓

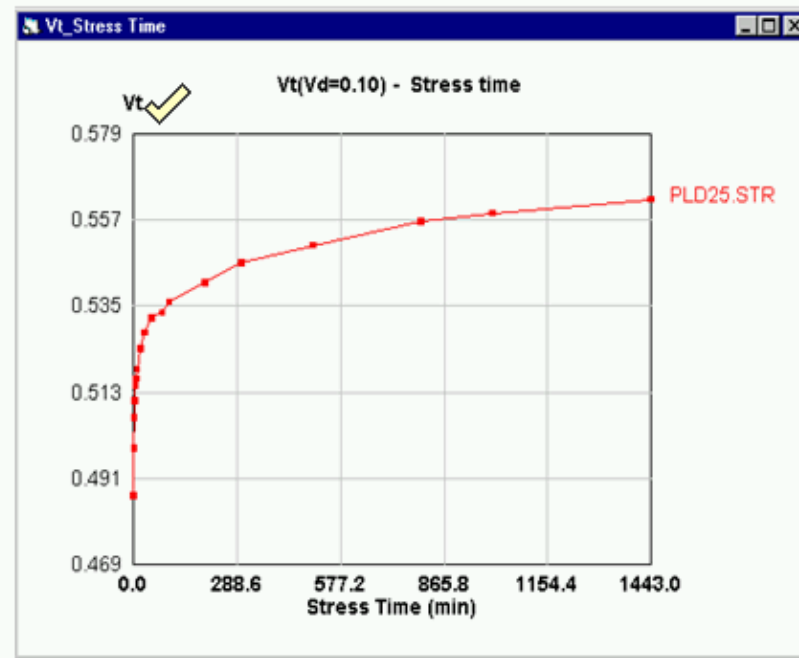
- Results in immediate failures ✓

- Reduces performance ✓



0.13 $\mu$ m CMOS Crisis = NBTI

## Degraded Vt



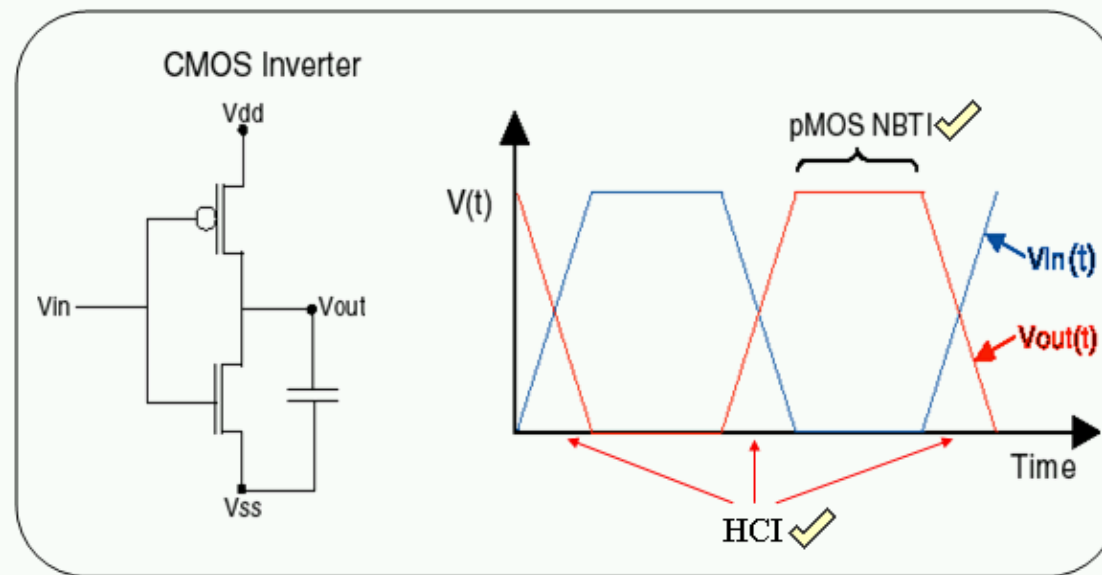
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## Degraded Vt

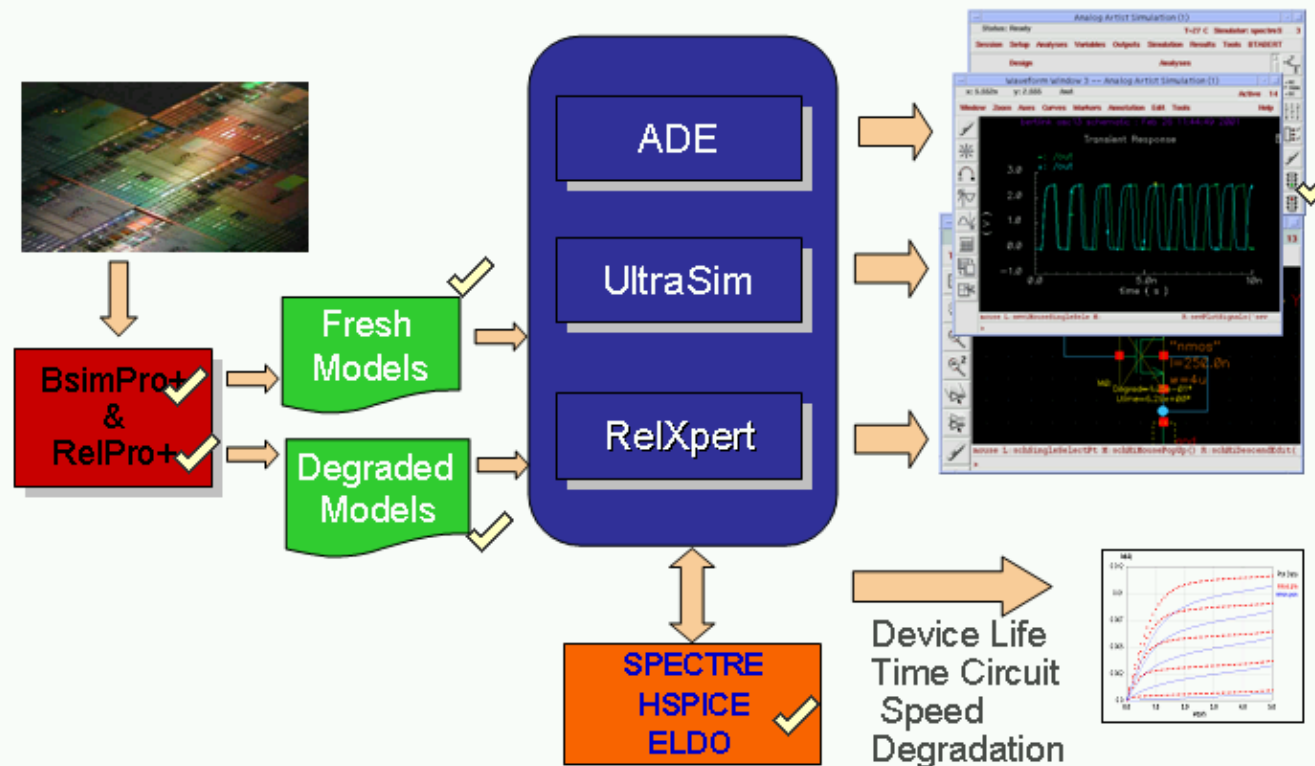


## HCI & NBTI Effects in Circuit Operation



## HCI & NBTI Effects in Circuit Operation

## Reliability Modeling Flow

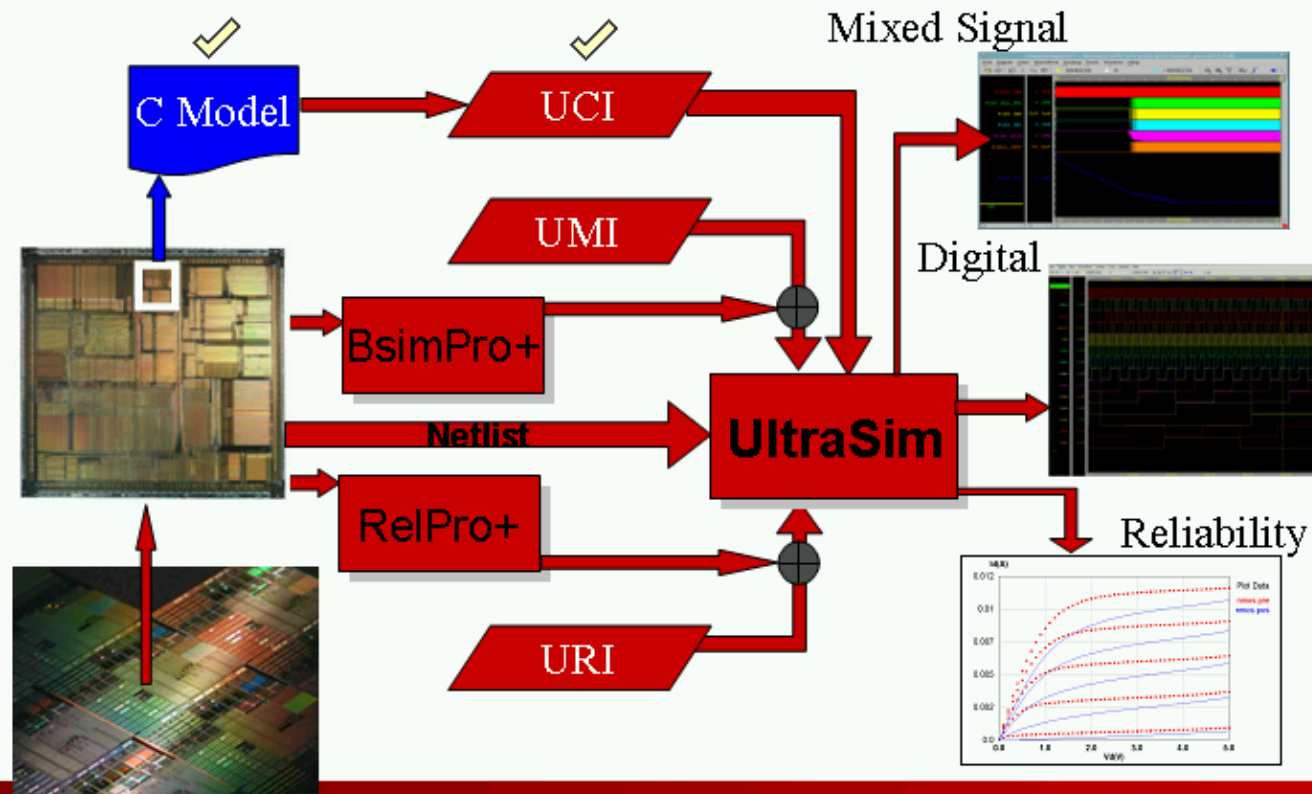


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## Reliability Modeling Flow

## UltraSim Model/C Interfaces

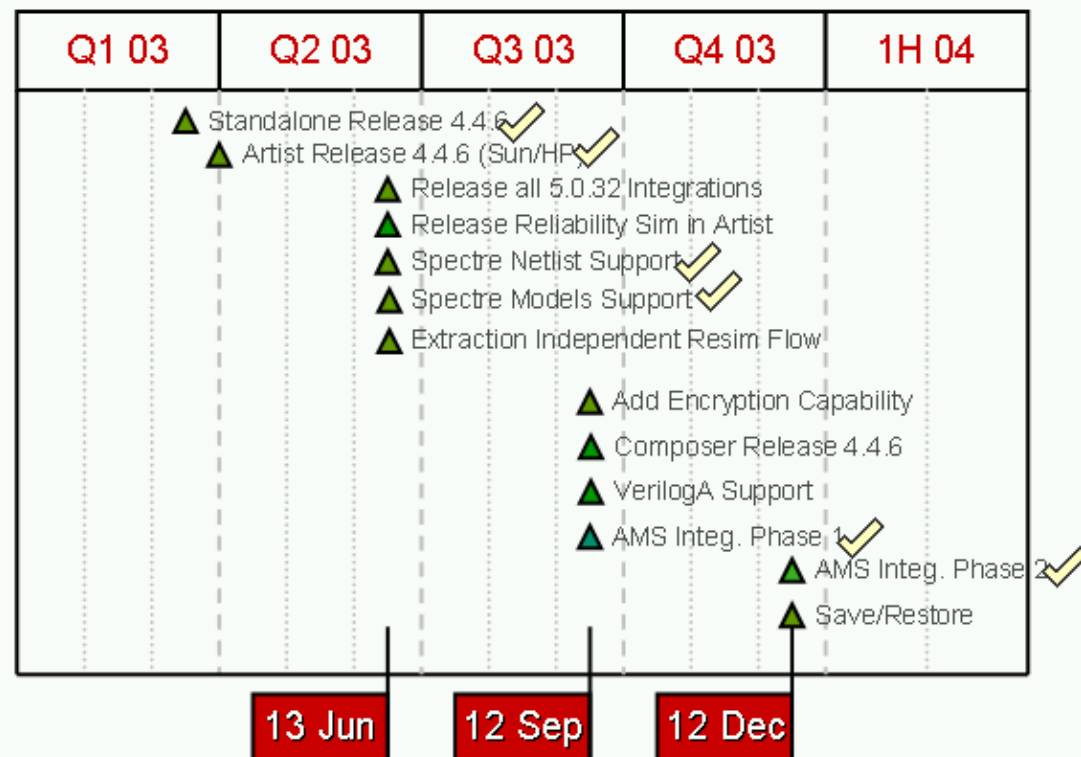


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## UltraSim Model/C Interfaces

## UltraSim Roadmap



## UltraSim Roadmap

## UltraSim Case Studies

- **Mixed Signal Simulation**

- PLL
- Multiplier
- ADC / DAC
- Voltage Regulator

- **Digital Simulation**

- Memory
- Clock Mesh

## UltraSim Case Studies

## UltraSim Simulation Modes Overview

Simulation Mode	df (default) <digital fast mode>	da <digital accurate mode>	ms <mixed signal mode>	a <analog mode>	s <spice mode>	Option
<b>MOSFET</b>	<b>Digital Model</b>		<b>Analog Model</b>		<b>SPICE</b>	
Current / Charge Model	df	da	a		s	mos_methode
Diff. Junct.	df	da	a		-	mosd_methode
DIODE	df	da	a		s	diode_methode
BJT	s					
Accuracy	1 2 3	1 2 3	1 2 3	1 2 3	1 2 3	acc
Default Accuracy (Tol.)	1 (0.01)	2 (0.001)	2 (0.001)	2 (0.001)	2 (0.001)	acc (tol)
	acc=1 -> Relative Tolerance tol=0.01, acc=2 -> tol=0.001, acc=3 -> tol=0.0001					
Netlist Hierarchy	Autodetect (1)				Flat (0)	hier
Partitioning	Digital			Analog	None	
Target Error	< 10%	< 5%	< 1%	< 1%	< 1%	
Application	Functional Verification of Digital Circuits / Memories	Timing Verification of Digital Circuits and Memories, some PLL's, some AMS Designs	PLL's, AMS Designs, special Memories	DAC, ADC, DC/DC, Volt. Refs. Generators		

## UltraSim Simulation Modes Overview

## UltraSim Post-Layout Options

postl	0 (default) ✓	1	2	3	4
RC reduction	no	yes	yes	yes	yes
rcr_fmax (GHz)	1.0	1.0	1.0	1.0	1.0
rshort ( $\Omega$ ) ✓	1.0E-6	1.0E-3	0.1	1	100
rvshort ( $\Omega$ ) ✓	1.0E-6	1.0E-3	0.1	1	100
cgnd (F) ✓	1.0E-20	1.0E-16	1.0E-16	1.0E-15	1.0E-14
cgndr ✓	0	0.01	0.1	0.1	0.3

## UltraSim Post-Layout Options

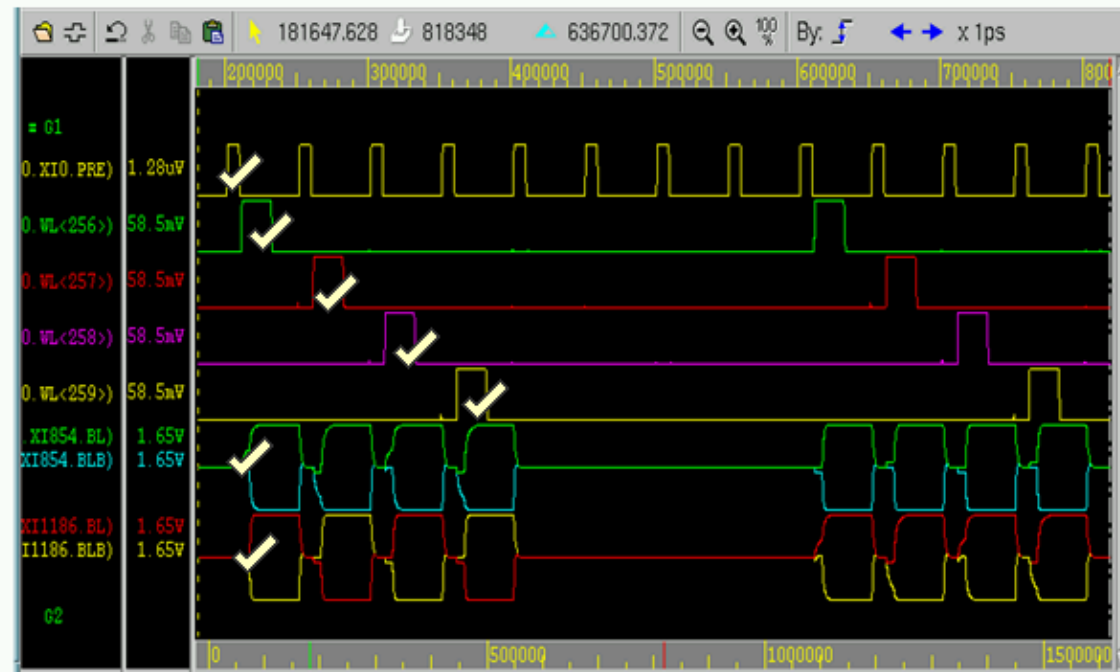
## UltraSim: 3<sup>rd</sup> Generation Technology

- **256K-bit DRAM**
  - 308,408 mosfets
  - CPU = 575sec ✓
- **16M-bit DRAM**
  - 19,738,112 mosfets
  - CPU = 607sec ✓
- **1G-bit DRAM**
  - 1,263,239,168 mosfets
  - CPU = 759sec ✓
- **UltraSim performance metric**
  - Fast simulation benchmark
- **Machine:**
  - Solaris2.6, 400MHz CPU
- **Number of vectors:**
  - 4 write cycles, 4 read cycles

## UltraSim: 3rd Generation Technology



## 1Gb DRAM Simulation Waveform



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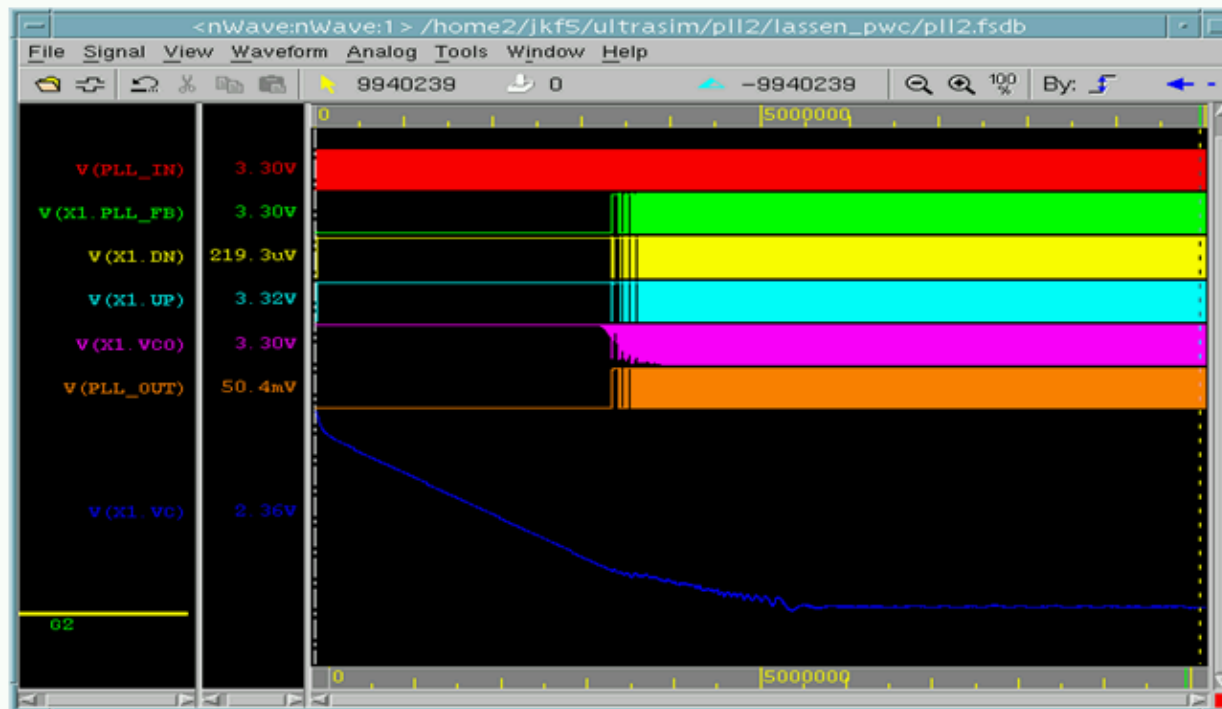
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## 1Gb DRAM Simulation Waveform

## UltraSim: Ultra-fast and Ultra-accurate

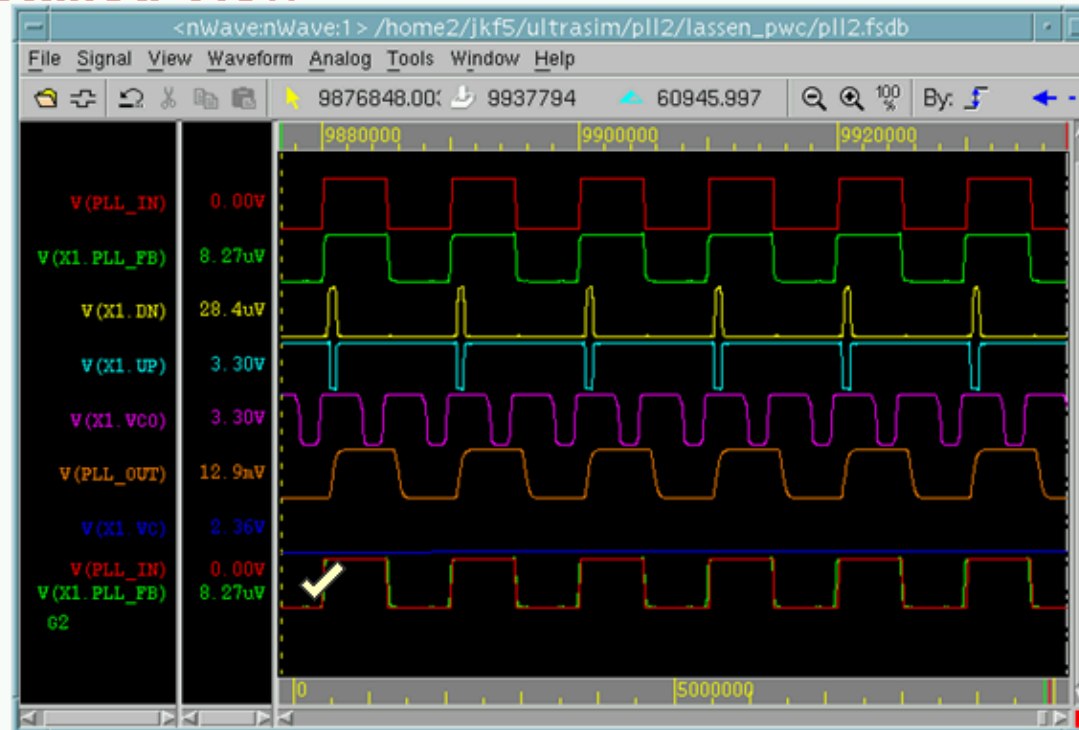
- Retains precision even in “fast” mode

## PLL Simulation Waveform - Full View



## PLL Simulation Waveform - Full View

## PLL Simulation Waveform – Detailed View



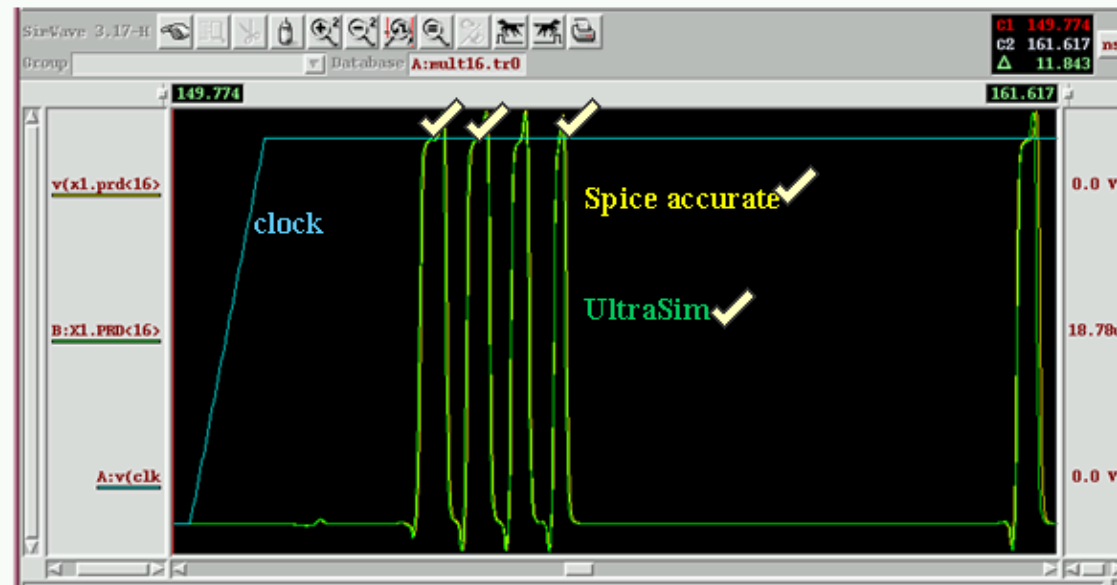
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## PLL Simulation Waveform ? Detailed View

## UltraSim: Accuracy Is Key

- Spice & UltraSim overlaid for a 16bit Multiplier



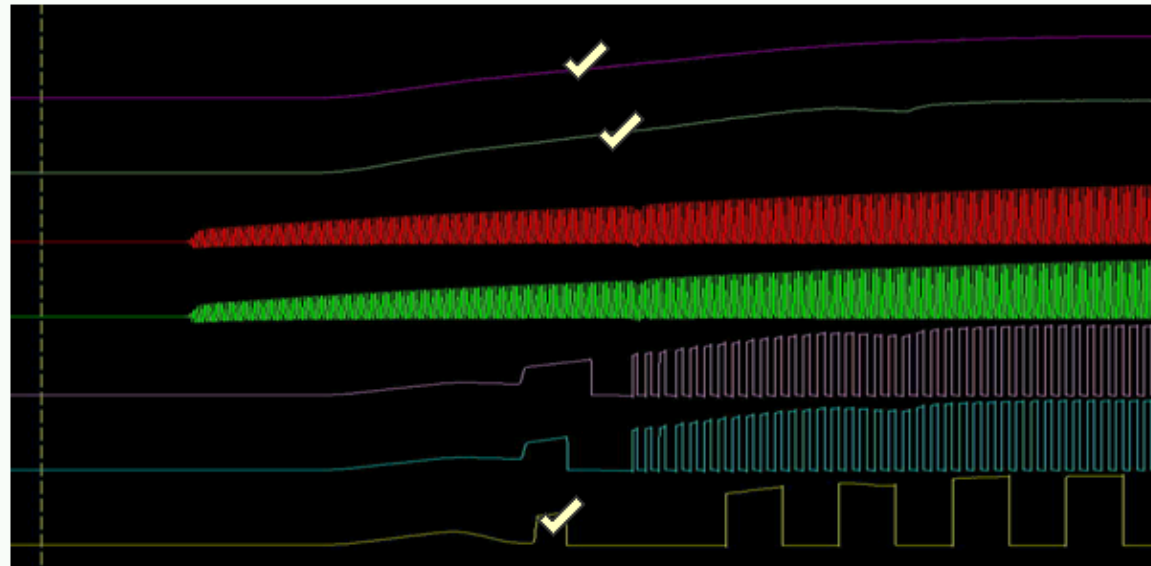
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## UltraSim: Accuracy Is Key

## Mixed-Signal – Voltage Regulator

- Startup Sequence for Analog Portion



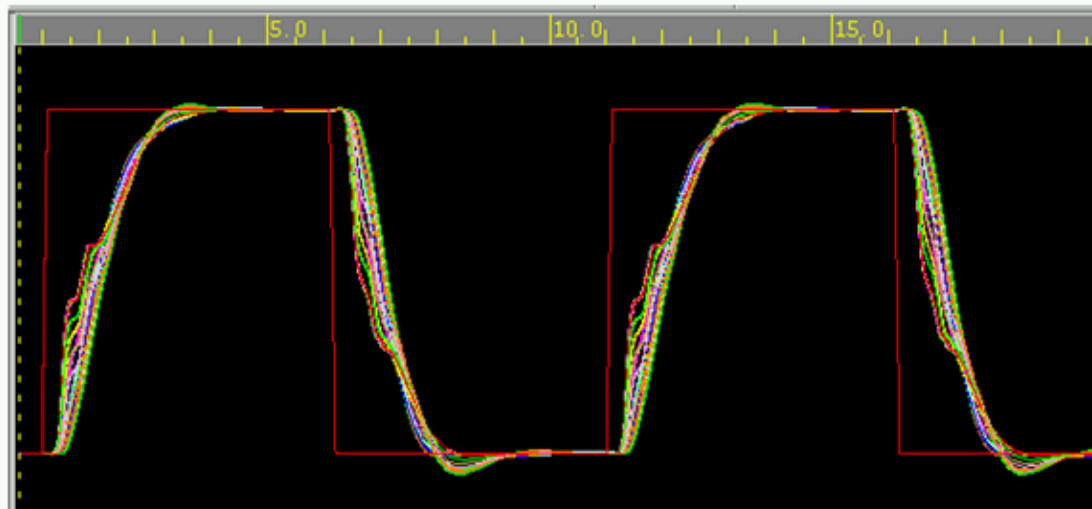
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Mixed-Signal ? Voltage Regulator

## Analysis of Clock Mesh

- Coupling induced noise
  - Capacitive and inductive effects

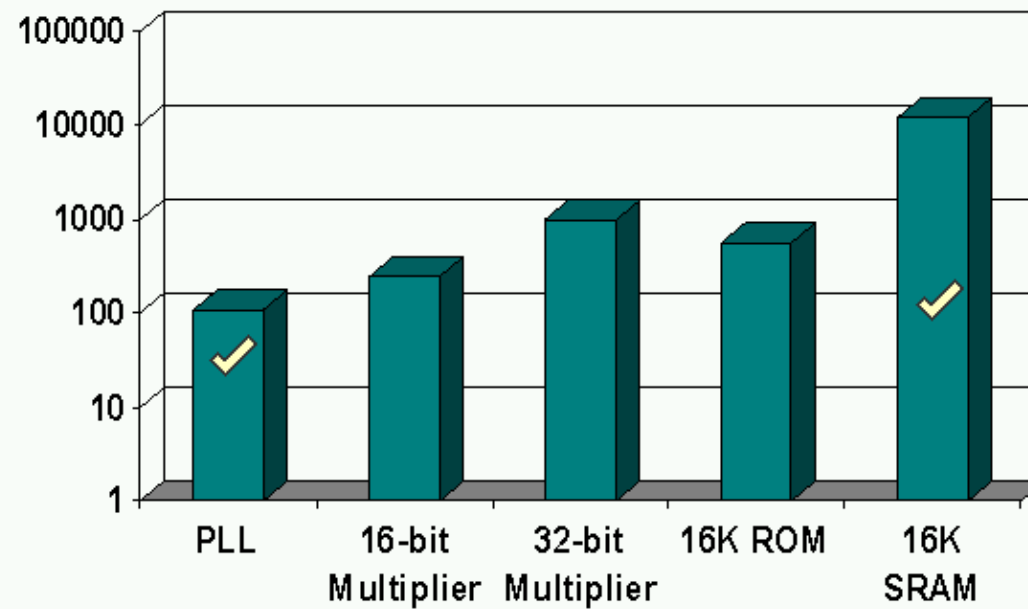


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## Analysis of Clock Mesh

## UltraSim Speed Vs. SPICE



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UltraSim Speed Vs. SPICE



## Success Stories - Details

Category	Type	# Devices	TRAN Time	Memory Usage	CPU Time
Memories ✓	8M S.RAM ✓	25.8M	400ns	110M	96s
	S.RAM	50M		443M	1357s
	S.RAM (postlayout)	1.1M, 1.1M C	12ns	500M	500s
	S.RAM	3.8M	614us	62M	9h
	DRAM ✓	74k	380ns	385M	545s
	256M DRAM	283M	350n	208M	160s
	256M DRAM	586M	500ns	820M	2h 46min
Digital Circuits ✓	Flash Memory	35k	2.2us	103M	19 min
	Digital Design ✓	174k	6ms	213M	7h 35min
	Joystick	15k	22.5m	20M	3.57h
	MCU	45k, 16.8k C	1ms		1.2h
	CLK Tree	15k, 87k C, 71k R	20n	1.5G	25min
	clock mesh ✓	226k, 62k c, 62k r, 60k l	50n	189 MB	40min
	Switch -Capacitor Circuit	271	1ms	19.7M	22min
Mixed-Signal Circuits ✓	PLL ✓	3.1k	8us	14.7M	44min
	Mixed Signal	712	30us	4.4M	142s
	Mixed-Signal Transceiver	25k	200us	137M	7h
	BICMOS Mixed-Signal	8k	10.1us	9M	75 min
	Mouse Controller (MS)	49K, 57k R, 38k C	50ms	137M	3h
S.OI ✓	Fire Wire ✓	500k, 30k Diodes, 2k C, 6k R	120u	700M	5 days
	RF ID	42k, 30k Diodes	100us	71M	3.5h
Analog Circuits ✓	Sigma Delta Converter	357	3ms	4M	2.22h
	Bandgap	112	5ms	7.5M	4s
	OpAmp ✓	78	100us	6.5M	4s
	Bandgap	119	3u	2MB	3s
	Bandpass	1078	1ms	27.5M	40min
	Booster	554	1ms	3.2M	20s
	DC-DC Converter	602	2.5ms	38M	22min
	ADC ✓	1.6k	6.5us	56M	98min
	ADC	5784	60.5us	60M	48 min

## Additional UltraSim Details

- **Supports industry standard models (partial list)**
  - BSIM3V3, GP, VBIC95 ✓
  - BSIMPD, BSIM4, Mextram, HICUM ✓
- **Other supported models**
  - Only fast simulator to support our High Voltage MOS model (HVMOS) ✓
- **Built-in hierarchical RC reduction feature**
  - Proven accuracy ✓
- **Cadence waveform viewer and hierarchical browser** ✓
- **SPICE, RelXpert, DSPF, SPEF, VCD & Vector Formats** ✓

## Additional UltraSim Details

## UltraSim Availability

- **Supported platforms**
  - SUN Solaris 6.0 or higher (32 or 64 bit)
  - HP-UX 11.0 or higher (32 or 64 bit)
  - Linux—Red Hat 7.2
- **Availability**
  - Last production release— April, 2003
  - Next production release— June 2003 ✓

## UltraSim Availability

## What Is the Value of UltraSim?

- **Ensuring timing closure**
- **Prediction of timing error due to interconnect**
- **Verification of SoC's**
  - Simulation capacity for large SoC's
  - Mixed level/mixed signal verification w/ NCsim
  - Unfinished blocks (C macromodel)
- **Mixing digital design with analog intellectual property (IP)**
  - Digital functional verification of mixed signal
- **Rapid prototyping (speed vs. accuracy)**
- **Improved yield**
  - Reducing margin stealing guardbanding
  - Avoiding reliability introduced failures

## What Is the Value of UltraSim?

## Why UltraSim?

- **Best capacity, accuracy and performance**
  - 3rd generation capacity ✓
  - SPICE-like accuracy
  - Orders of magnitude speed improvement
- **Wide range of applications**
  - Flat or hierarchical
  - Large digital, memory, SoC, mixed signal,...
  - Pre & post RC extraction with reduction
- **The Silicon Accurate Sign-off™ Solution**
  - Ensure timing, noise, power & reliability closure
- **Performance & time to market**

Why UltraSim?

Web Slide: [http://www.cadence-europe.com/web\\_seminars/feedback.cfm?feedback\\_form\\_id=15](http://www.cadence-europe.com/web_seminars/feedback.cfm?feedback_form_id=15)

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**Slide 37**