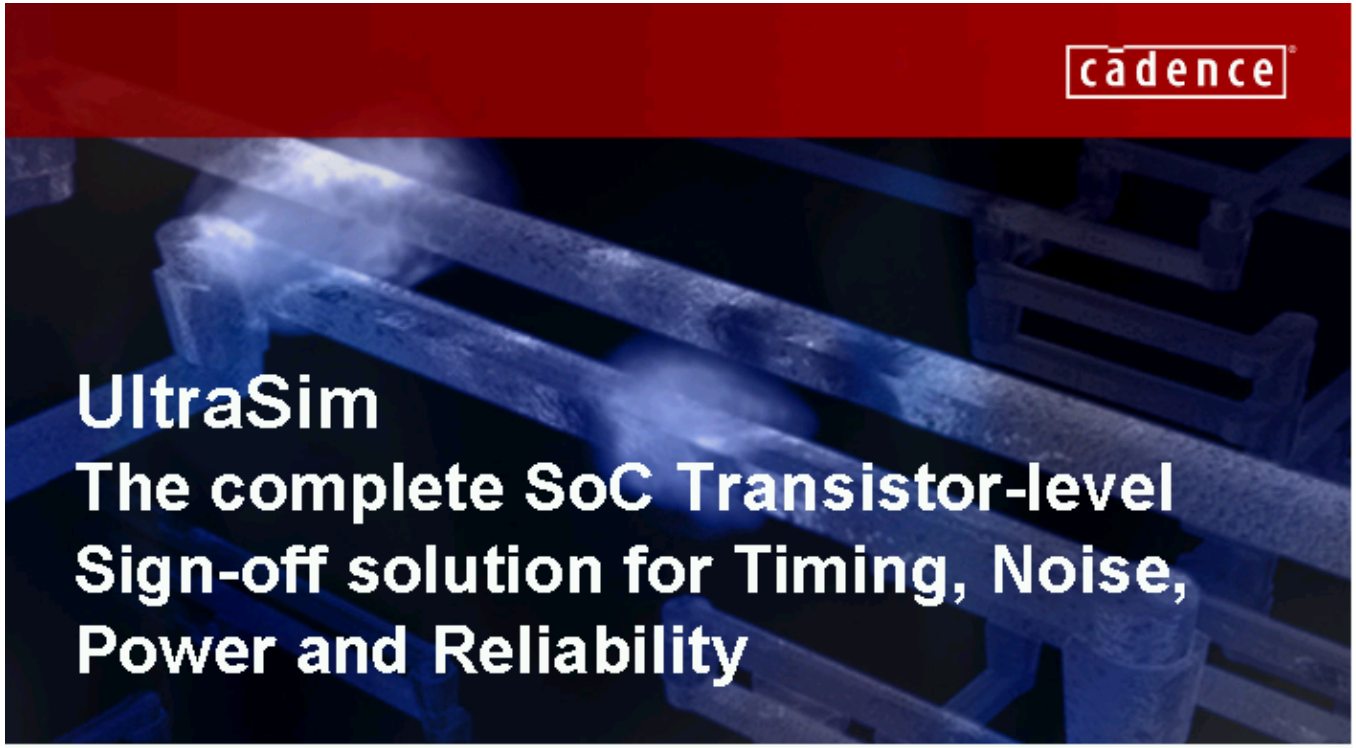
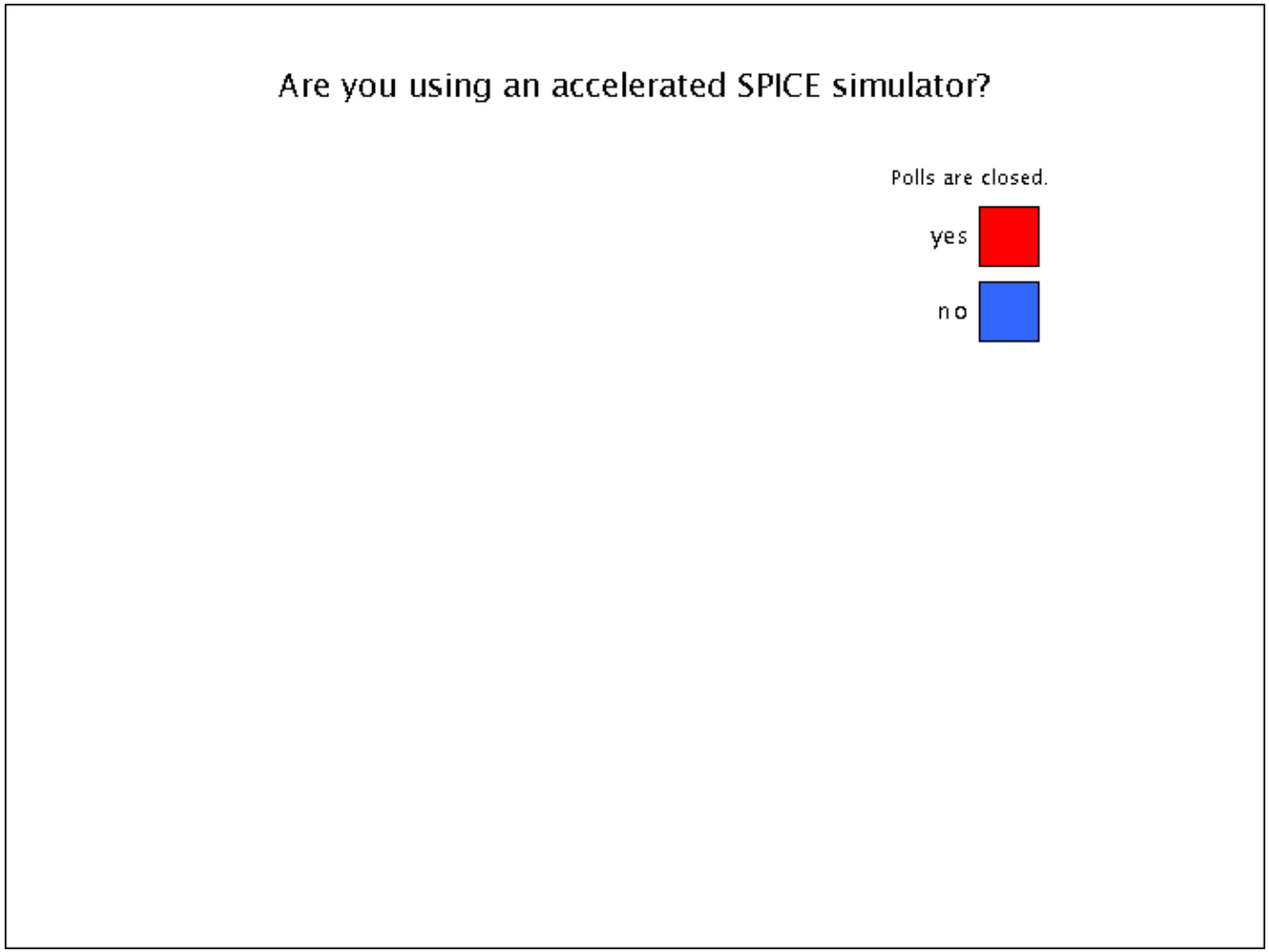
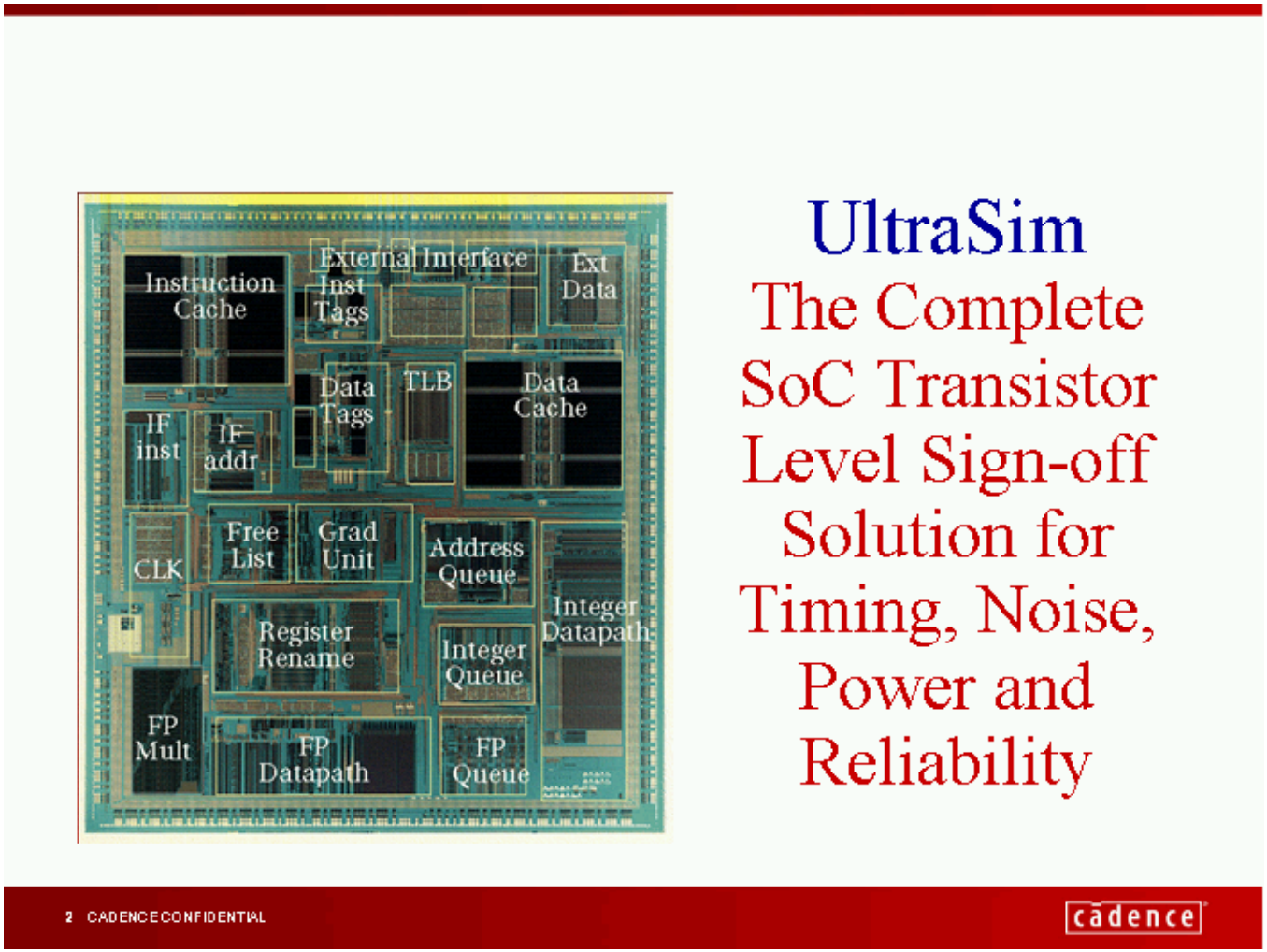


UltraSim The complete SoC Transistor-level Sign-off solution for Timing, Noise, Power and Reliability


Are you using an accelerated SPICE simulator?
Polls are closed.
yes
no

[Poll A]


Instruction Cache
External Inst Tags
Interface
Ext Data
Data Tags
TLB
Data Cache
IF inst
IF addr
CLK
Free List
Grad Unit
Address Queue
Integer Datapath
Register Rename
Integer Queue
FP Mult
FP Datapath
FP Queue
UltraSim
The Complete SoC Transistor Level Sign-off Solution for Timing, Noise, Power and Reliability
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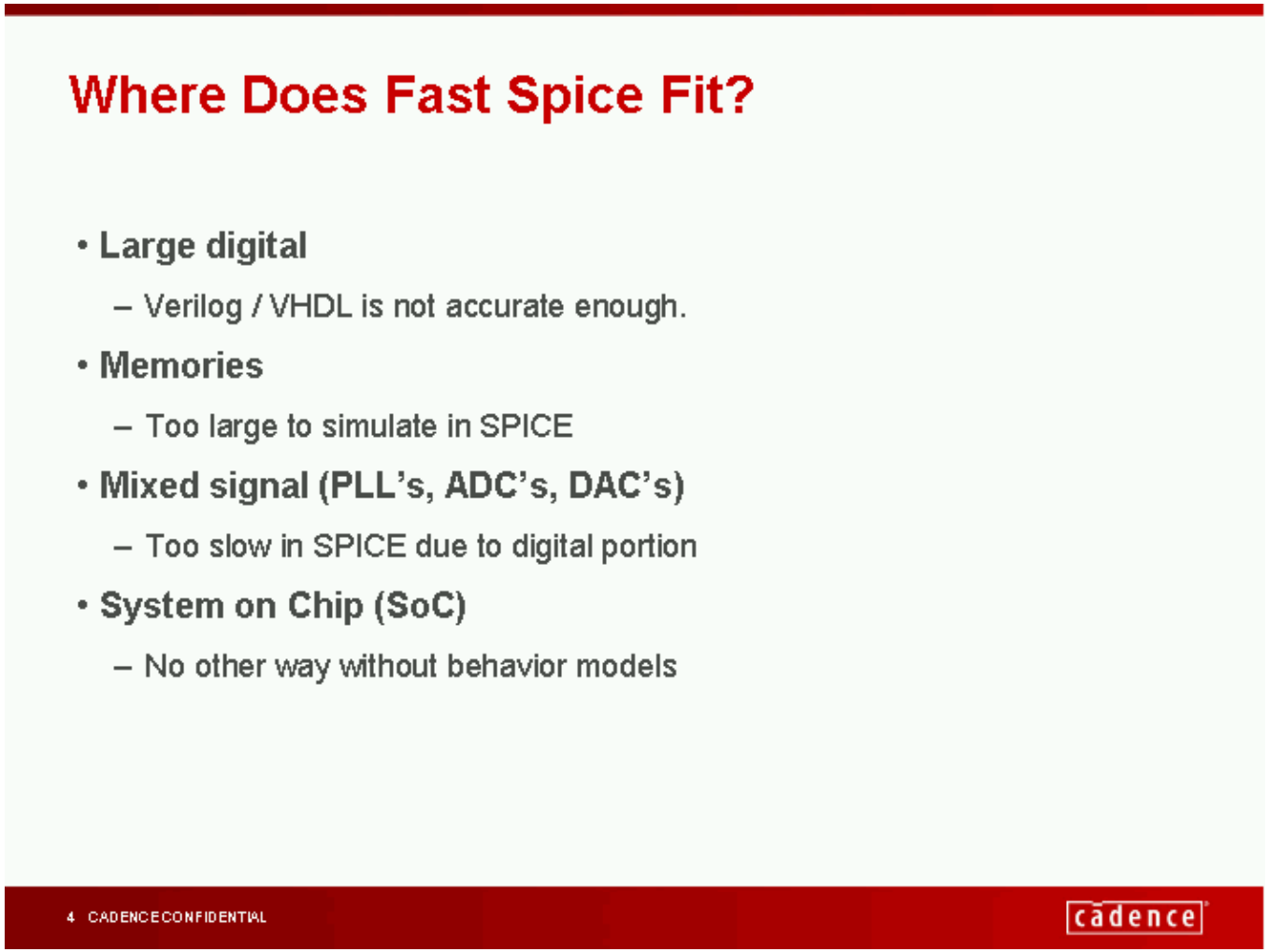
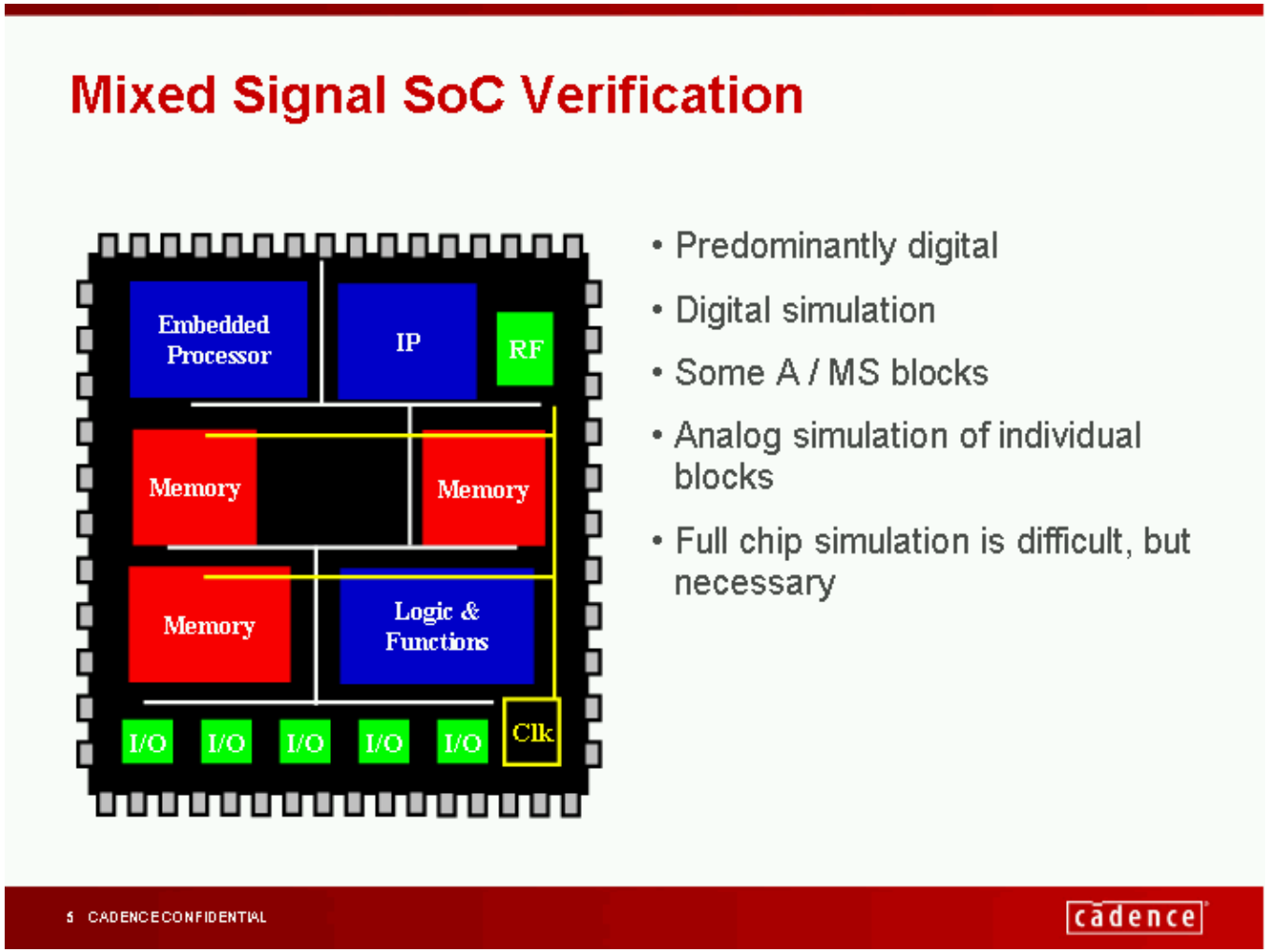
Slide 2

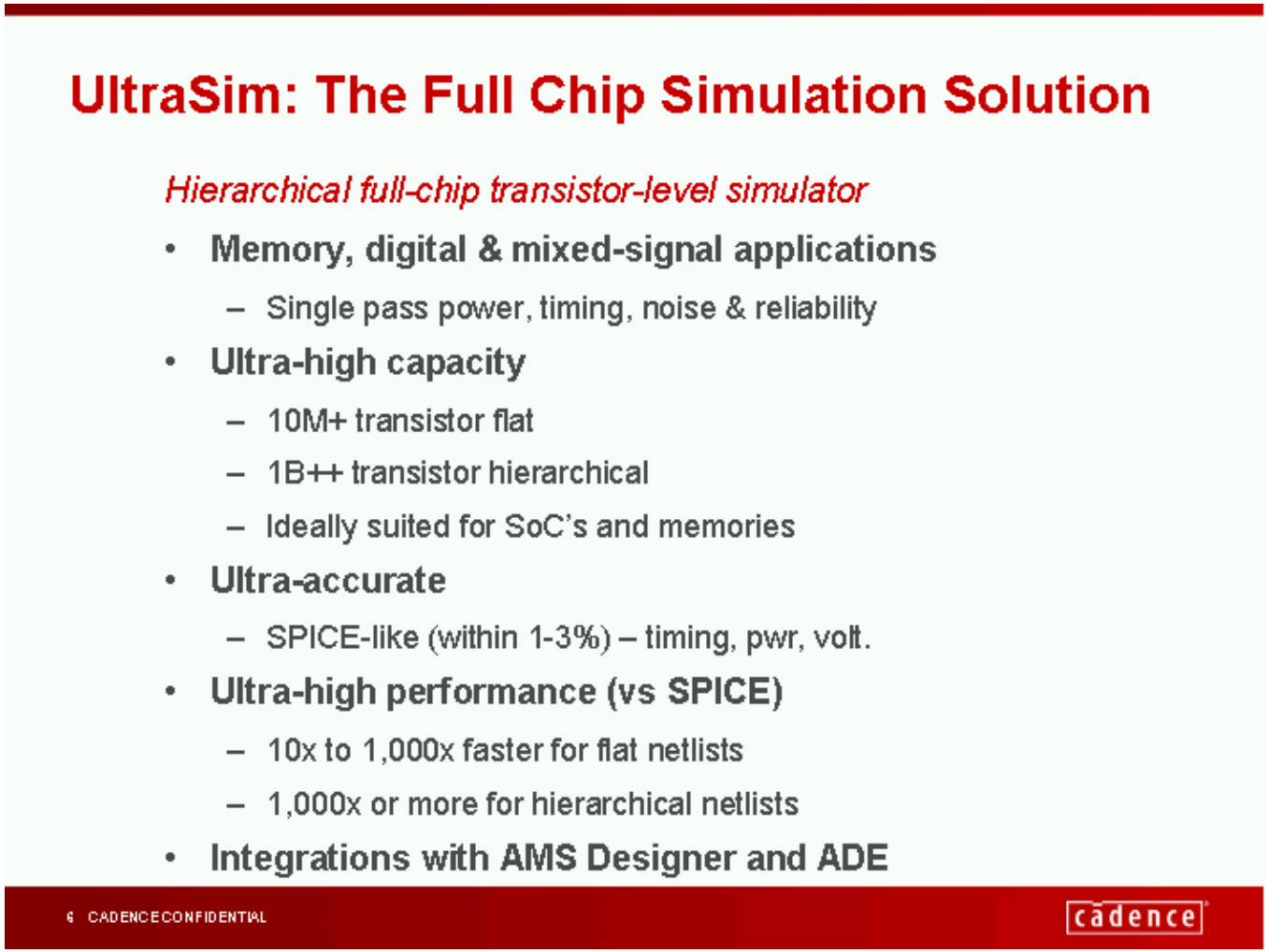
Why Use a Fast Spice Simulator?



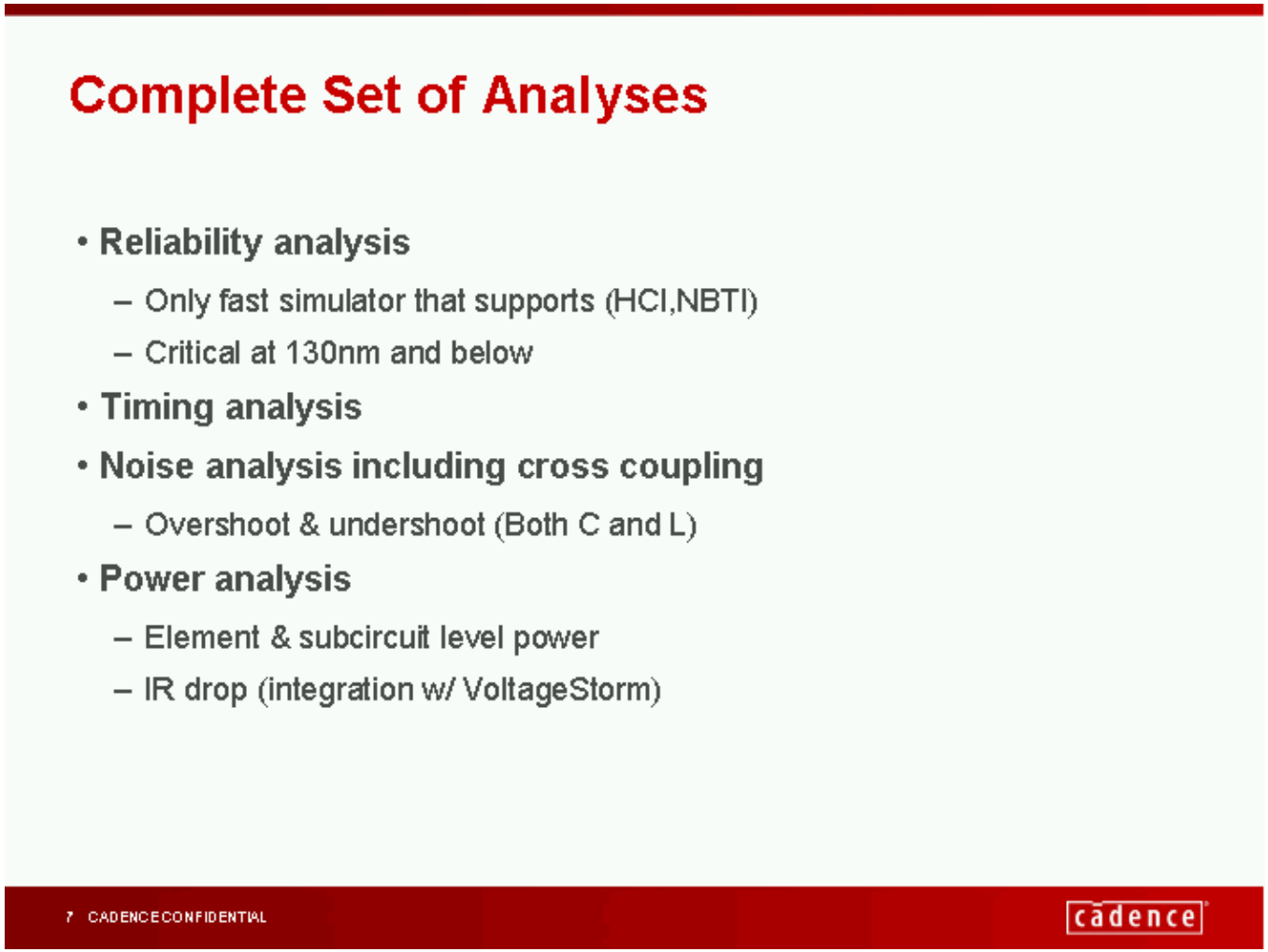
Where Does Fast Spice Fit?



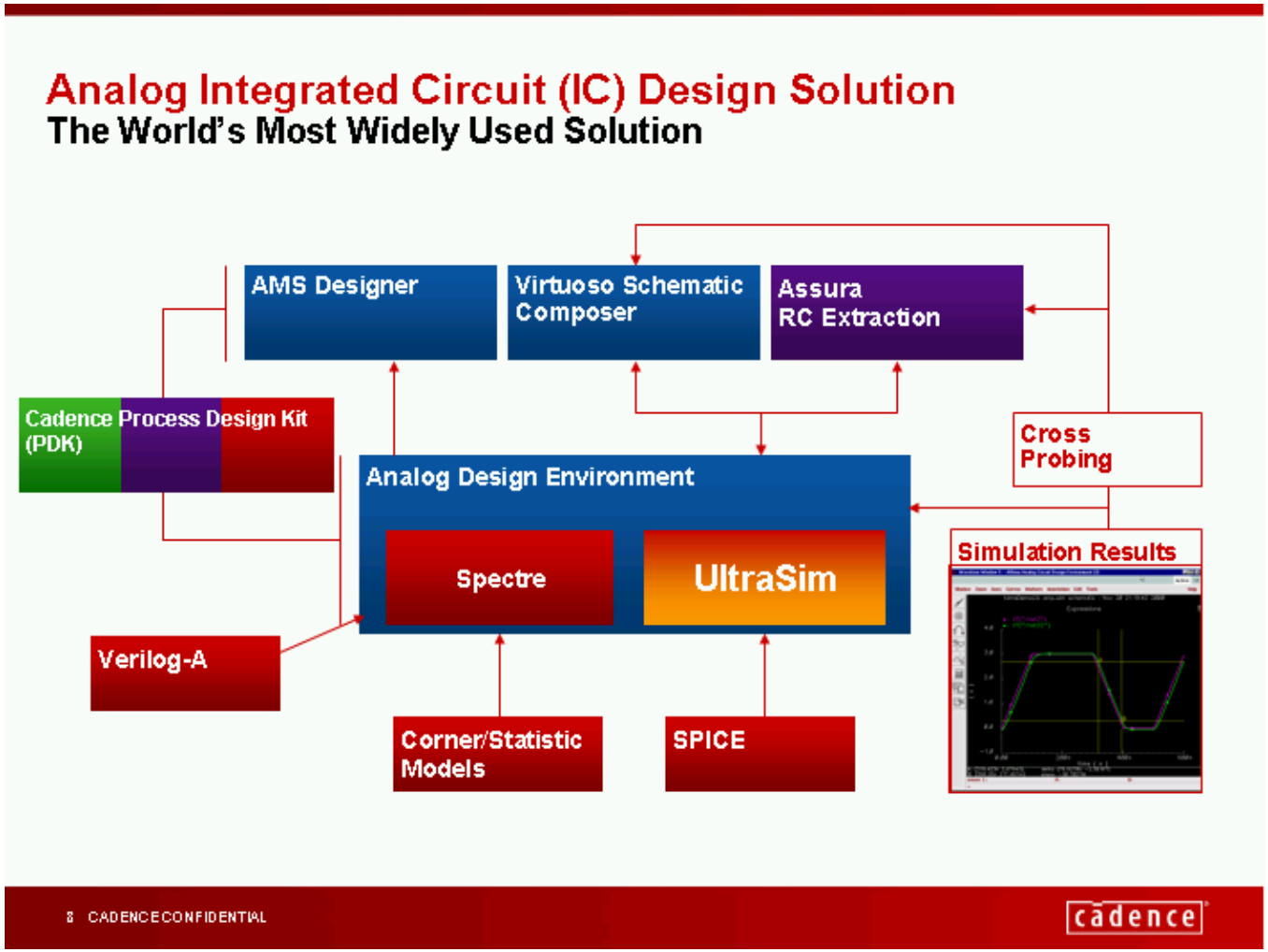
Mixed Signal SoC Verification



UltraSim: The Full Chip Simulation Solution



Complete Set of Analyses


Analog Integrated Circuit (IC) Design Solution
The World's Most Widely Used Solution
AMS Designer
Virtuoso Schematic Composer
Assura RC Extraction
Cadence Process Design Kit (PDK)
Cross Probing
Analog Design Environment
Spectre
UltraSim
Simulation Results
Verilog-A
Corner/Statistic Models
SPICE
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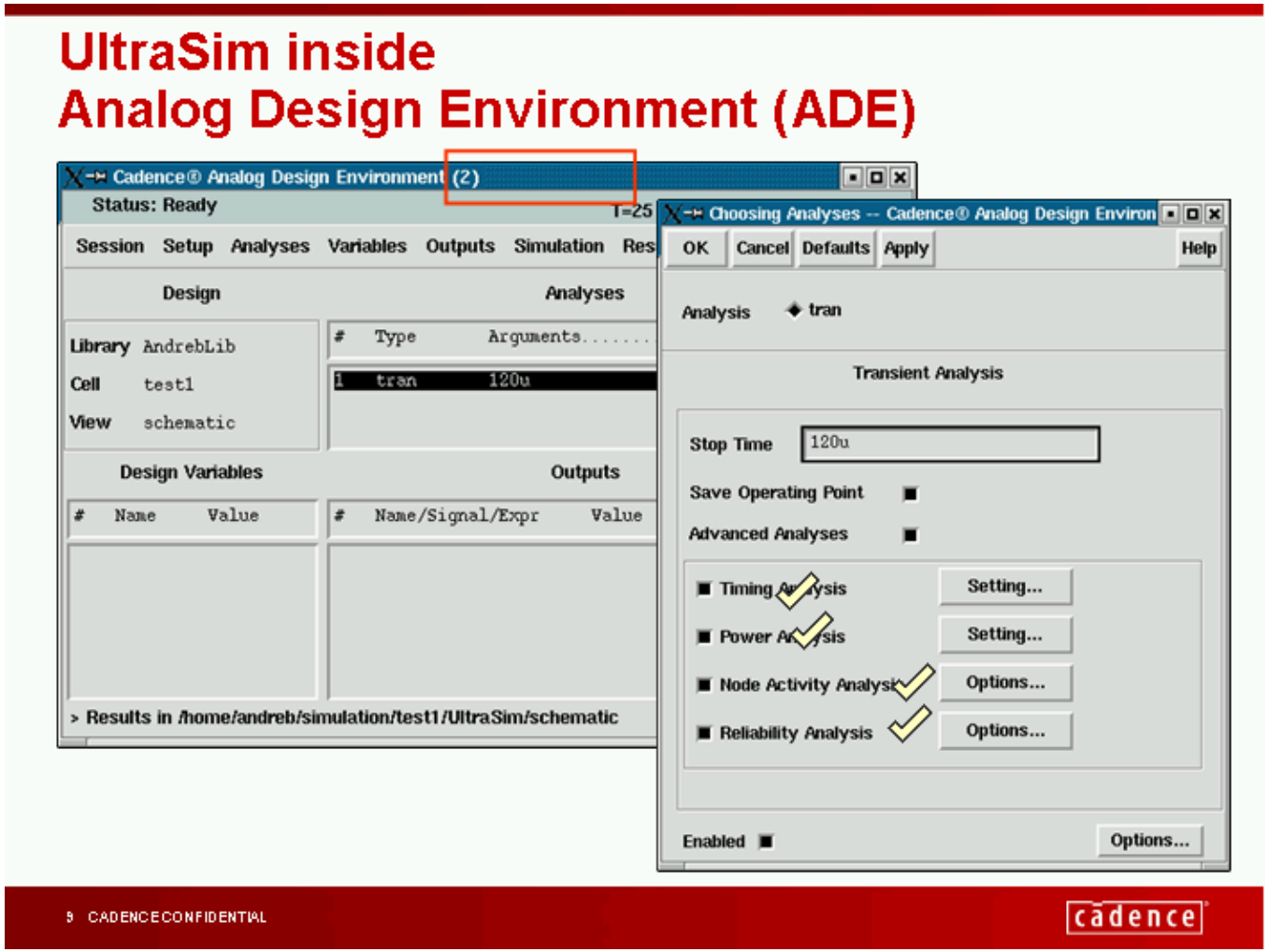
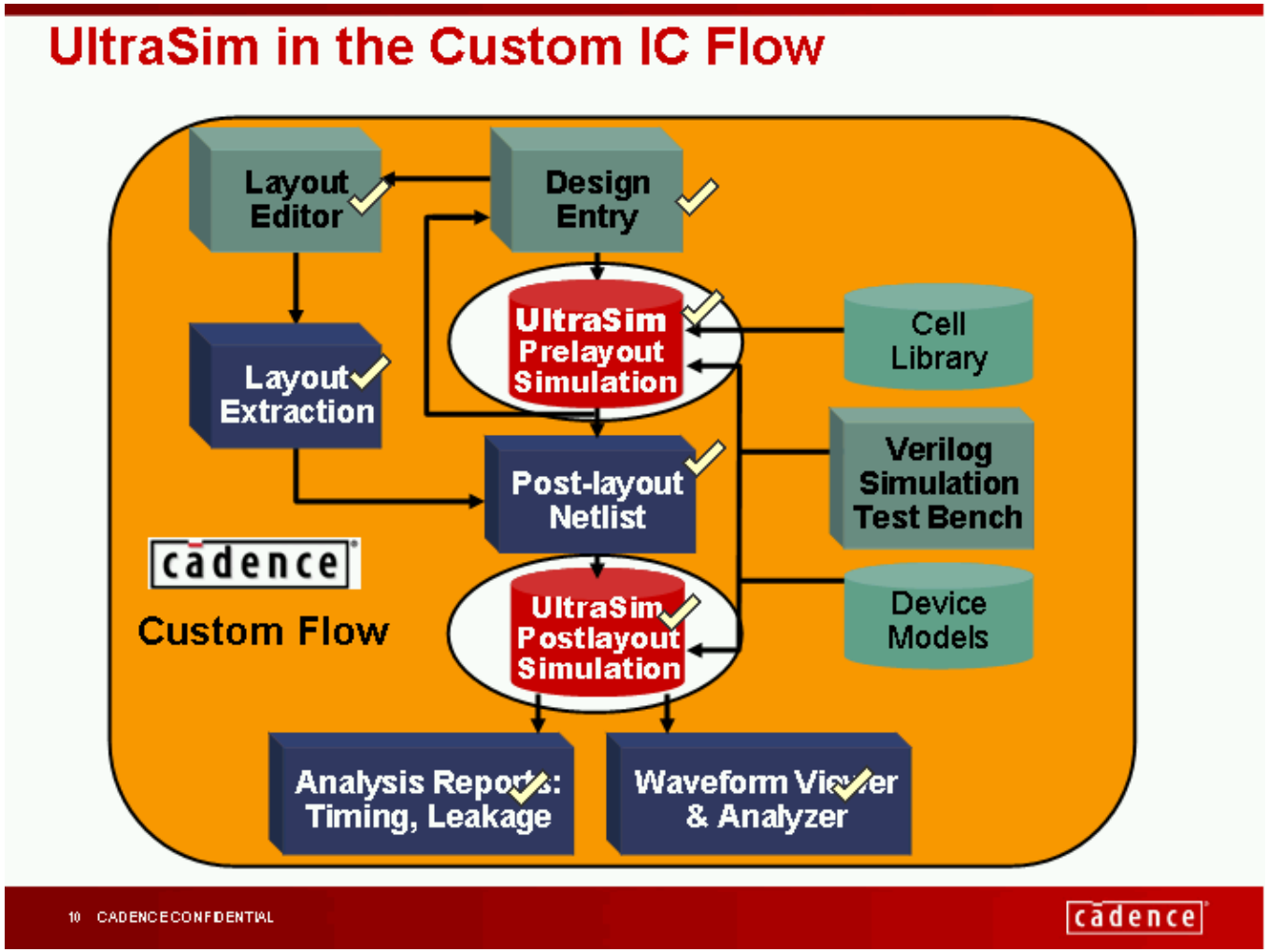
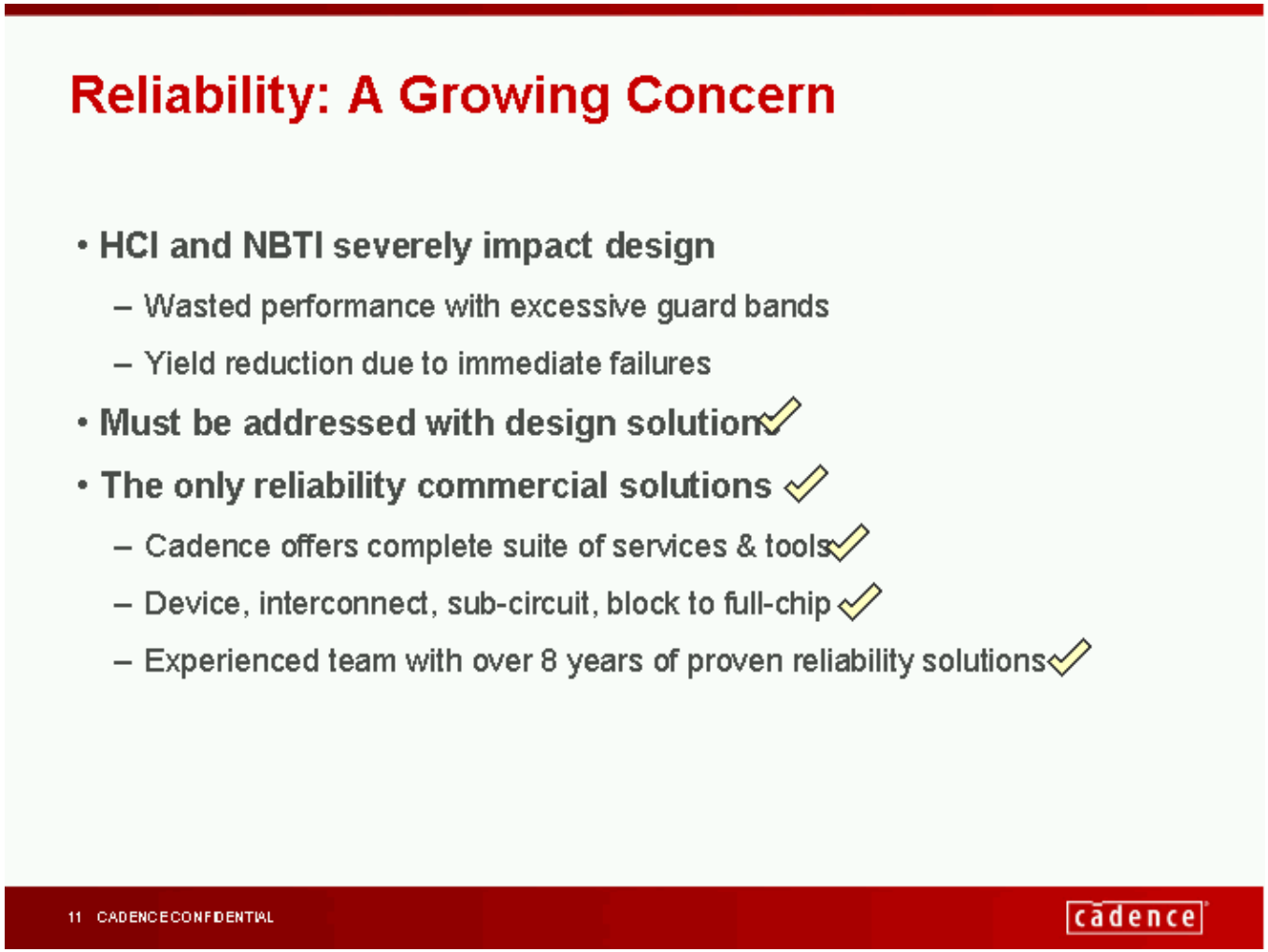
Slide 8



UltraSim inside Analog Design Environment (ADE)



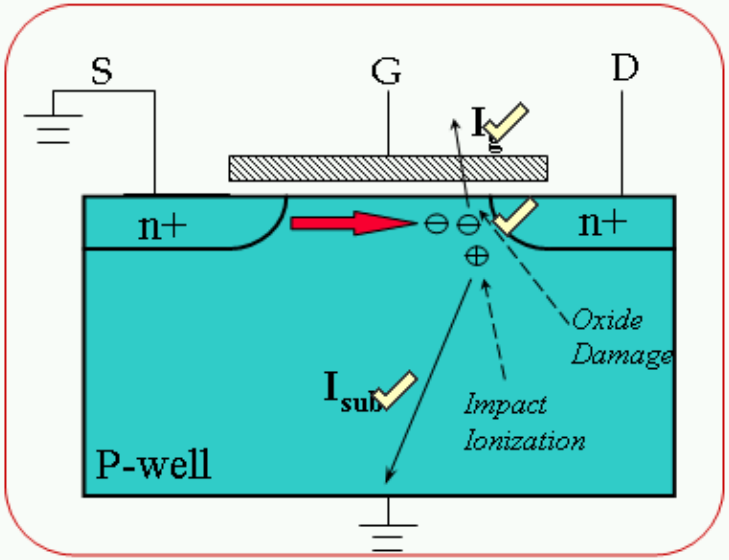
UltraSim in the Custom IC Flow



Reliability: A Growing Concern

Hot Carrier Effects

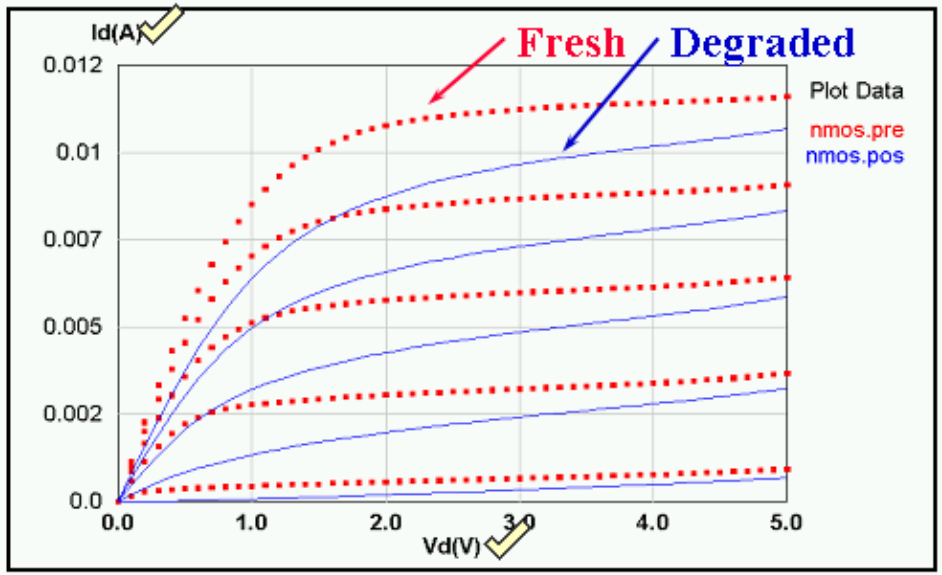
- E_{max} at drain corner causes hot carrier generation
- Hot carriers cause I_{sub}, I_{gate} and oxide damages



Hot Carrier Effects

Hot Carrier Effects

- Current driving capability degradation
  - Causes longer time delay
    - "Degraded" also sometimes called "aged"

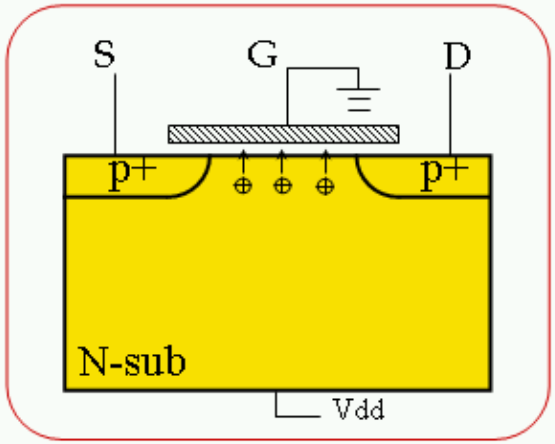


Hot Carrier Effects

0.13µm CMOS Crisis = NBTI

- "Reliability problems scale up as CMOS scales down"
  - By David Lammers, EE Times
    - April 12, 2002 (on-line at EETimes.com)
    - April 14, 2002 (EETimes print edition cover story)

- NBTI = Negative Bias Temperature Instability
  - Degrades performance & yield of PMOS devices ✓
  - Critical @ tox < 50 angstroms ✓
  - Results in immediate failures ✓
  - Reduces performance ✓



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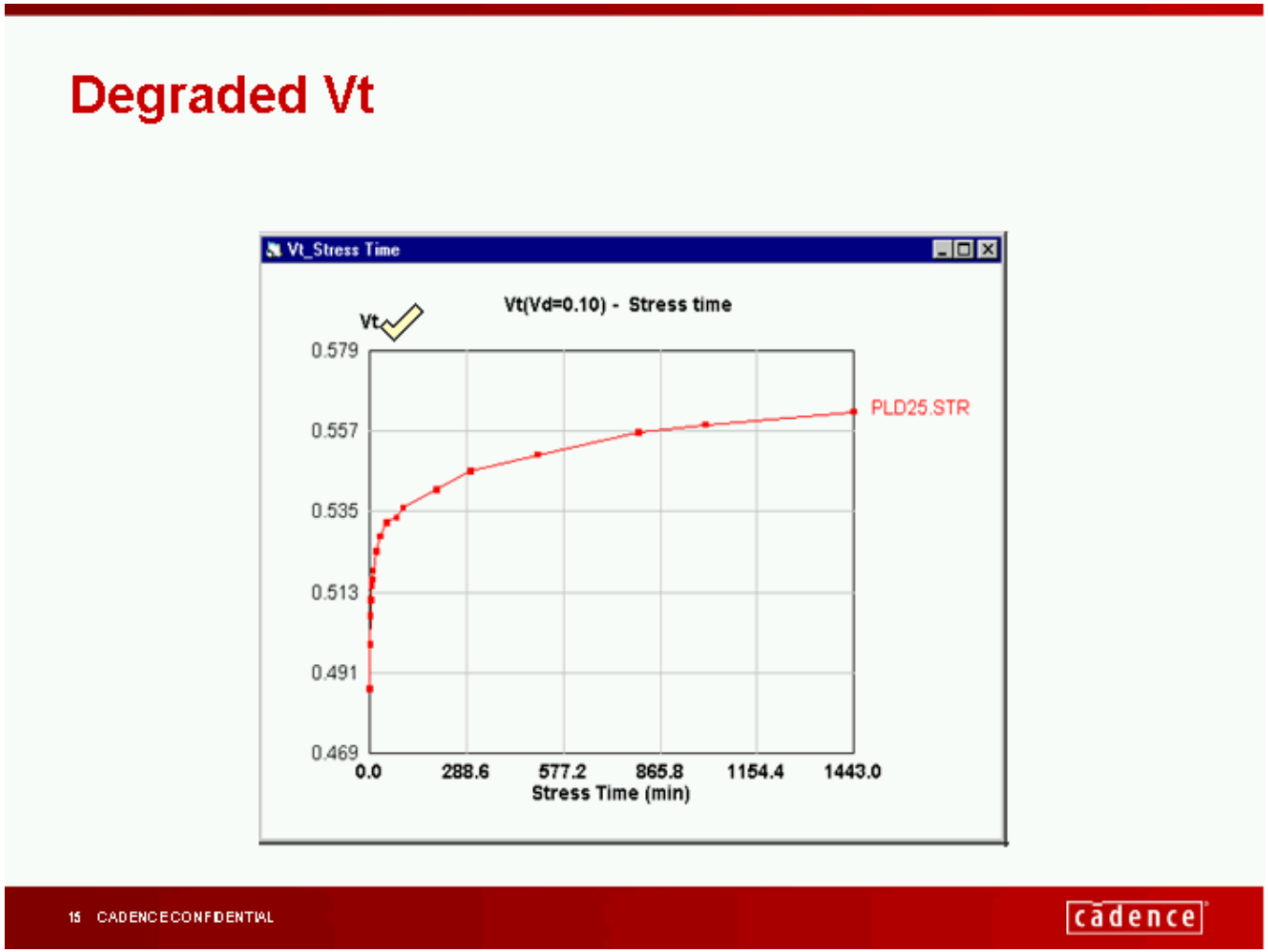
0.13?m CMOS Crisis = NBTI


Degraded Vt
Vt_Stress Time
Vt(Vd=0.10) - Stress time
Vt
0.579
0.557
0.535
0.513
0.491
0.469
PLD25.STR
0.0
288.6
577.2
865.8
1154.4
1443.0
Stress Time (min)
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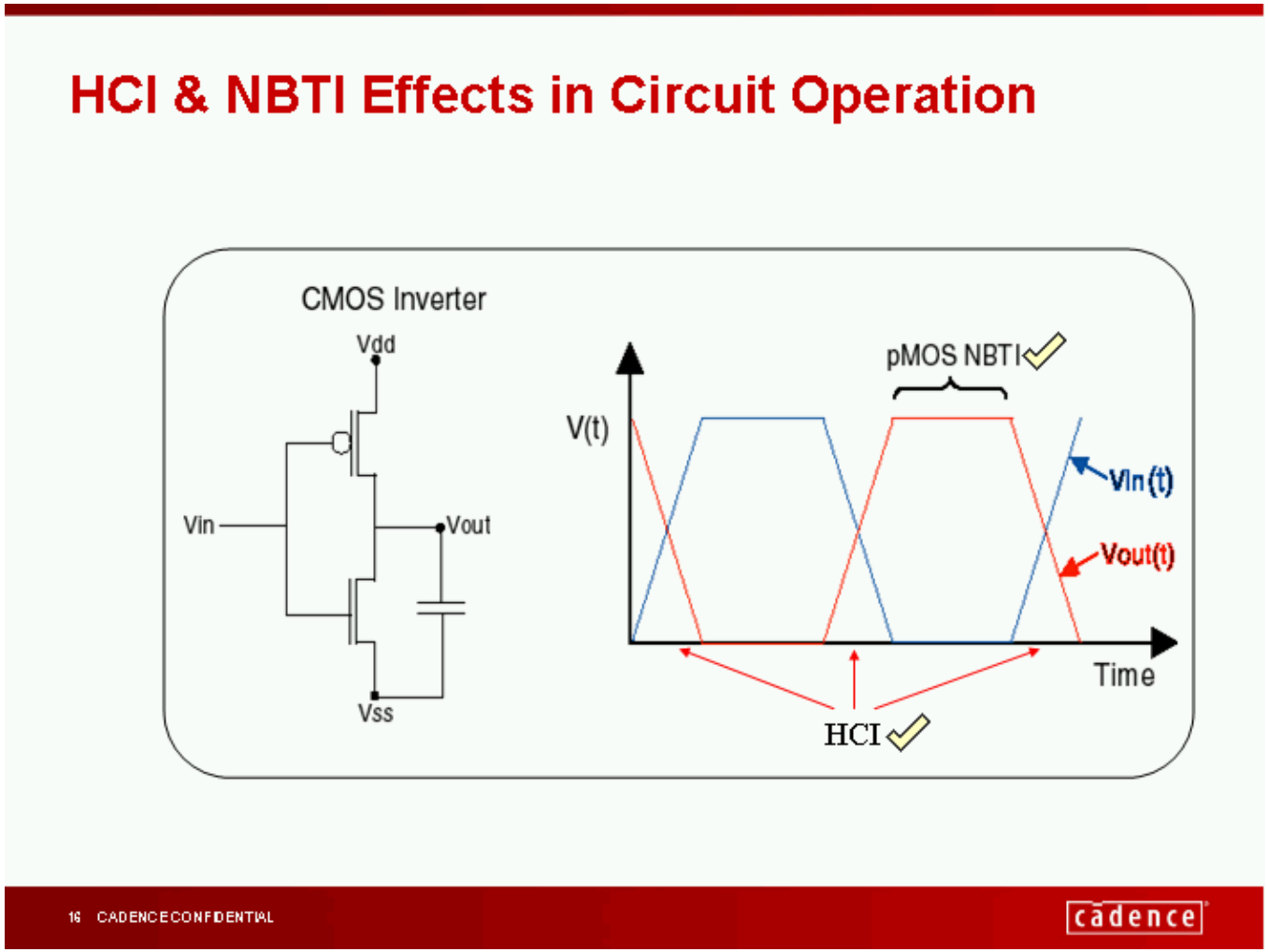
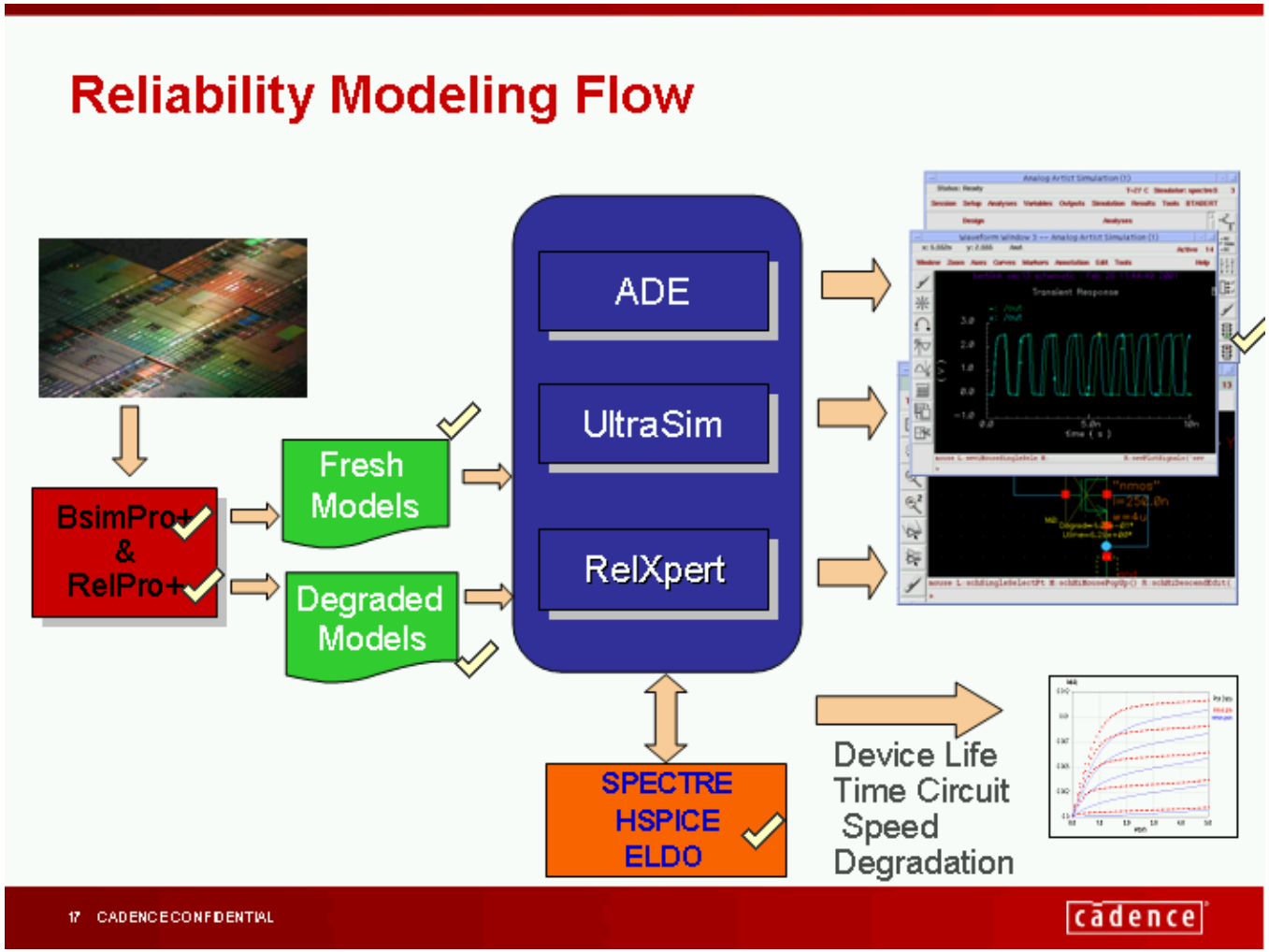
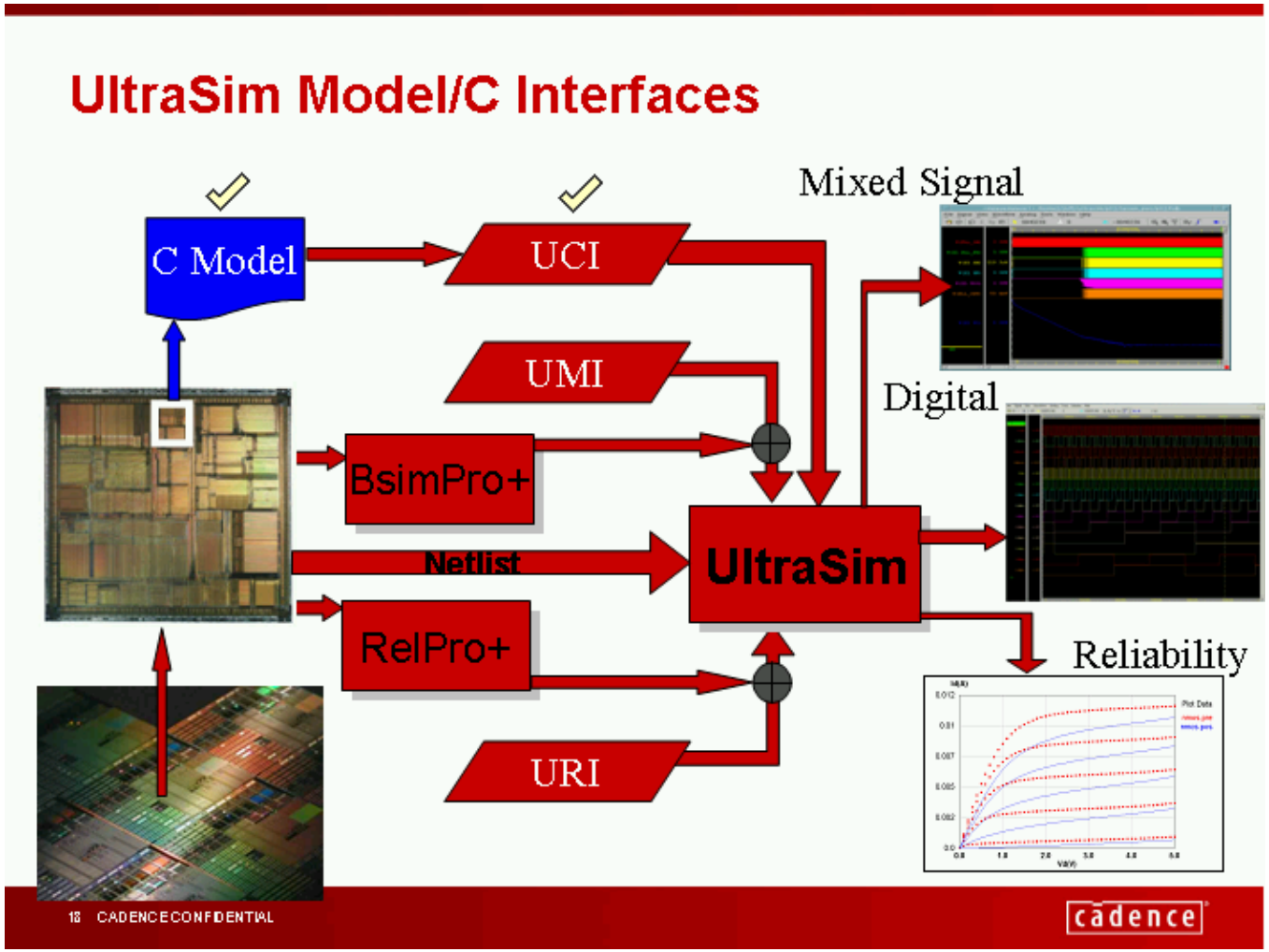
Degraded Vt



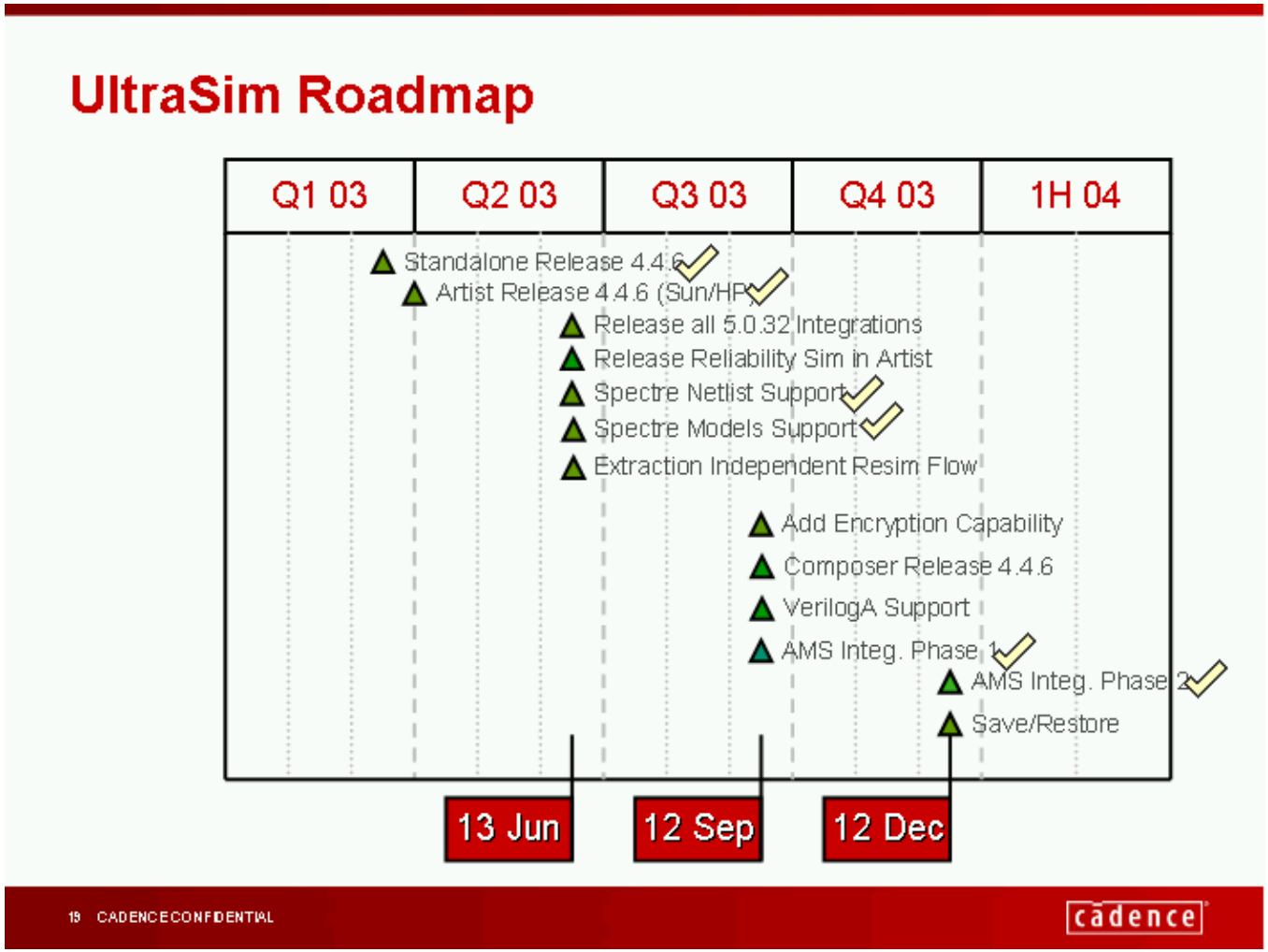
HCI & NBTI Effects in Circuit Operation



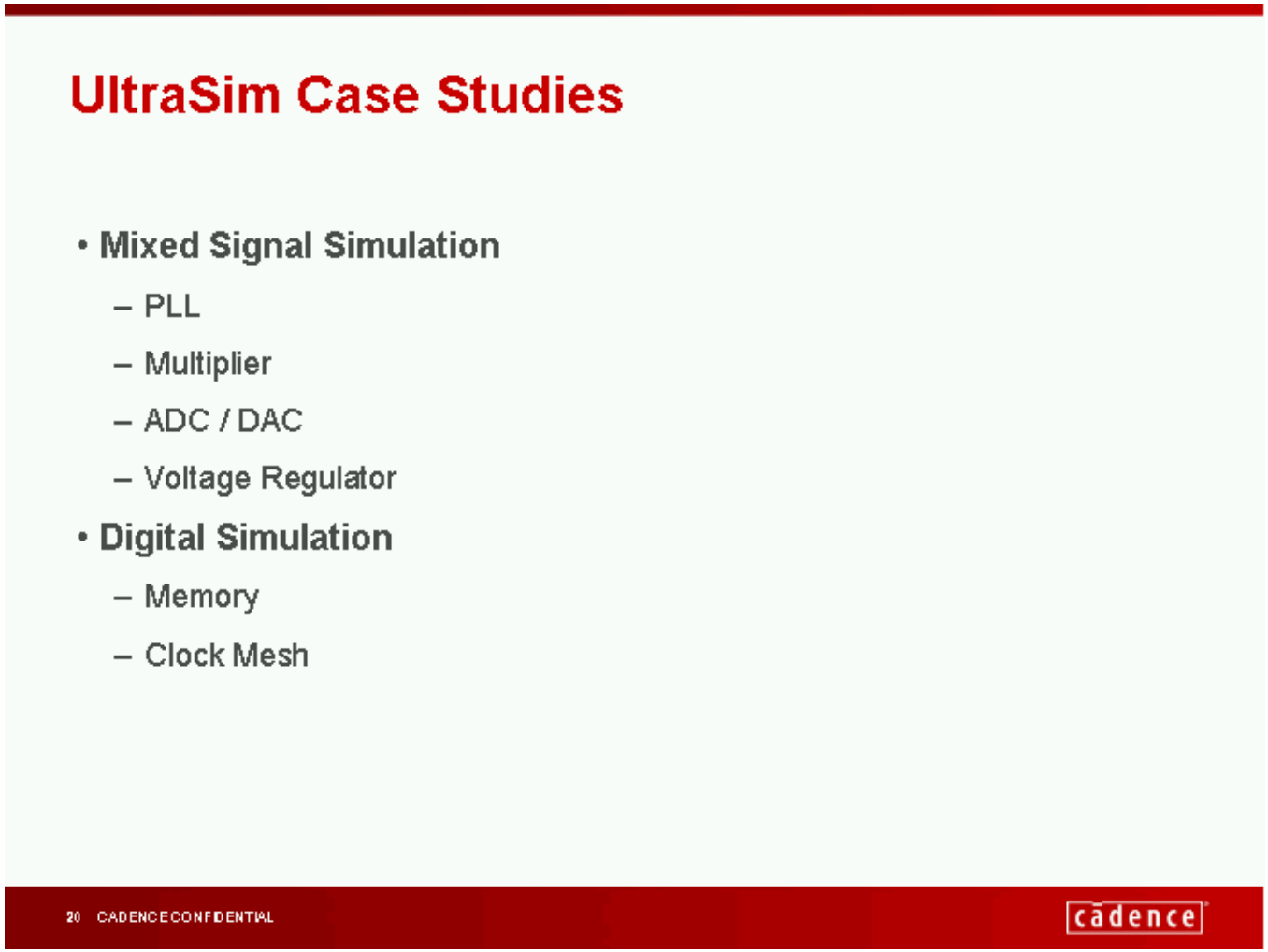
Reliability Modeling Flow



UltraSim Model/C Interfaces



UltraSim Roadmap

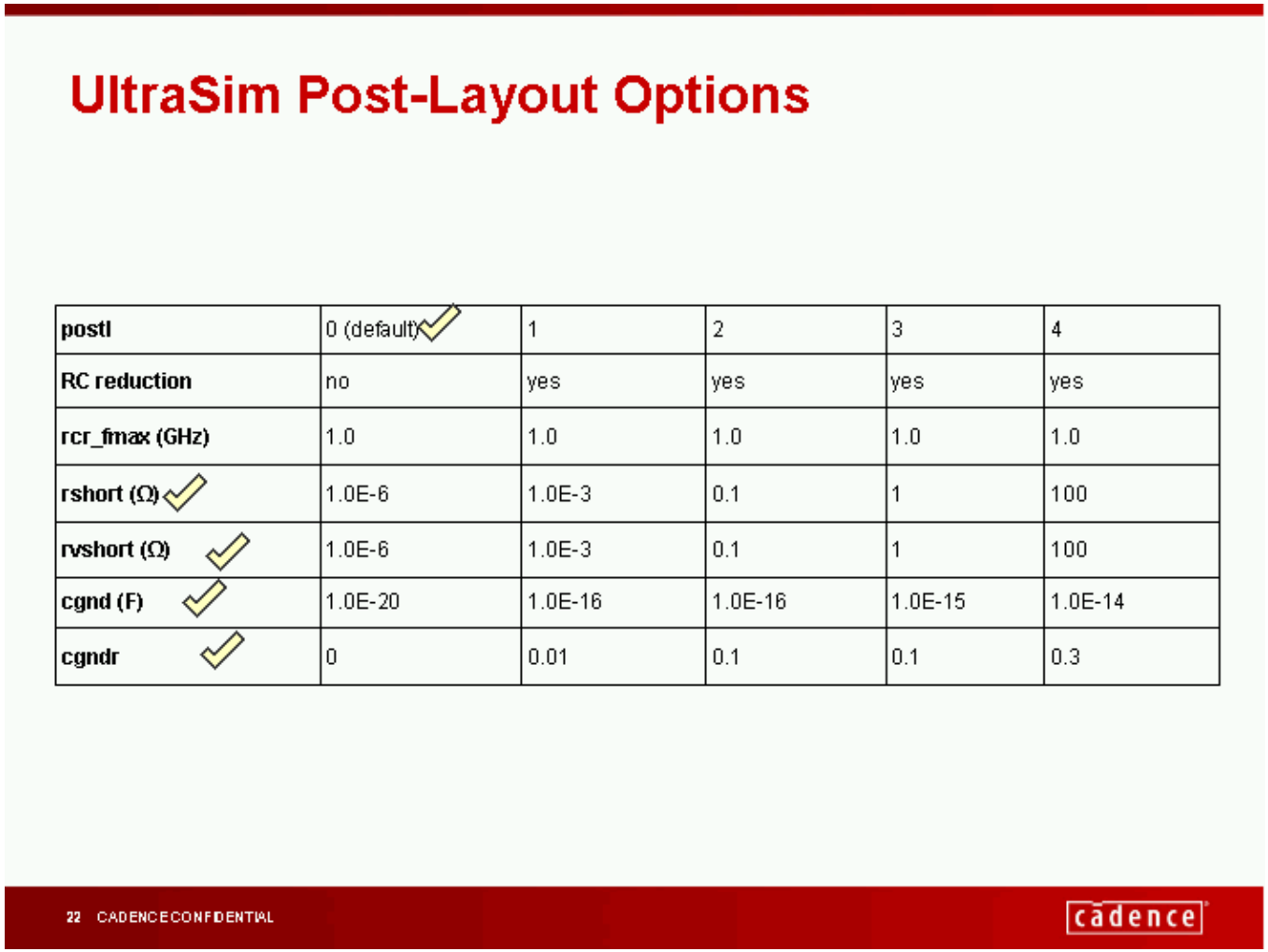


UltraSim Case Studies

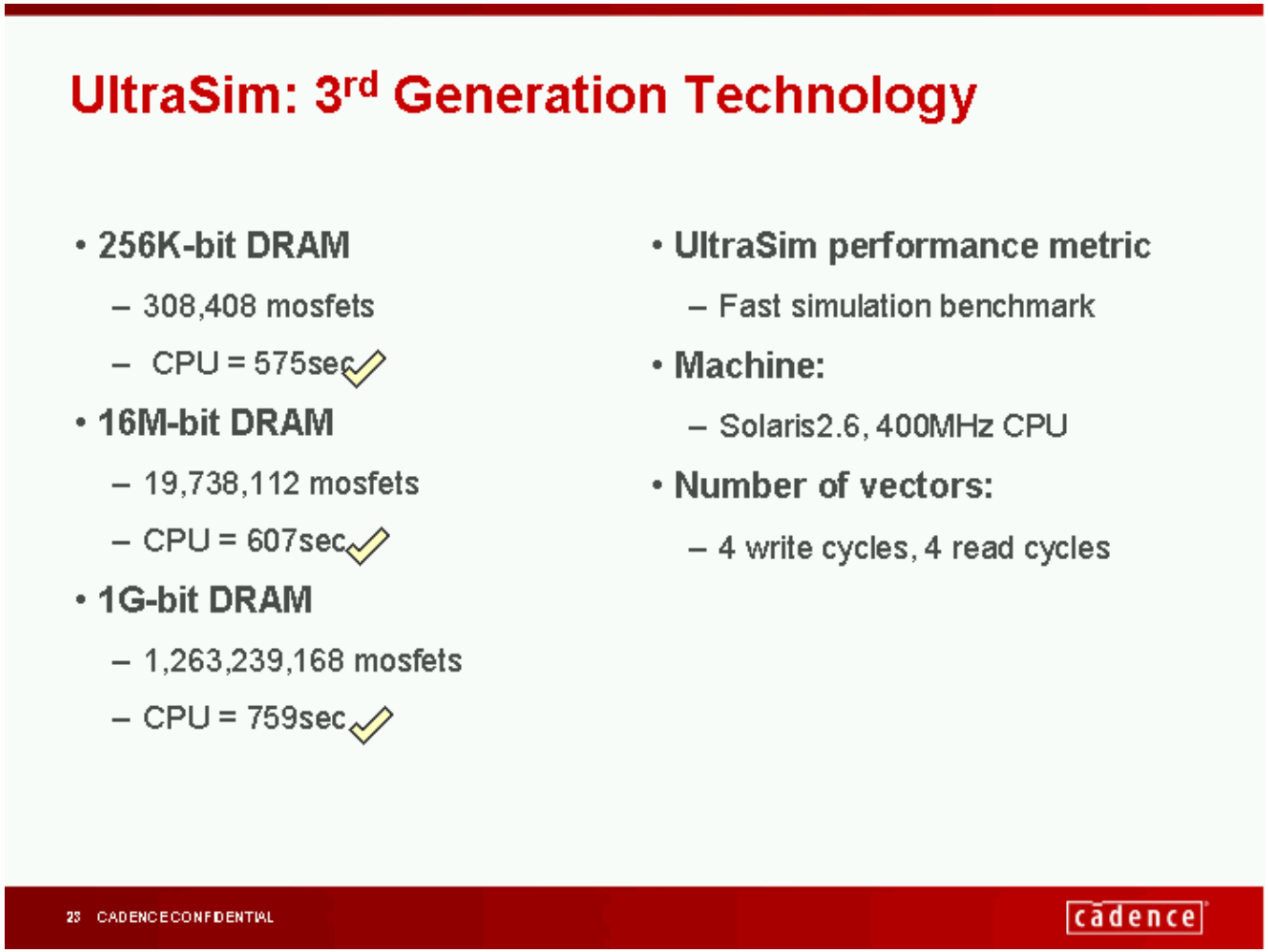
UltraSim Simulation Modes Overview

Simulation Mode	df (default) <digital fast mode>	da <digital accurate mode>	ms <mixed signal mode>	a <analog mode>	s <spice mode>	Option
MOSFET	**Digital Model**		**Analog Model**		**SPICE**	
Current / Charge Model	df	da	a		s	mos_methode
Diff. Junct.	df	da	a		-	mosd_methode
DIODE	df	da	a		s	diode_methode
BJT	s					
Accuracy	1 2 3	1 2 3	1 2 3	1 2 3	1 2 3	acc
Default Accuracy (Tol.)	1 (0.01)	2 (0.001)	2 (0.001)	2 (0.001)	2 (0.001)	acc (tol)
	acc=1 -> Relative Tolerance tol=0.01, acc=2 -> tol=0.001, acc=3 -> tol=0.0001					
Netlist Hierarchy	Autodetect (1)				Flat (0)	hier
Partitioning	Digital			Analog	None	
Target Error	< 10%	< 5%	< 1%	< 1%	< 1%	
Application	Functional Verification of Digital Circuits / Memories	Timing Verification of Digital Circuits and Memories, some PLL's, some AMS Designs	PLL's, AMS Designs, special Memories	DAC, ADC, DC/DC, Volt. Refs. Generators		

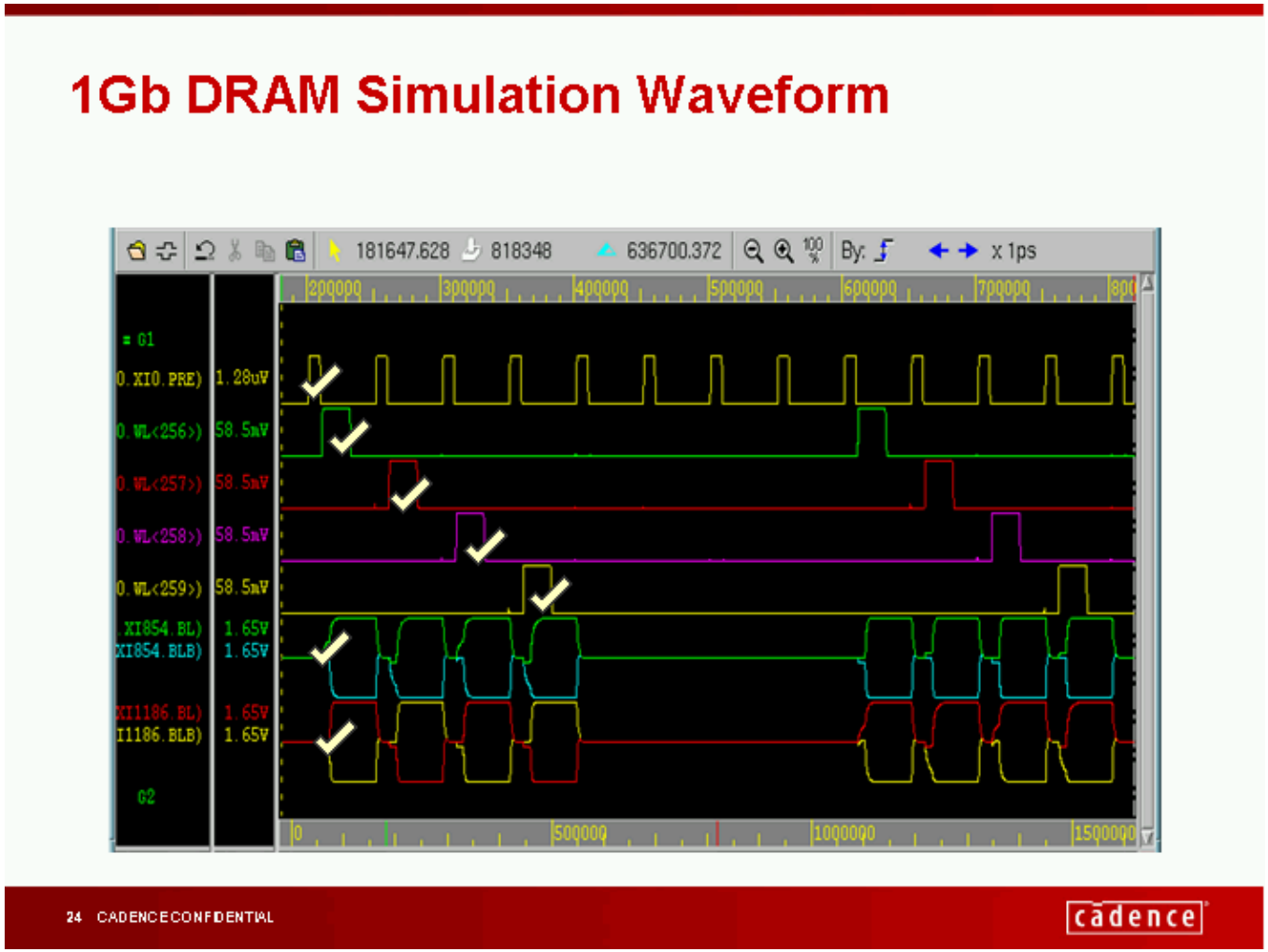
UltraSim Simulation Modes Overview



UltraSim Post-Layout Options



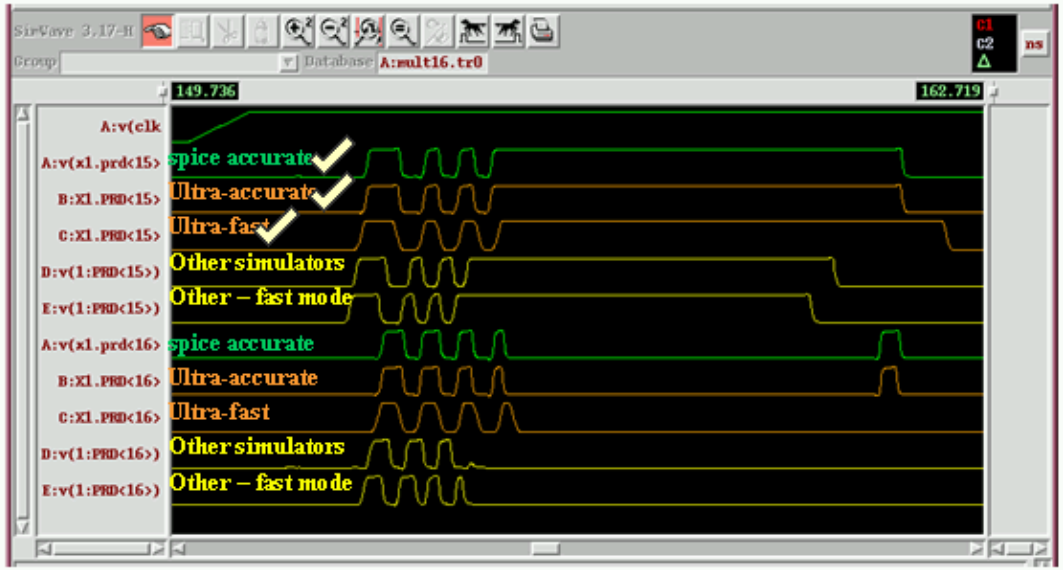
UltraSim: 3rd Generation Technology



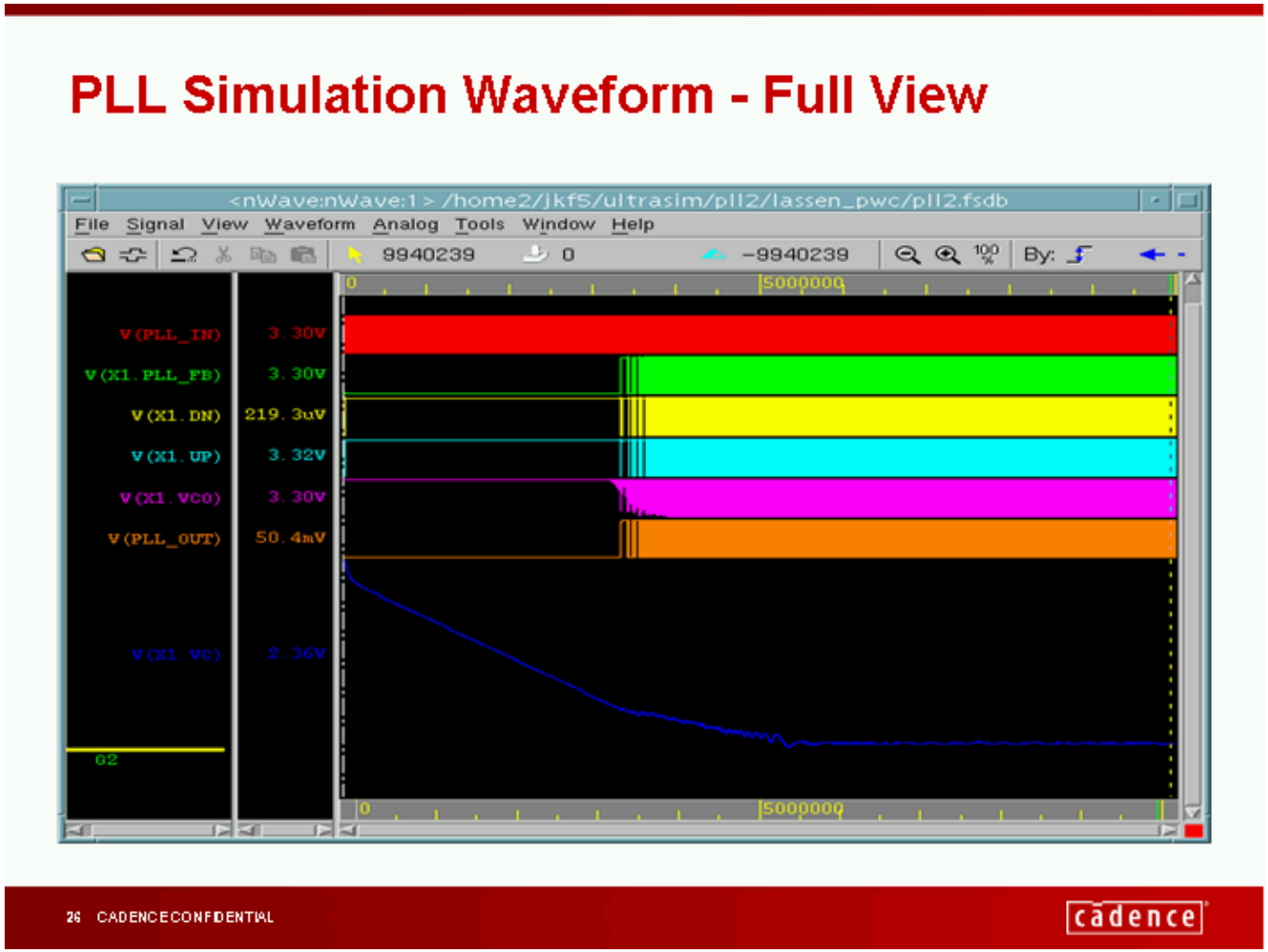
1Gb DRAM Simulation Waveform

UltraSim: Ultra-fast and Ultra-accurate

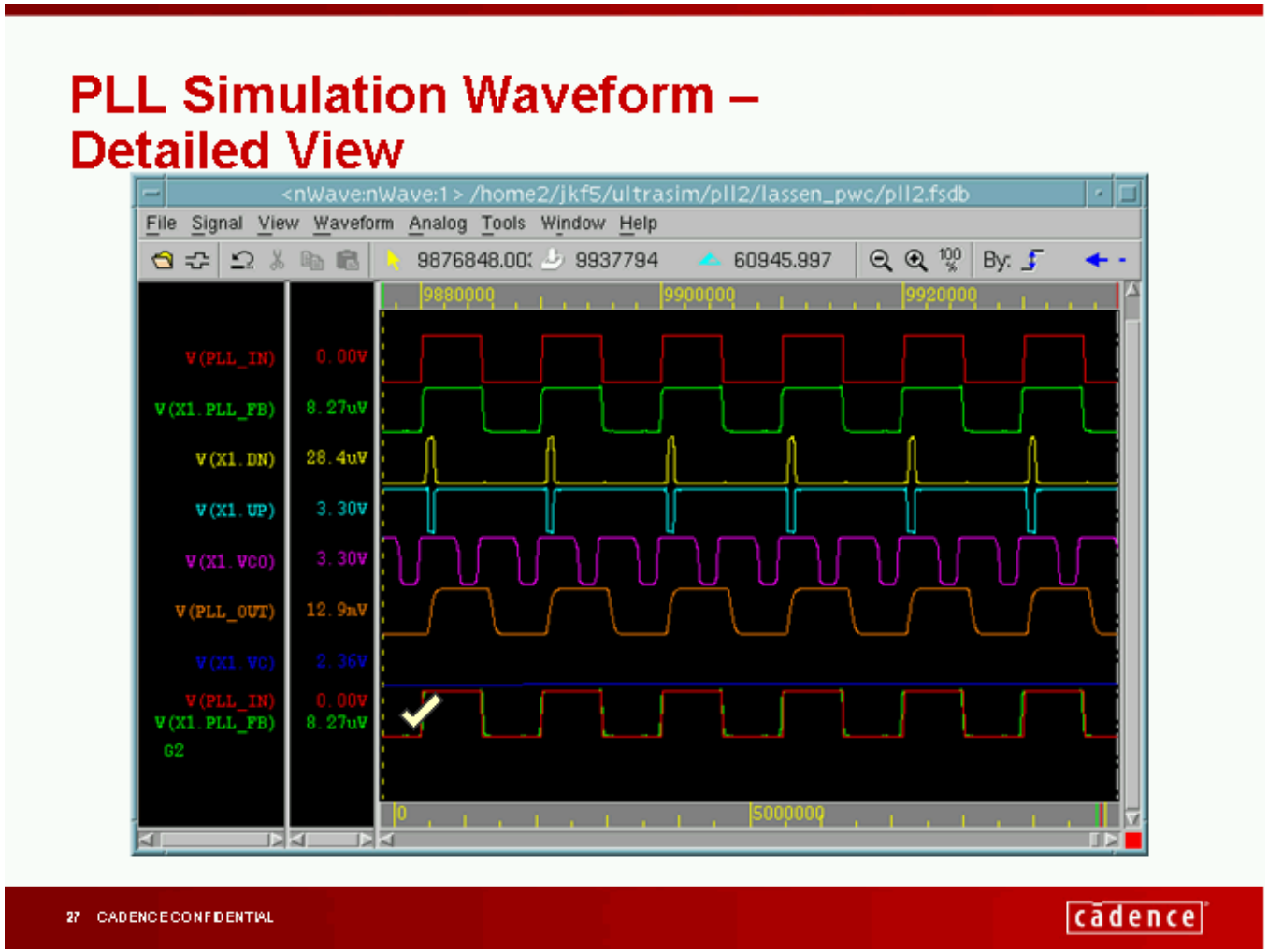
- Retains precision even in “fast” mode



UltraSim: Ultra-fast and Ultra-accurate



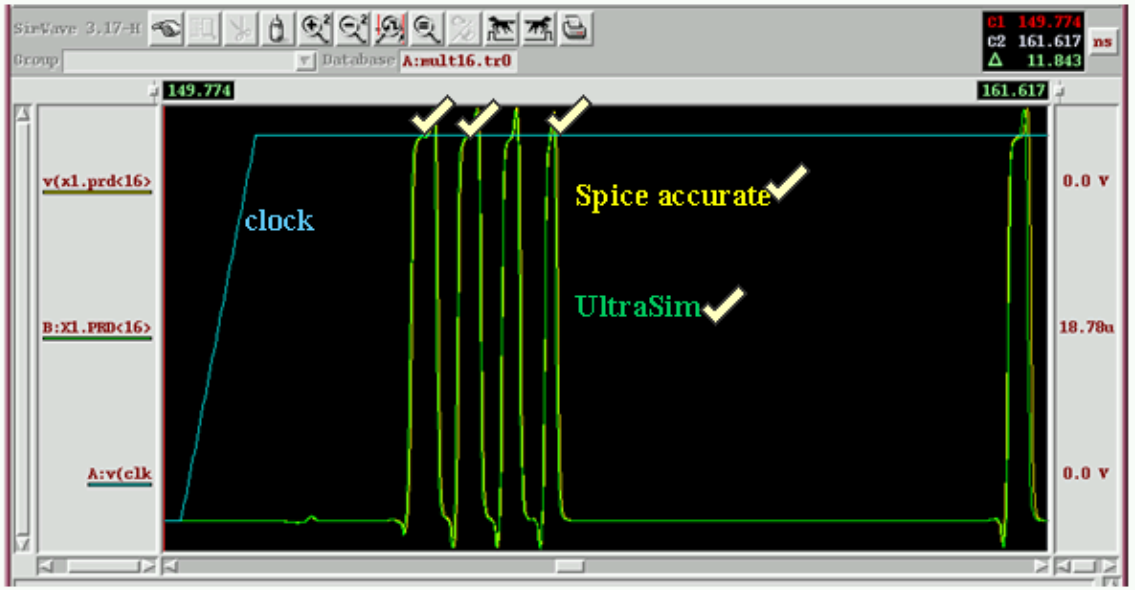
PLL Simulation Waveform - Full View



PLL Simulation Waveform ? Detailed View

UltraSim: Accuracy Is Key

- Spice & UltraSim overlaid for a 16bit Multiplier



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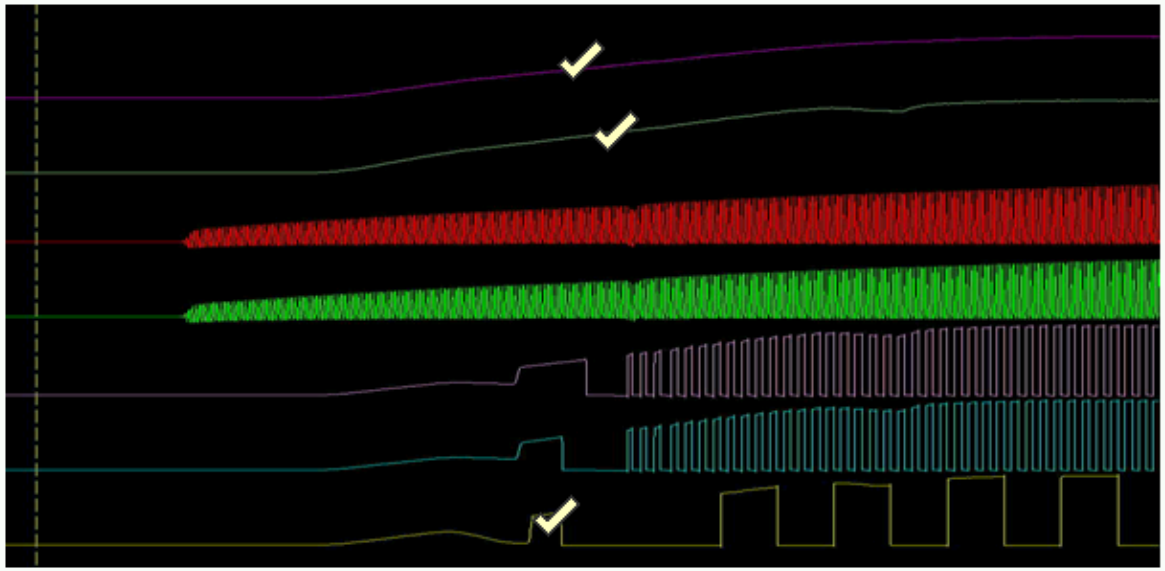
UltraSim: Accuracy Is Key

Mixed-Signal – Voltage Regulator

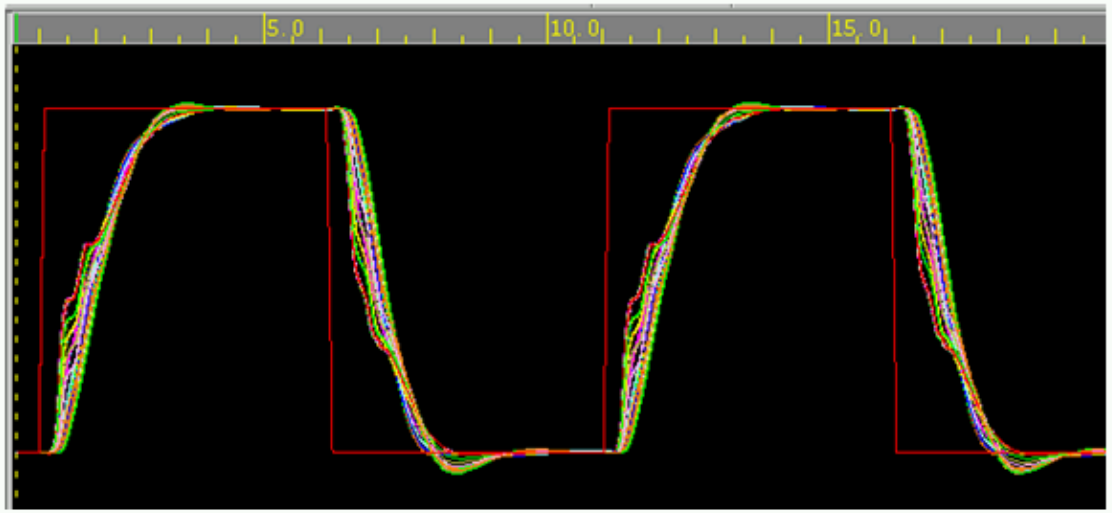
- Startup Sequence for Analog Portion



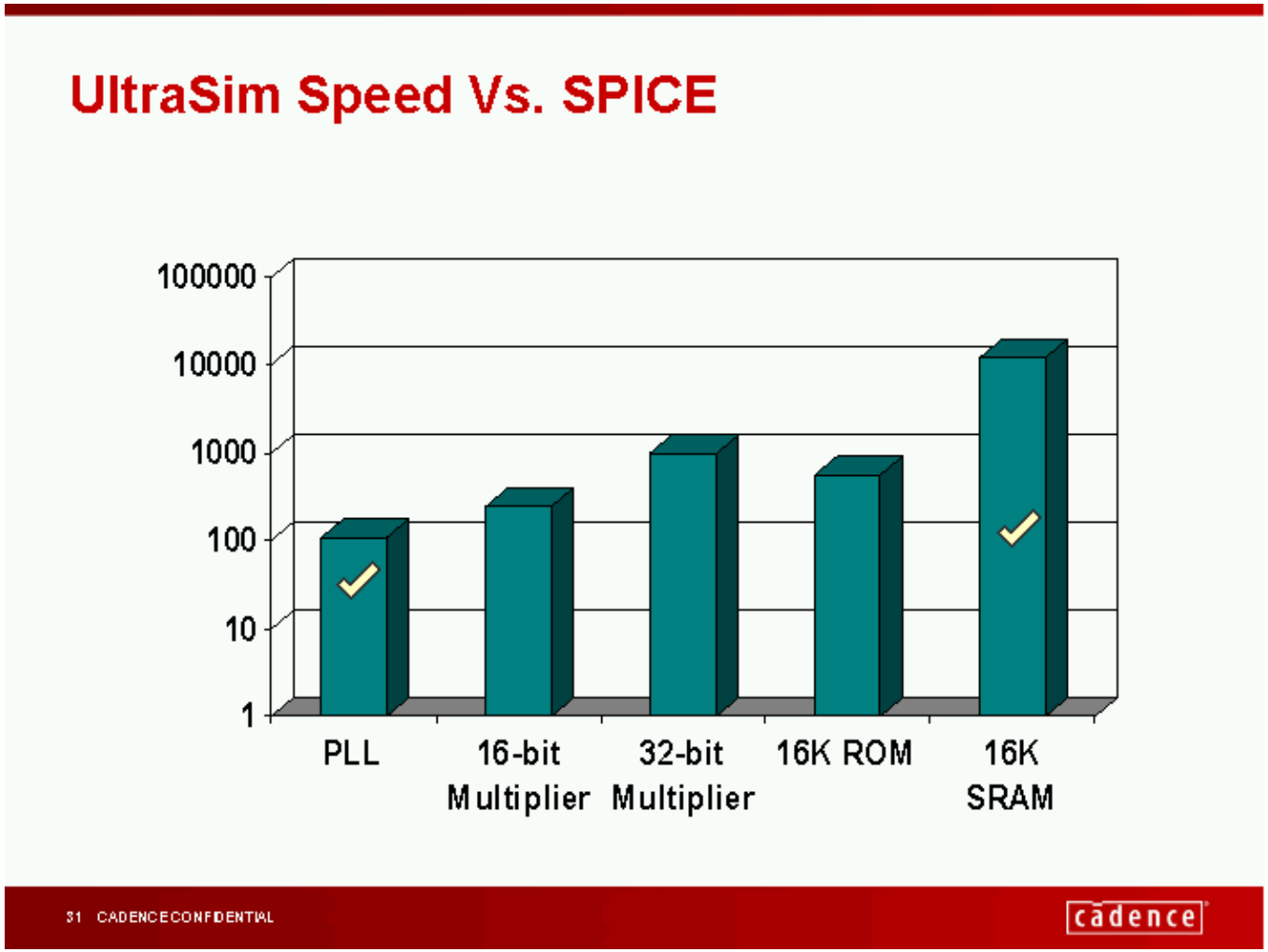
Mixed-Signal ? Voltage Regulator

Analysis of Clock Mesh

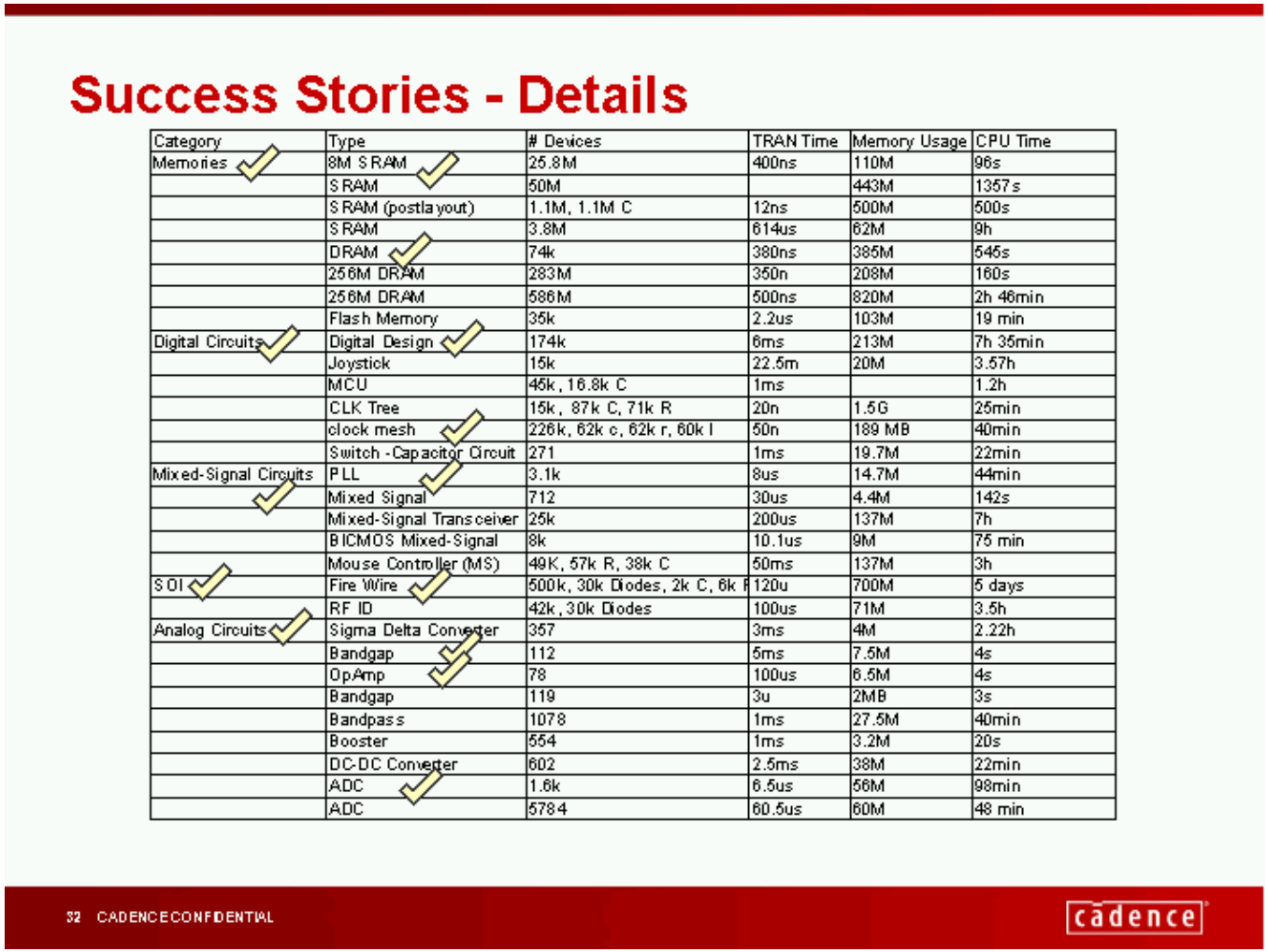
- Coupling induced noise
  - Capacitive and inductive effects



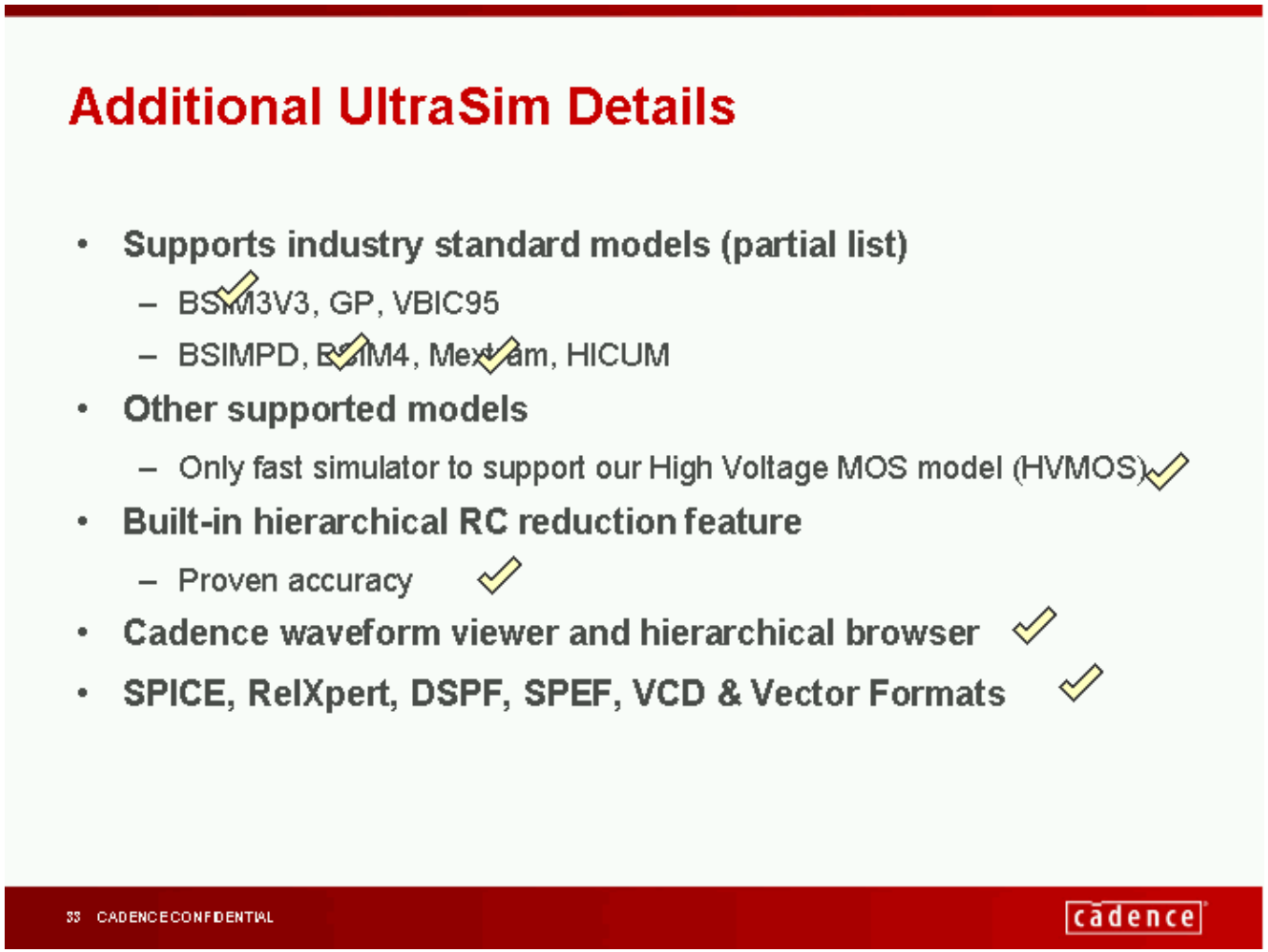
Analysis of Clock Mesh



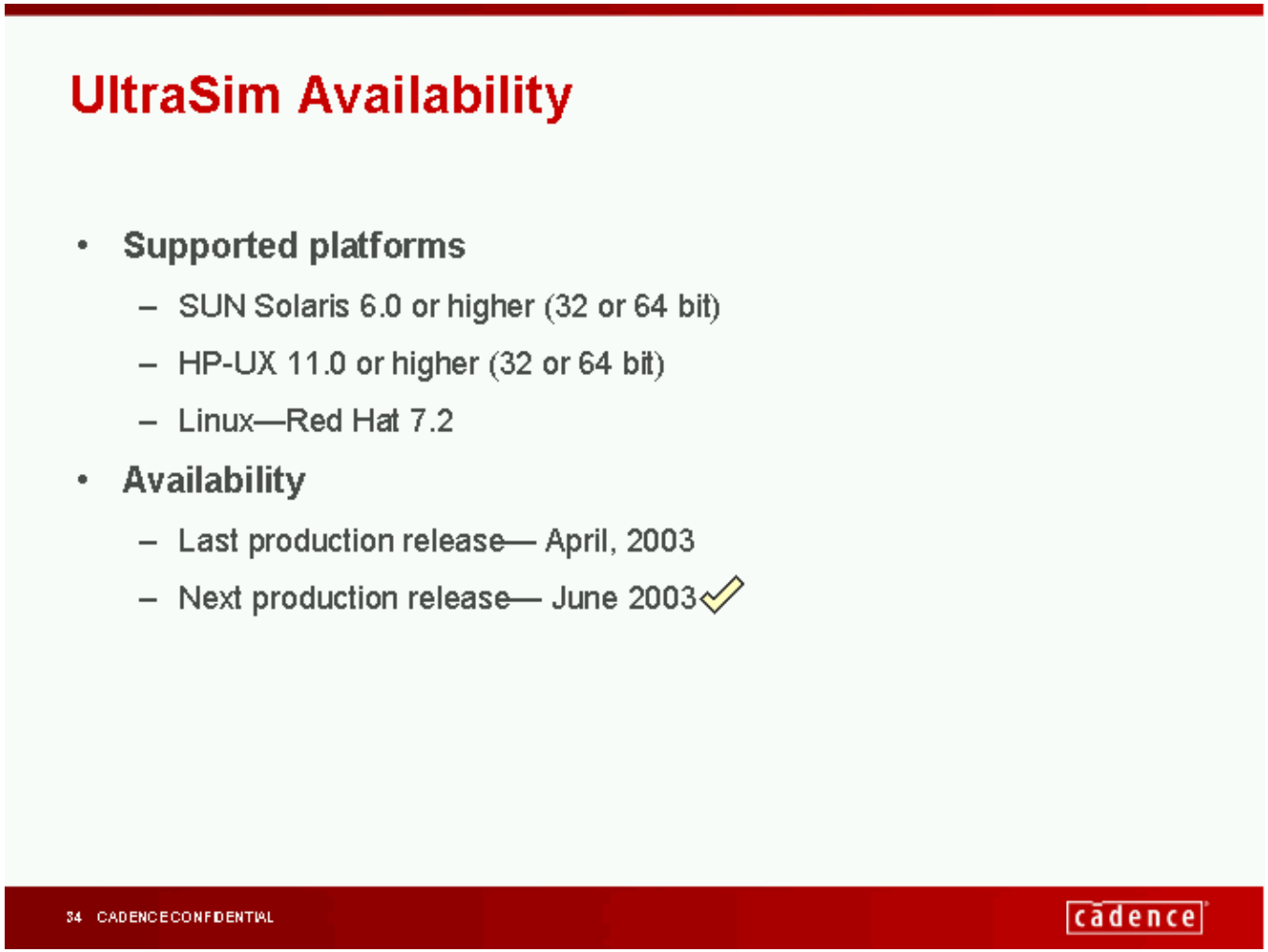
UltraSim Speed Vs. SPICE



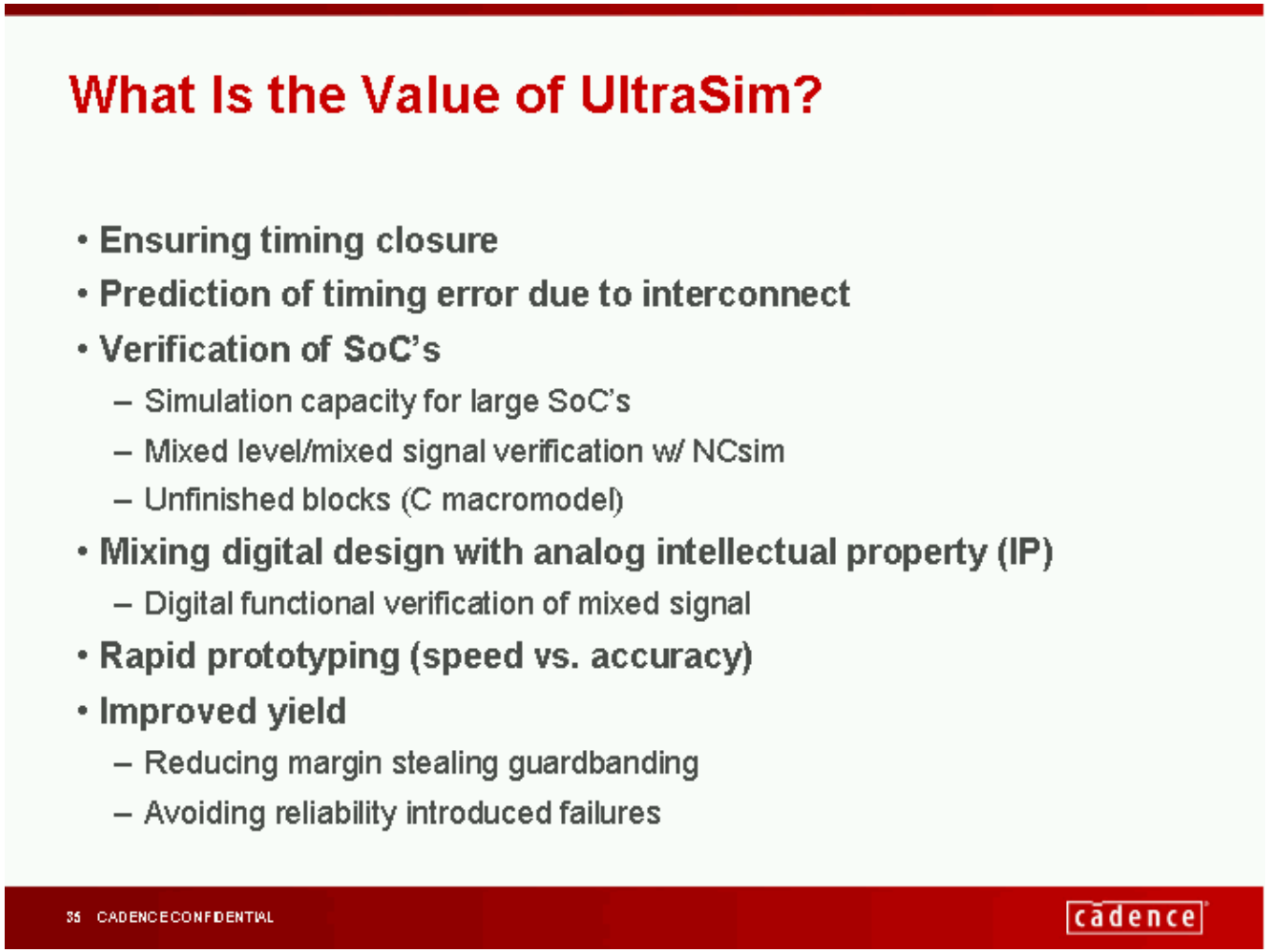
Success Stories - Details



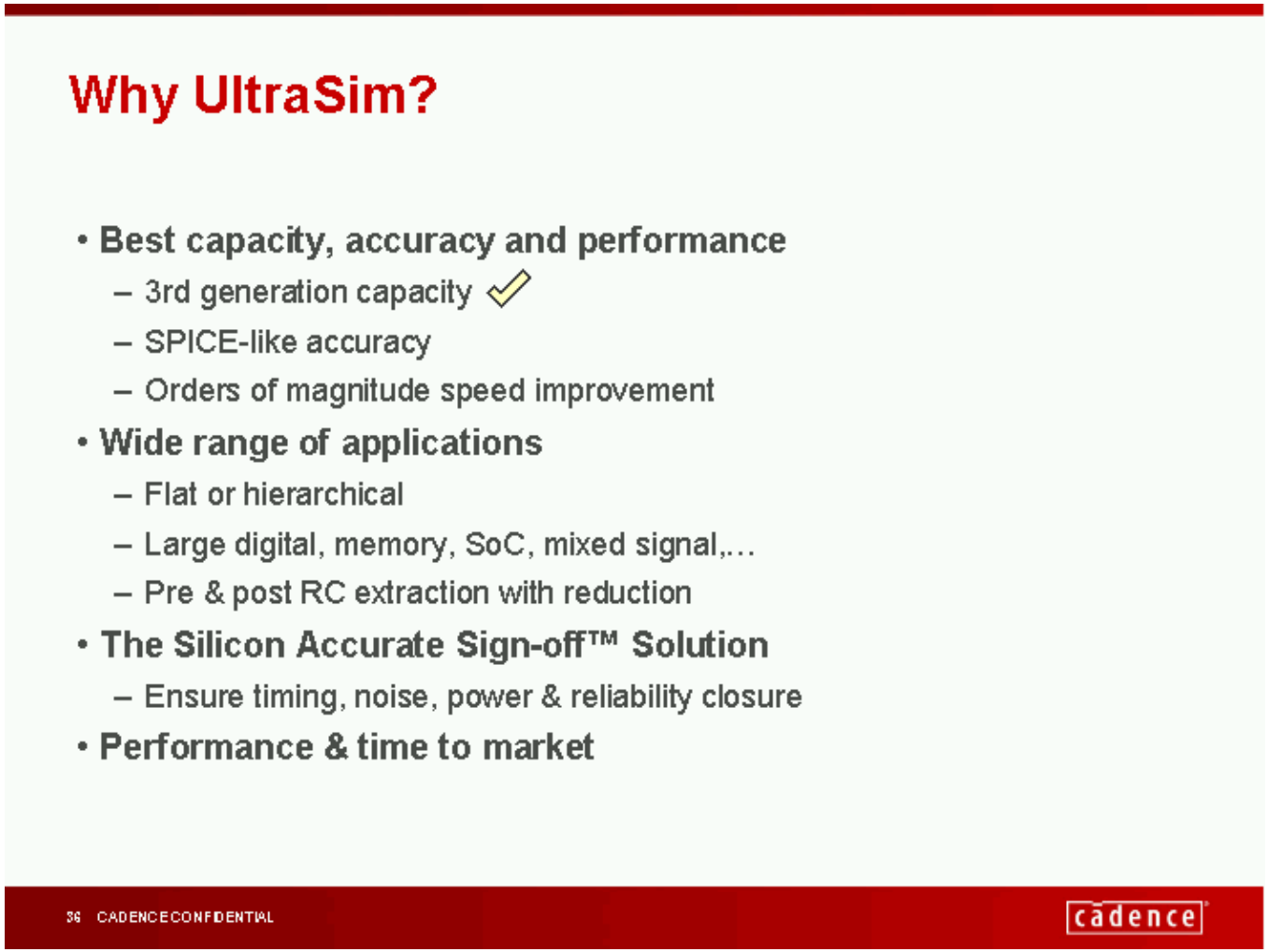
Additional UltraSim Details



UltraSim Availability



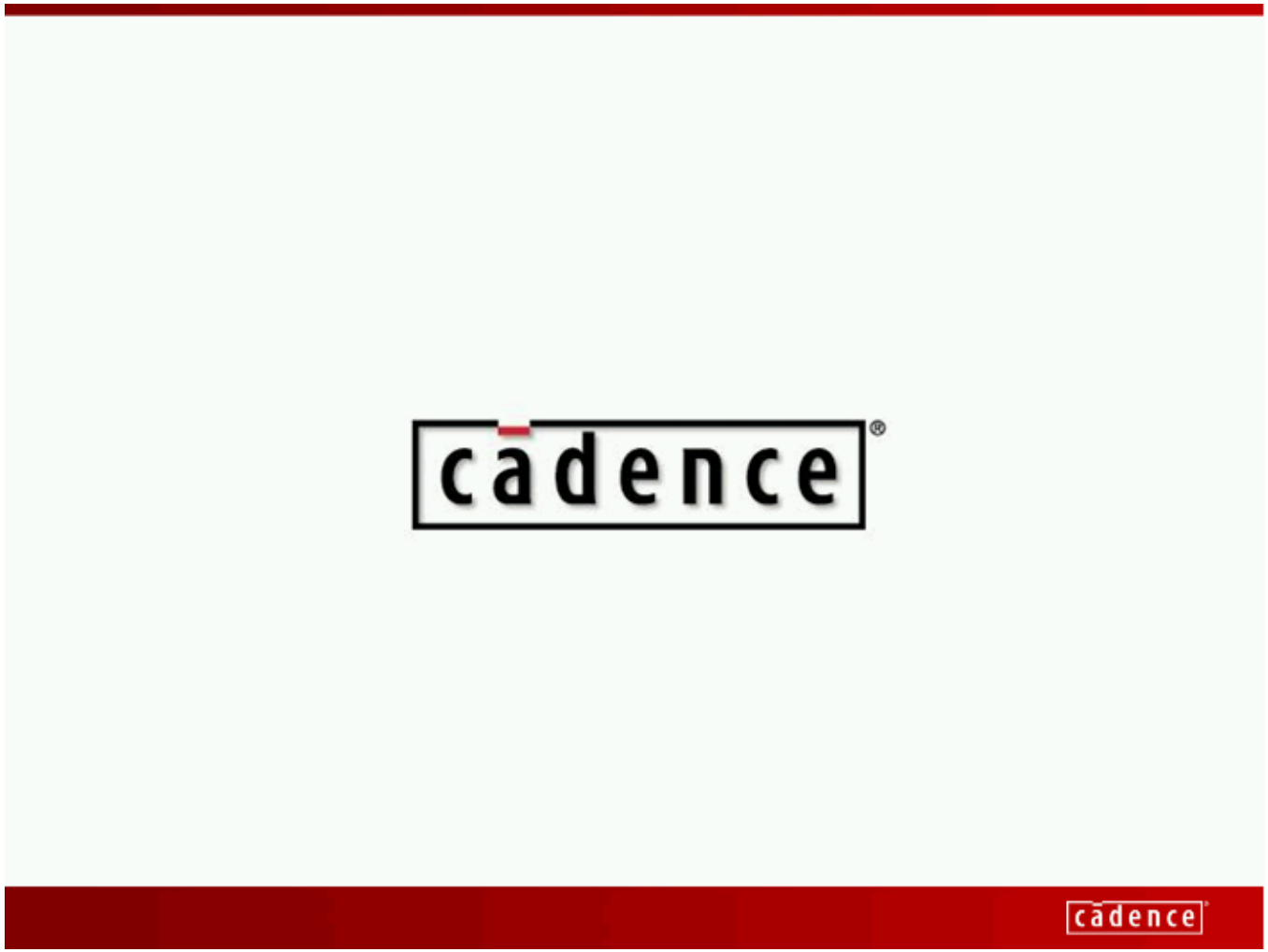
What Is the Value of UltraSim?



Why UltraSim?

Web Slide: http://www.cadence-europe.com/web_seminars/feedback.cfm?feedback_form_id=15

[Web Slide A]



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