ETH
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Analog Integrated Circuits
Exercise 3: Current Mirrors and References

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Hand in: 15.11.2013

The exercise takes place in room ETZ E6 on 1st and in room ETZ D61.2 on 8th of November. The exercise starts at 13:15 and ends at 15:00.

1 Introduction

This exercise deals with current mirrors and current/voltage references, thereby giving you hands-on experience in analyzing, designing and simulating these subcircuits. During the first part of this exercise we will study, with paper and pencil, the simplest current mirror structure and we will calculate its main parameters. The second half of the exercise will be dedicated to the simulation of the basic as well as more complex mirror structures. The current mirrors and current/voltage references presented in this exercise are widely used in practical circuits for various bias purposes.

1.1 The Design of Analog Circuits

The circuit simulator is necessary for the optimization of analog integrated circuits but will never replace initial hand calculations and circuit development with paper and pencil. Before we simulate a circuit we *must* have an idea of its functionality and — very importantly — we must know the rough size of its design parameters. A very simple circuit with just two MOSFETs already has six design parameters: the channel width and length, and the drain current of each MOSFET. If you have no idea of these numbers, then ”optimizing” the circuit with a simulator is going to be very tedious and in any case bad engineering practice. A trial and error procedure like this does not allow you to gain any insight in the circuit and is likely to end in a design that is not very creative and thus probably not very competitive. Therefore, a design should be started on paper using fairly simple device models. Of course, these hand calculations are not very accurate in the end but they allow you to understand the basic relationships between the design parameters and are a good starting point for the successive circuit optimization with a simulator.

For your hand calculations, use the long-channel equations to describe the MOSFET transistor and refer to the technological parameters given in the Appendix.

2 Current Mirrors

Current sources are widely used in analog circuits for bias purposes. Figure 1 shows a first attempt of a current source using a MOSFET. However, such a current source is never going to be used in a practical circuit as the current delivered heavily depends on process and temperature variations as well as on the the supply voltage. The threshold voltage V_{TH} of the MOSFET may vary up to 100 mV from wafer to wafer and both the mobility μ_{n} and the threshold voltage V_{TH} exhibit temperature dependence. Therefore, I_{REF} is poorly defined, and a different approach for generating currents in analog circuits is needed. The idea is to "copy" currents from a current reference with the assumption that one precisely defined current reference is available. We defer the problem of providing a current reference to section 3 of this exercise and are going to assume that such a current reference is already available.

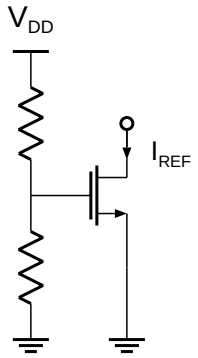

Figure 1: Bad current source - never use this!

2.1 Numerical Exercise

Consider the diode-connected transistor shown in Figure 2 and answer the following questions:

1. Regions of operation
   (a) List all the possible operating regions of an n-channel MOS transistor. How is the drain-source current I_{DS} defined in these regions of operation? Add the conditions for each region in terms of V_{GS}, V_{DS}, and V_{THn}.
   (b) Is the transistor M_1 in Figure 2 in saturation assuming $I_{\mathrm{B}} = 0.5\,\mathrm{mA}$?
   (c) Is the transistor M_1 still in saturation for $I_{\mathrm{B}} = 0$?
2. Operating point
   (a) Determine the large-signal node voltage V_1 for $I_{\mathrm{B}} = 0.5\,\mathrm{mA}$.
   (b) The width of M_1 is doubled and the length quadrupled ($W_1 = 10\,\mu\mathrm{m}$, $L_1 = 4\,\mu\mathrm{m}$). Determine the large-signal node voltage V_1 for $I_{\mathrm{B}} = 0.7\,\mathrm{mA}$.
   (c) By which factor α should the width of M_1 be increased to halve the DC operating point voltage V_1 with respect to the circuit specifications given in the previous problem?

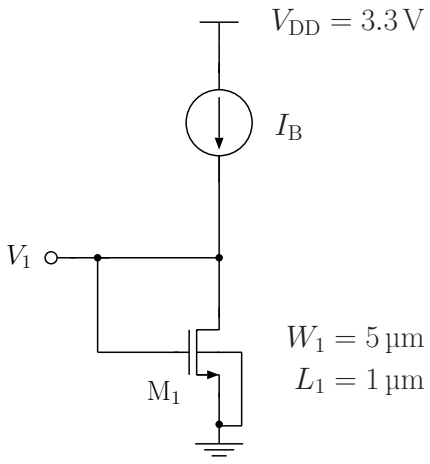

Figure 2: Simple diode-connected NMOS transistor.

3. Small-signal parameters

   The transistor M_1 has the dimensions $W_1 = 5.8\,\mu\mathrm{m}$ and $L_1 = 1\,\mu\mathrm{m}$ and the bias current is specified as $I_{\mathrm{B}} = 0.5\,\mathrm{mA}$.

   (a) Compute the transconductance g_{m} of M_1.

   (b) Determine the gate-source capacitance C_{GS} of M_1.

   (c) Determine the output resistance r_{out} of M_1.

An additional transistor M_2 and a resistor R_{L} are added to the circuit in Figure 2 resulting in the circuit in Figure 3. Answer the following questions:

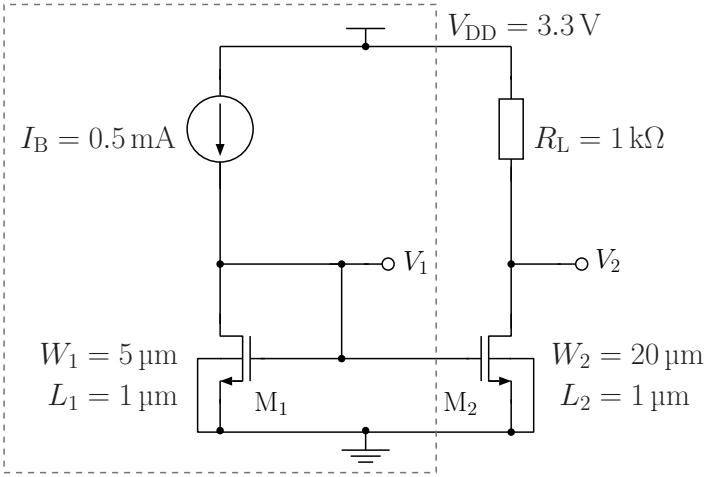

Figure 3: Simple MOSFET current mirror.

4. Current mirror

   (a) Determine the large-signal node voltages V_1 and V_2 assuming both transistors are in saturation.

   (b) Verify that both transistors are in saturation.

   (c) How can the width of transistor M_2 be set for the transistor to operate at the transition point from triode to saturation region (pinch-off)?

   (d) Determine the large-signal node voltage V_2 for the widths $W_2 = \{5, 15, 25\}\,\mu\mathrm{m}$.

2.2 Cadence Exercise

Two main characteristic parameters of a current mirror are its minimum output voltage $V_{\mathrm{OUT,min}} = V_{\mathrm{dsat2}}$ and its output resistance R_{out}. Determine these two values for the basic current mirror shown in Figure 4.

1. Create a directory `uebung3`. Change into that directory and start Cadence with the command `icdesign ams-hk4.10 &`.

2. Create a new library (e.g., `MyLibrary`) in the Library Manager and a new cell `CurrentMirror` with the view `schematic`. Refer to exercise 2 on how to do that if you do not remember any more.

3. Draw a schematic according to Figure 4. For the transistors use the cell `nmos4` from the library `PRIMLIB` and for the current source use the cell `idc` from the library `analogLib`. Do not forget to place a `gnd` component! Make both transistors 1.75 μm wide (the values in the fields `Width` and `Width Stripe` should match) and 0.35 μm long ($W/L = 5$). Hint: to mirror the transistor on the vertical axis press the button `Sideways` in the `Add.Instance` dialog.

4. Perform a DC sweep to plot the output characteristic of the current mirror. Sweep V_{OUT} from 0 V to 3.3 V. Now plot the drain current of M2 as a function of V_{OUT} and determine the output resistance of the current mirror in the region between 1 V and 2 V. (If your plot is empty, make sure you ticked the option `Select device currents: all` in the dialog `Outputs.Save All` of Analog Environment.) Also determine the rough value of V_{dsat2} from your plot.

5. Determine R_{out} and V_{dsat2} from a DC analysis! For the DC analysis set $V_{\mathrm{OUT}} = 1.5\,\mathrm{V}$. Tick the option `Save DC Operating Point` in the `Analyses.Choose` dialog and run the simulation. Afterwards choose `Results.Print.DC Operating Points` and click on the transistor M2 in the schematic to print the DC operating points. You may now determine R_{out} from `gds` and directly read out V_{dsat2}. How well do these values match the ones determined from the plot?

2.3 Reducing the Saturation Voltage

The previously made simulations have shown that the voltage $V_{\mathrm{OUT,min}} = V_{\mathrm{dsat2}}$ is fairly high compared to the supply voltage of just 3.3 V. Most of the times several transistors must be stacked upon each

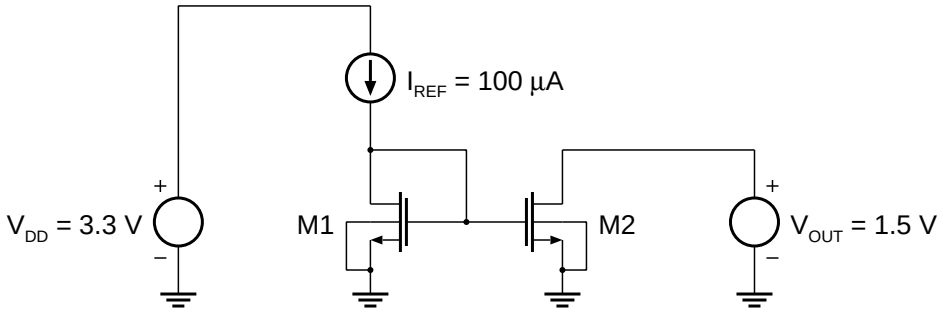

Figure 4: Simulation circuit for the current mirror.

other in the output branch to achieve a good current mirror (as will be shown later on in the exercise), which leads to a further reduction of the allowable voltage swing of the driven circuit. The problem of available voltage headroom for the driven circuit aggravates when the supply voltage shrinks to 2.5 V (0.25 μm processes), 1.8 V (0.18 μm processes), or even to 1.2 V (0.13 μm and 90 nm processes) as the saturation voltage does not scale down proportionally to the supply voltage.

In the following we want to reduce the saturation voltage to about 200 mV.

1. The saturation voltage of a MOSFET depends, among other parameters, on the W/L ratio. Therefore, we are going to change the W/L ratio in order to lower the saturation voltage. With help of the formulas given in the appendix determine an expression for V_{dsat} and solve it for W/L.
2. Determine the W/L ratio for $V_{\mathrm{dsat}} = 200\,\mathrm{mV}$. Keep L at 0.35 μm and calculate the needed W.
3. Simulate the current mirror of the last subsection with the new dimensions. Does the simulated V_{dsat} match the calculated one? Why? What happened to the output resistance?

2.4 Increasing the Output Resistance

Recall that the output resistance of a current source determines how well its current is defined. Therefore, we are interested in a high output resistance. The output resistance of a MOSFET may be modeled as

$$r_{\mathrm{o}} = \frac{L}{\lambda' I_{\mathrm{d}}}$$

for crude calculations where λ' is a proportionality constant. However, modeling the output resistance r_{o} of a MOSFET is actually very tricky. The output resistance is affected by many more parameters and effects than the simple formula suggests. Even elaborate models such as the BSIM3V3 model used in our simulations have difficulties in accurately modeling the output resistance.

1. From the simple formula above and the output resistance determined in point 3 of the previous subsection, calculate the channel length L that results in an output resistance of 2 MΩ.

2. Adjust W so that W/L remains constant and simulate the current mirror with the new dimensions. What is the simulated value of the output resistance? What happened to the saturation voltage?

The price we pay for a larger output resistance by increasing the channel length L is fairly high in terms of chip area. Moreover, increasing the channel width (remember we want to maintain the W/L ratio to keep V_{dsat} more or less constant) also increases the current mirror output capacitance. Therefore, other means for increasing R_{out} are desirable. The cascode current mirror presented in the next subsection is a much better solution to the problem and has further desirable properties.

2.5 High Swing Cascode Current Mirror (Optional)

So far the effect of channel length modulation has been neglected. However, when also taking into account channel length modulation, the simple current mirror equation eq. (1)

$$I_{\mathrm{OUT}} = \frac{W_2/L_2}{W_1/L_1} I_{\mathrm{REF}} \tag{1}$$

becomes

$$I_{\mathrm{OUT}} = \frac{W_2/L_2}{W_1/L_1} \frac{1+\lambda V_{\mathrm{ds2}}}{1+\lambda V_{\mathrm{ds1}}} I_{\mathrm{REF}}. \tag{2}$$

Eq. (2) shows that the drain-source voltages of M1 and M2 should be made equal for I_{OUT} to be a precise copy of I_{REF}. However, V_{ds2} in Figure 4 is defined by the driven circuit. The idea is now to use a cascode in the output branch, i.e. to stack another transistor on top of M2 in order to shield the drain of M2 from variations of the output voltage. The resulting structure is known as a cascode current mirror. However, it can be shown that this cascode current mirror loses one threshold voltage in voltage headroom for V_{out} (see P. Gray et al., 5th Ed., Ch.4, Par.4.2.5, pp.261, for the derivation). Therefore, in practical circuits the high swing cascode current mirror of Figure 5 is used, since this structure does not exhibit the mentioned disadvantage of the normal cascode current mirror.

1. The cascode current mirror was suggested because of its increased output resistance. Draw the small signal equivalent circuit of the output branch of Figure 5 and derive the formula for the output resistance. Do you expect a significant increase in the output resistance based on your formula?

2. What conditions must be satisfied for V_{B1} and V_{B2} so that R_{out} becomes large?

3. Eq. (2) shows that V_{ds1} and V_{ds3} should be equal when channel length modulation is considered. Why does it make sense to set $V_{\mathrm{B1}} = V_{\mathrm{B2}}$? Set $V_{\mathrm{ds1}} = V_{\mathrm{ds3}}$ and derive the relationship between $\frac{W_1/L_1}{W_3/L_3}$ and $\frac{W_2/L_2}{W_4/L_4}$ for $V_{\mathrm{B1}} = V_{\mathrm{B2}}$ and a general ratio of $\frac{I_{\mathrm{OUT}}}{I_{\mathrm{REF}}}$. Use the MOSFET formulas given in the appendix (i.e., do not include the factor $(1+\lambda V_{\mathrm{ds}})$ for the drain current I_{d}).

4. Dimension the high swing cascode current mirror so that $V_{\mathrm{dsat1}} = V_{\mathrm{dsat2}} = 200\,\mathrm{mV}$ for $I_{\mathrm{REF}} = I_{\mathrm{OUT}} = 100\,\mu\mathrm{A}$. Assume an imposed output voltage of 1.5 V and set $V_{\mathrm{B}} = V_{\mathrm{B1}} = V_{\mathrm{B2}}$. For

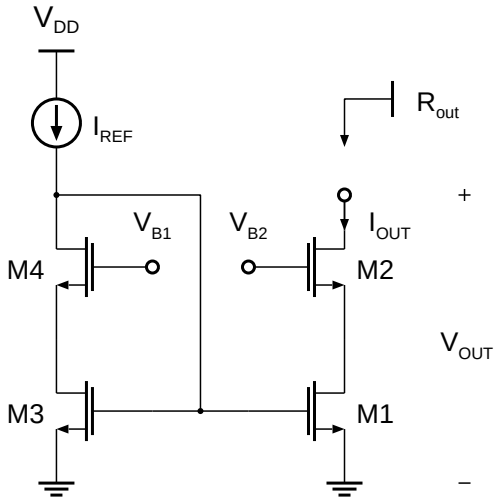

Figure 5: High swing cascode current mirror. (The bulk terminals of all NFETs are connected to the ground potential.)

the derivations use the MOSFET formulas given in the appendix (i.e., do not include the factor $(1 + \lambda V_{\mathrm{ds}})$ for I_{d}). Use minimum channel length transistors to minimize the current mirror output capacitance and save chip area. At some point you will have to select an appropriate value for V_{DS1}. On the one hand, we would like to make V_{DS1} small to leave as much voltage headroom as possible for the driven circuit. On the other hand however, we want to avoid that M1 operates in triode region, thereby degrading the output resistance of the current mirror. From these considerations, $V_{\mathrm{DS1}} = 1.5 \times V_{\mathrm{dsat1}}$ probably is an adequate choice. This now enables you to determine the value of V_{B}.

5. The only quantity still missing to compute the output resistance of the current mirror with the formula of point 1 is the channel length modulation coefficient λ. However, λ strongly depends on the drain-source voltage and may vary as much as from 0.05 1/V to 0.5 1/V (or more). Therefore, relying on an accurate value for λ is problematic in hand calculations. Generally, it is a bad idea to solve $I_{\mathrm{d}} = \frac{K_{\mathrm{P}}}{2}\frac{W}{L}(V_{\mathrm{gs}} - V_{\mathrm{TH}})^2(1 + \lambda V_{\mathrm{ds}})$ for V_{ds}; the variations in λ cause V_{ds} to deviate significantly from the calculated value! Nevertheless, estimate of the output resistance by assuming $\lambda_{\mathrm{n}} = 0.1\,1/\mathrm{V}$.

6. You are now in a position to plug your design of the cascode current mirror into the simulator. Create a new cell in the Schematic Composer and draw the circuit schematic of Figure 5. After you have specified all transistor dimensions and voltage sources according to your design, start Analog Environment and perform a DC analysis. When the simulation has finished, annotate the DC node voltages and the DC operating points in the schematic by clicking `Results.Annotate.DC Node Voltages` and `Results.Annotate.DC Operating Points` in the Analog Environment window. The subset of parameters displayed for the components may be changed. Let us add `gds` for the transistors: Choose `Edit.Component Display` in the schematic window, tick the option `Select Label: parameter` and make sure the following options are active below: `library`, `operating point`, and `DC`. Afterwards click on a `nmos4` in the

schematic window which allows you to specify the subset of parameters displayed for that component. E.g., `id`, `gds`, `vds`, and `vdsat` is a convenient subset for our purposes. Now compare the node voltages and operating points from the simulation with your designed values.

7. To determine the output resistance of the current mirror set `AC magnitude` of the output voltage source to 1 and perform an AC analysis from 1 kHz to 1 GHz. You may now plot the expression `real(-VF("/VOUT")/IF("/VOUTsrc/PLUS"))` (adjust to the names in your schematic) to determine the output resistance as a function of the frequency. Compare the low-frequency output resistance to the calculated one. How good was our estimate of λ_n? How would you proceed if you had to further increase the output resistance? Compare the chip area occupied by our cascode current mirror to the chip area of the simple current mirror from the previous subsection.

3 Current and Voltage References

In the last section we have always assumed that a precisely defined current reference I_REF is available. This section now treats the design of current and voltage references. Generally, a voltage reference may be obtained by loading a current reference with a precisely defined load. The design of current references and voltage references is thus closely related to each other. The last two subsections will treat the design of voltage references in particular.

3.1 Simple Current Reference

The circuit of Fig. 1 was introduced as a bad example of a current source. A better version of a current source is depicted in Figure 6. The left circuit (a) shows a NMOS and the right circuit (b) a PMOS implementation of a current source. However, note that the current sources of Figure 6 still depend on the supply voltage V_DD and are, of course, sensitive to process and temperature variations.

1. Have a look at the PMOS configuration of Fig. 6b and assume $I_\mathrm{OUT} = 100\,\mu\mathrm{A}$ and $V_\mathrm{DD} = 3.3\,\mathrm{V}$. How large should the output resistance r_o2 of M2 be so that I_OUT remains within 1% of its nominal value regardless of the drain voltage of M2?

2. Do you think the required output resistance is attainable with reasonably sized transistors? You may assume that $\lambda_\mathrm{p} = 0.2\,1/\mathrm{V}$ for a minimum channel length transistor.

3.2 Simple Voltage Reference

To construct a simple voltage reference, the circuit of Figure 6b can be loaded with a diode connected NFET. Such a voltage reference is shown in Figure 7.

The goal is to dimension the simple voltage reference such that $V_\mathrm{REF} = 1\,\mathrm{V}$.

1. Dimension the transistor M1 and calculate R_REF if we require $I_\mathrm{REF} = 10\,\mu\mathrm{A}$ and $V_\mathrm{dsat1} = -200\,\mathrm{mV}$. Use a minimum length transistor for M1. Dimension the transistor M2 such that

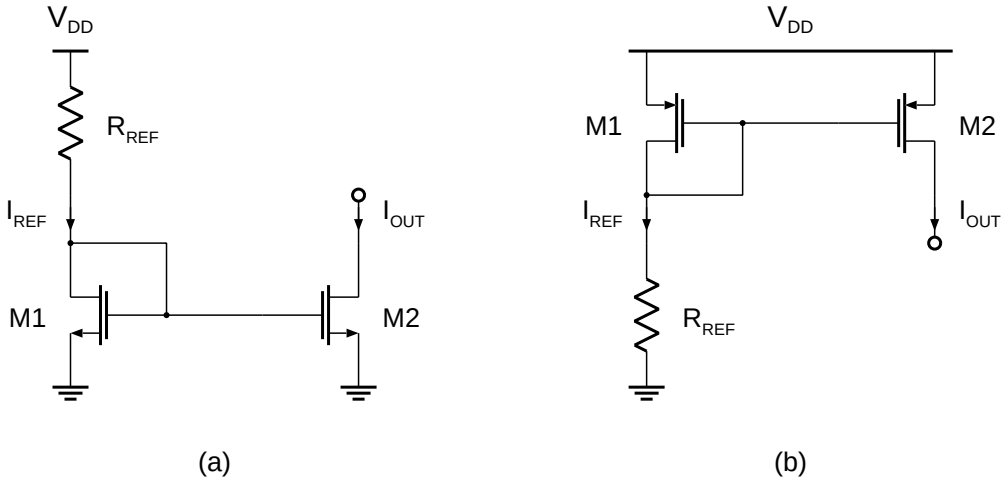

Figure 6: Current source in NMOS (a) and PMOS (b) configuration.

$I_{\mathrm{OUT}} = 100\,\mu\mathrm{A}$ ($N = 10$). Use $L_2 = 3.5\,\mu\mathrm{m}$ to increase the output resistance by a factor of 10 compared to a minimum length transistor. Calculate the width of transistor M3: assume a case A, where $L_3 = 0.35\,\mu\mathrm{m}$, and a case B, where $L_3 = 3.5\,\mu\mathrm{m}$.

2. Create a new cell `VoltageRef` and perform a DC simulation of the designed voltage reference (only for case B). Annotate the DC operating points in the schematic. Adjust the dimensions of M2 such that V_{REF} falls into the range of $\pm 1\%$ of its target value (only for case B).

3. For your adjusted dimensions vary R_{REF} by ± 20 %. How does the output voltage change for case A and B? Which one is preferable?

4. Now vary V_{DD} by $\pm 10\%$. How does the output voltage change for case A and B? Which one is preferable here?

4 Appendix

Transistor equations (valid in saturation region only)

$$I_{\mathrm{DS}} = \frac{k'_{[\mathrm{n,p}]}}{2}\frac{W}{L}\left(V_{\mathrm{GS}} - V_{\mathrm{TH[n,p]}}\right)^2 = \begin{cases} \text{positive} & \text{for NFET} \\ \text{negative} & \text{for PFET} \end{cases}$$

$$k'_{[\mathrm{n,p}]} = \mu_{\mathrm{eff[n,p]}} C_{\mathrm{ox}}$$

$$V_{\mathrm{TH[n,p]}} = V_{\mathrm{TH0[n,p]}} + \gamma_{[\mathrm{n,p}]}\left(\sqrt{\left|2\phi_{\mathrm{F[n,p]}} - V_{\mathrm{BS}}\right|} - \sqrt{\left|2\phi_{\mathrm{F[n,p]}}\right|}\right)$$

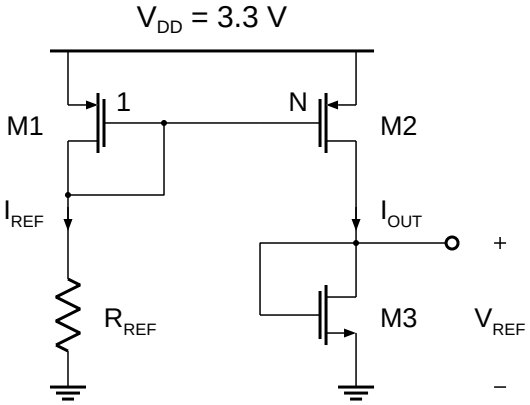

Figure 7: Simple voltage reference. (The bulk terminals of all PFETs are connected to V_{DD}.)

$$g_{\mathrm{m}} = k'_{[\mathrm{n,p}]}\frac{W}{L}\left(V_{\mathrm{GS}} - V_{\mathrm{TH[n,p]}}\right) = \sqrt{2k'_{[\mathrm{n,p}]}\frac{W}{L}I_{\mathrm{DS}}} = \frac{2I_{\mathrm{DS}}}{V_{\mathrm{GS}} - V_{\mathrm{TH[n,p]}}}$$

$$r_{\mathrm{out}} = \frac{L}{\lambda'_{[\mathrm{n,p}]}I_{\mathrm{DS}}}$$

$$\lambda'_{[\mathrm{n,p}]} = L\lambda_{[\mathrm{n,p}]}$$

$$C_{\mathrm{GS}} = \frac{2}{3}WLC_{\mathrm{ox}}$$

$$C_{\mathrm{ox}} = \frac{\epsilon_{\mathrm{ox}}}{t_{\mathrm{ox}}}$$

$$V_{\mathrm{DSAT}} = V_{\mathrm{GS}} - V_{\mathrm{TH[n,p]}}$$

Transistor parameters

3.3 V NFET		3.3 V PFET	
k'_{n}	$170\,\mu\mathrm{A/V^2}$	k'_{p}	$58\,\mu\mathrm{A/V^2}$
V_{TH0n}	$0.50\,\mathrm{V}$	V_{TH0p}	$-0.65\,\mathrm{V}$
γ_{n}	$0.58\,\mathrm{V}^{1/2}$	γ_{p}	$-0.40\,\mathrm{V}^{1/2}$
Φ_{Fn}	$0.44\,\mathrm{V}$	Φ_{Fp}	$0.42\,\mathrm{V}$
λ'_{n}	$0.0875\,\mu\mathrm{m/V}$	λ'_{p}	$0.0875\,\mu\mathrm{m/V}$
NFET and PFET			
ϵ_{ox}	$34.53\,\mathrm{pF/m}$	t_{ox}	$7.6\,\mathrm{nm}$

Table 1: Typical process parameters for the AMS C35 FETs.