TSMC Standard I/O Library

Application Note

Ver. 100

8/17/2001

Taiwan Semiconductor Manufacturing Co., Ltd.

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1. POWER ARRANGEMENT

1.1 I/O Power Rail Structure

Fig.1 is an example of the TSMC standard I/O layout to assist designers to understand the I/O power/ground rail configuration. Please refer to data books of the corresponding I/O library for more detailed description on power/ground rail separation scheme.

(1) Internal control and signal pins to core logics.

(2) Side port ***VDD***: connecting to the core power ring, for pre-driver.

(3) Side port ***VSS***: connecting to the core ground ring for pre-driver.

(4) Side port ***VD33*** (or ***VDDPST****): connecting to the I/O power ring for level-shifter and post-driver.

(5) Input diffusion resistor, guard ring, ESD circuit, pull-up/down and high-voltage tolerant logic.

(6) Double guard ring.

(7) Side port ***VSSPST***: connecting to the I/O ground ring for post-driver.

(8) I/O signal to connect to bonding pad.

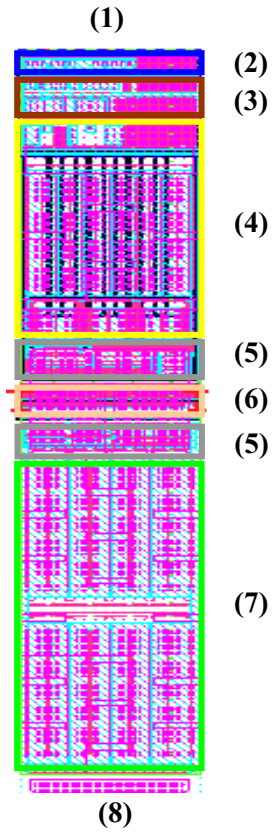

Fig. 1 I/O power rail structure

* Post driver power is named of VDDPST in 0.13um I/O libraries.

1.2 Power/Ground Cells and LVS Consideration

In TSMC IO, there are several power/ground cells to supply different voltage to the core, pre-divers, and the post-drivers. The global text is attached to the pad to separate multi-power/ground routing and for LVS (Layout Versus Schematic) consideration. The routing pin to the core side and the pad text attached for LVS are described in Table 1.

Table 1. Pins information of power/ground cells

Power/Ground cells	Connected to	Pin to core	Pad text for LVS
PVDD1DGZ	core cells + pre-drivers	**VDD**	**VDD:**
PVDD2DGZ	post-drivers	None	**VD33:** (or **VDDPST:**)
PVSS1DGZ	core cells + pre-drivers	**VSS**	**VSS:**
PVSS2DGZ	post-drivers	None	**VSSPST:**
PVSS3DGZ	all the transistors	**VSS**	**VSS:**

There are two ground schemes when using TSMC standard I/O library. Designers should use different power/ground cells and LVS SPICE netlist files for corresponding set. The first scheme separates the ground sources of (core cells + pre-drivers) and (post-drivers) as VSS and VSSPST to provide cleaner ground to the core. From Table 1, it takes ***PVDD1DGZ/PVSS1DGZ*** and ***PVDD2DGZ/PVSS2DGZ*** for this scheme and the SPICE netlist file for LVS takes ***<library_name>_1_2.spi***. Another scheme provides only one ground source to all transistors as VSS to save I/O bandwidth. According to Table 1, we still take ***PVDD1DGZ*** and ***PVDD2DGZ*** for multi-power, while only ***PVSS3DGZ*** for ground. The SPICE netlist file for LVS takes ***<library_name>_3.spi*** in this approach.

If most cases, the first scheme is suggested to provide better ground source as core and I/O area are separated. Even with limited package pins, designer can use double bonding for the adjacent PVSS1DGZ and PVSS2DGZ to a single package pin and reduce the noise to the core area. Scheme two is suggested only when ground noise is not critical in the extremely pad-limited design.

Note that there must be at least two kinds of power sources because the power

supply of core and I/O cells are in different voltage. That's why TSMC don't provide single power to supply both core cells and I/O cells. For LVS checking, designers should be careful in applying the SPICE netlist file according to their ground scheme. Table 2 shows the LVS files required for two different schemes.

Table 2. Ground schemes and the corresponding SPICE netlist for LVS

Ground Schemes	1st scheme	2nd scheme
Core cells + Pre-drivers	***PVDD1DGZ*** ***PVSS1DGZ***	***PVDD1DGZ*** ***PVDD2DGZ*** ***PVSS3DGZ***
Post-drivers	***PVDD2DGZ*** ***PVSS2DGZ***	
LVS SPICE netlist	***<library_name>_1_2.spi***	***<library_name>_3.spi***

2. FLEXIBLE BONDING STYLE - E-Z-BOND™

TSMC standard I/O can be easily applied to the design with different pad pitch by filling the appropriate pad filler cells (***PFEEDx***) in between the I/O cells. This is done by separated bonding pad and driving buffer. Since the driving buffer is quite slim, it is suitable for either staggered bonding or linear bonding style with two kinds of bonding pad cells (***PADIZx, PADOZx***). (The linear bond is also called "in-line" bond.) With this approach, users got the flexibility to attach the pads in desired pad pitches for either staggered or linear style. This flexible bonding style has been registered by TSMC as ***E-Z-Bond***™. Note that the minimum bounding pitch is constrained by the design rule that assembly houses and the probe card fabrication allowed. TSMC standard I/O follows the bonding rule of ***ASE***. Customers should double check the bonding rules with their assembly house. Fig.2 shows how to realize E-Z-Bond™. I/O filler cells connect the I/O buffers and should be inserted to increase the bonding pad pitch. The details of the two bonding styles are described below.

(1) Staggered Bond Style

Two different pads are used for staggered bonding. One is the outer pad ***PADOZx***, which is taller, and another is shorter, called the inner pad ***PADIZx.*** They are not embedded in the driving buffers because of the size difference. Users should attach appropriate bonding pads to the I/O driving buffers with the PR boundary aligned to each other. These bonding pads are placed in the repeated sequence of inner and outer ones. The pattern is repeated until all the bonding pads are placed.

(2) Linear Bond Style

For linear bond, only one type of bonding pad is selected to make an in-line pattern. We suggest ***PADIZx*** (or ***PADLZx***[†]) in chip size and EM (Electron Migration) concern. For details about EM effect, please refer to Chapter 4.

[†] These cells are provided in 0.13um I/O libraries for smaller in-line bonding pitch.

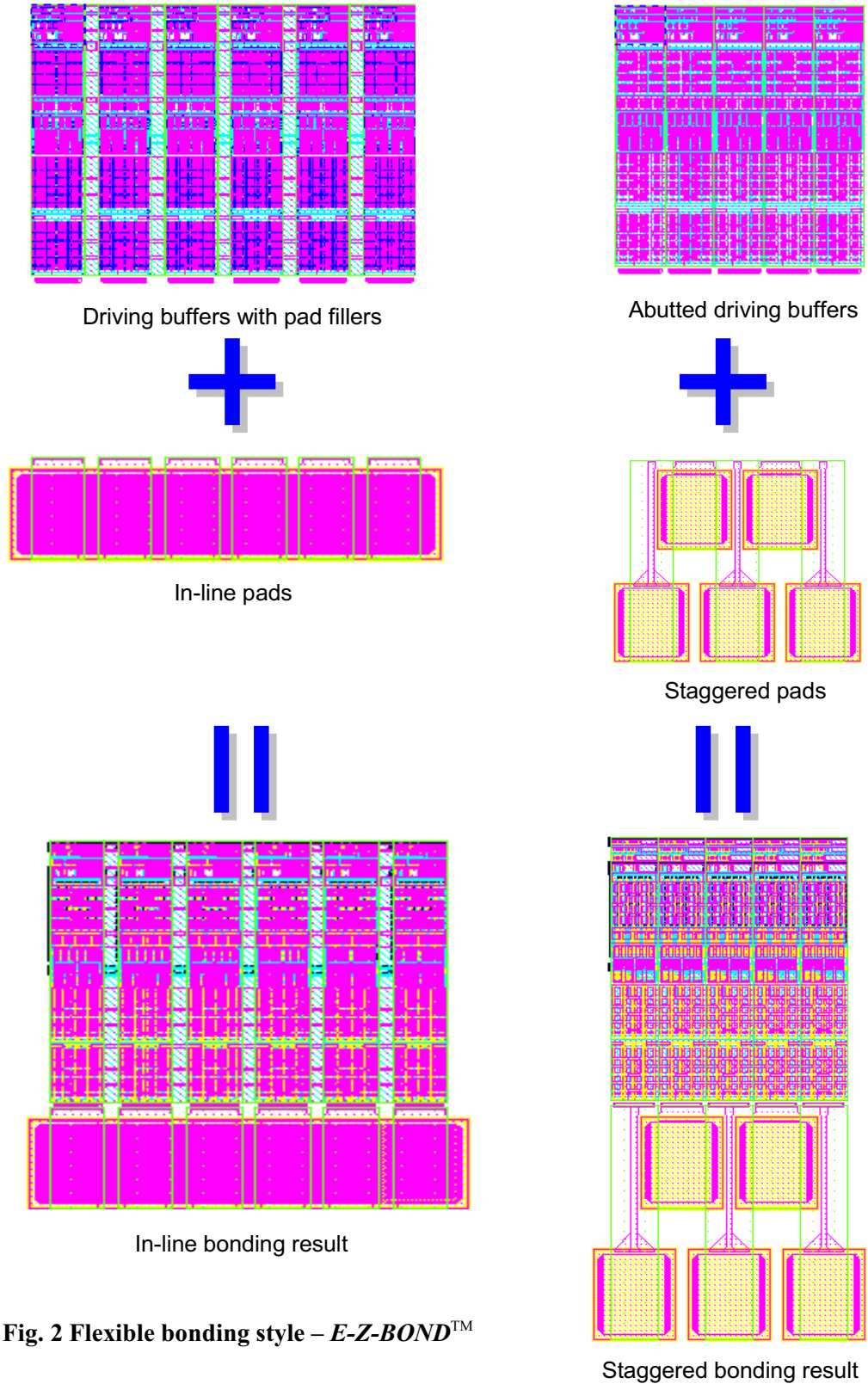

Fig. 2 Flexible bonding style – *E-Z-BOND*™

3. POWER UP SEQUENCE

In TSMC standard IO, different voltages are supplied to the pre-driver (lower voltage) and post-driver (higher voltage). Because of the multi-power ESD (Electro Static Discharge) structure, there is a parasitic forward diode path from core power rail (VDD) to I/O power rail (VD33 or VDDPST) as shown in Fig.3 the diode in red. So, if the core (lower) voltage is powered up earlier than the I/O (higher) voltage without care, there will be current flowing through the parasitic diode that may trigger latch-up. To avoid this problem, users can take either one of the approaches below.

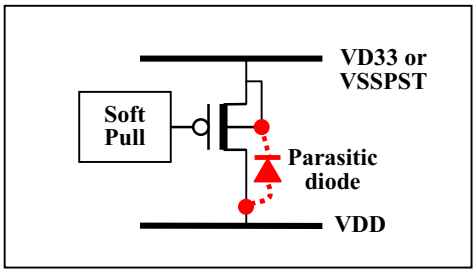

Fig. 3 Parasitic diode between core and I/O power rails

(1) Power Up Higher Voltage First

Turning on the higher voltage power first can prevent from the parasitic diode turning on. For example, power up VD33 (or VDDPST) first and then VDD. Note that TSMC don't recommend to power up higher voltage much earlier than lower one for reliability concern. That is because the un-powered VDD may result in short circuit current (crowbar current) on the post-driver for unknown state. Bus conflicting may also occur when only higher voltage is powered on. For customer who has great concern on short circuit current or bus contention in power up period (battery system for example), please contact TSMC filed AE for customized I/O service. Note that TSMC don't specify the maximum interval that lower voltage must be powered up after higher one because it depends on customers' application like the slew rate of ramping up.

(2) Place Schottcky Diode Between Powers

If we can ensure the parasitic diode does not turn on, we can even power up lower voltage first. This can be done by inserting an external diode between powers on the board as shown in Fig.4. By connecting the Schottcky diode with anode to lower voltage rail (VDD) and cathode to higher voltage rail (VD33 or VDDPST), we can force the latter to ramp up with the former by some voltage drop, which is less than the threshold voltage of the parasitic diode. This helps prevent from turning on the parasitic diode between power rails, hence avoiding the circuit to latch up. The external diode will be turned off when the higher voltage is powered up to its normal voltage. This approach requires an additional device on system board, so the cost could be a concern.

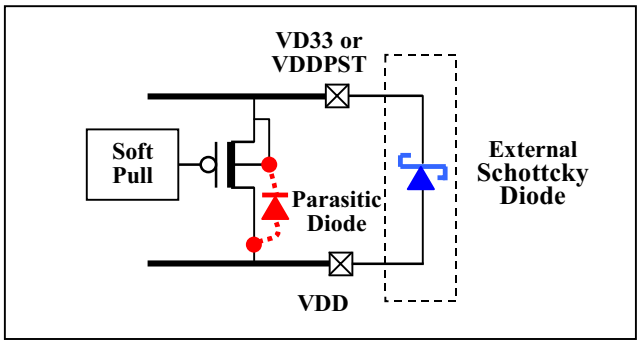

Fig. 4 Add external Schottcky diode to prevent from parasitic diode turning on

4. EM CONSIDERATION

4.1 Power/Ground Cells

TSMC standard I/O provides several sets of power/ground cells and bonding pads to provide current to the core or I/O area. To understand the maximum allowable current that the each power/ground cells and bonding pads can supply, users can check the layout with the ***EM*** (Electron Migration) criterion given in maximum current density (***Jmax***) table of the design rule document. The bottleneck may occur on certain metal routing, contact/via, or the connecting port metal width.

Users can get the corresponding maximum current table in the datasheet appendix of each I/O library. These data are useful in calculating the required number of power/ground cells to supply enough current to the core and I/O area with the estimated power consumption. Note that when calculating power/ground cell number for I/O area, designers should consider ***SSO*** (Simultaneously Switching Outputs) effect in addition to EM consideration. For details of SSO, please refer to Chapter 5.

Since EM is a reliability factor in chip manufacturing, it may not fail the chip at once but would degrade the performance as the run time grows. EDA tool analysis on current distribution and EM criterion is highly recommended to locate the possible EM weak point. If the tool is not available, layout review on the connecting port of power/ground cells is necessary especially on via number and metal width. Adding via array or stack metal can help increase maximum allowable current and release EM critical point.

4.2 Bonding Pads

For ***E-Z-Bond***™, users may have staggered or linear bond type. For staggered bonding style, care must be taken about the outer bonding pads' EM capability that might be the bottleneck of the current path. As to linear bond, since inner bound pad provide better EM capability with the increase of metal layer number, it's recommended to use inner bound pad for this bonding style. For the current supply capability of each bonding pads with different top metal layer, please refer to the tables in each I/O library datasheet.

4.3 Limited Power/Ground Bandwidth

For some designs with low-pin-count package, there could be only one or few pairs of power/ground pins that are not able to supply enough current and results in EM problem. Since the package pin count is limited, we suggest users to duplicate the power and ground I/O cells on the pad ring and apply double or even triple bonding to the same power or ground pin of the package. Fig.5 shows an example of duplicating and double bonding the core supplies. In this way, users may get the enough current supply from the limited power/ground bandwidth and also take the advantage of reduced wiring inductance from double bonding.

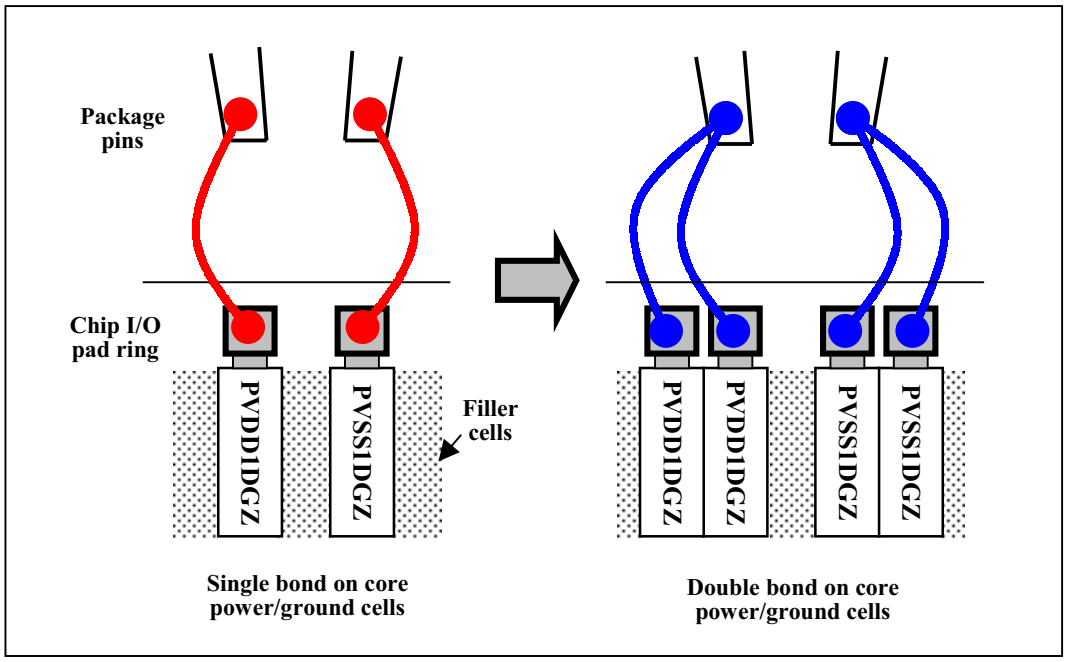

Fig. 5 Duplicate the power/ground cells and apply double bond to improve EM

5. SSO CONSIDERATION

5.1 Terminologies and Definitions

SSO: The abbreviation of "Simultaneously Switching Outputs", which means that a certain number of I/O buffers switching at the same time with the same direction (H ⇨ L, HZ ⇨ L or L ⇨ H, LZ ⇨ H). This simultaneous switching will cause noise on the power/ground lines because of the large di/dt value and the parasitic inductance of the bonding wire on the I/O power/ground cells.

SSN: The noise produced by simultaneously switching output buffers. It will change the voltage levels of power/ground nodes and is so-called "Ground Bounce Effect". This effect is tested at the device output by keeping one stable output at low "0" or high "1", while all other outputs of the device switch simultaneously. The noise occurred at the stable output node is called "Quiet Output Switching" (***QOS***). If the input low voltage is defined as ***Vil***, the QOS of "Vil" is taken to be the maximum noise that the system can endure.

DI: The maximum copies of specific I/O cell switching from high to low simultaneously without making the voltage on the quiet output "0" higher than "Vil" when single ground cell is applied. We take the QOS of "Vil" as criterion in defining DI because "1" has more noise margin than "0". For example, in LVTTL specification, the margin of "Vih" (2.0V) to VD33 (3.3V) is 1.3V in typical corner, which is higher than the margin of "Vil" (0.8V) to ground (0V).

DF: "Drive Factor" is the amount of how the specific output buffer contributes to the SSN on the power/ground rail. The DF value of an output buffer is proportional to dI/dt, the derivative of the current on the output buffer. We can obtain DF as:

$$DF = 1 / DI$$

SDF: "Sum of Drive Factors" accumulates the DF values of all the I/O cells within a group or the chip. SDF indicates the number of power/ground cell for I/O and is count on those cells switching simultaneously.

In SSO case,

Required number of ground cell for I/O = SDF

Required number of power cell for I/O = SDF / 1.1

In Non-SSO case, the required number of power/ground cell for I/O is less than the one in SSO case. We suggest (SDF/1.6) and (SDF/1.5) as a general rule for the number of power and ground cells, respectively.

5.2 SSO Simulation Model

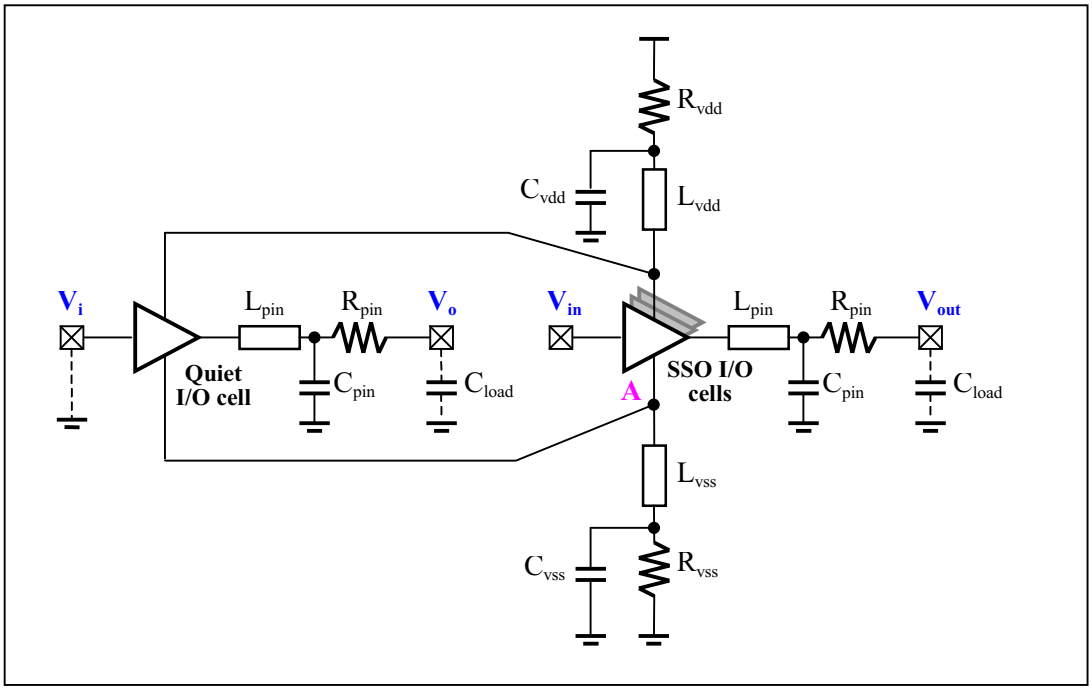

Fig. 6 The model for SSO simulations

As Fig.6 shows, each power/ground net and output node is modeled with individual RLC circuit according to the package type. V_{in} represents the input node of several SSO I/O cells. When V_{in} is toggling, all the SSO I/O cells are switching simultaneously and the change of the current (I) on L_{vss} could be high. So, the noise of $L_{vss}\times(dI/dt)$ is generated at node A. In the mean time, another quiet I/O cell grounded to node A is transmitting a "0" through V_o at the same time. The "0" could

be recognized as "1" if the noise at V_o is greater than Vil because of the raised reference voltage at node A. The minimum number of SSO I/O cells that contributes noise of "Vil" at V_o is characterized as DI and we can calculate DF accordingly.

The largest SSN happens in the best process corner, highest voltage applied and the lowest temperature. So, we characterize the corresponding DI based on the above conditions. Users can find the corresponding DF table in the appendix of each standard I/O library datasheet.

5.3 I/O Power/Ground Cell Number Calculation

From the DF table in datasheets of selected I/O library, users can easily calculate the required power/ground cell number for I/O in SSO or non-SSO cases. Here we show an example of the calculation.

(1) Check the DF value of each type of I/O cells

QOS of "Vil" is defined as failure criteria in SSO simulation. If four copies of the I/O cell with one ground cell (L_{vss}) caused noise of "Vil". The DI is 4 and the DF will be 1/4 = 0.25. Users can check the DF table in datasheet with their package wiring inductance (L_{vdd}, L_{vss}, L_{pin}).

(2) Calculate the SDF value of whole chip

Once we got the DF for various types of IO, we can sum them up to get the SDF. For example, if we got a design with ten 2mA buffers, six 8mA buffers, and twenty-six 24mA slew-rate-controlled buffers, what's the SDF value? Looking at the table, we have the corresponding DF of 2mA, 8mA, and 24mA cells as 0.012, 0.063, and 0.260 for wiring inductance of 7.8nH. We can calculate the SDF as

$$10 \times 0.012 + 6 \times 0.063 + 26 \times 0.260 = 7.258$$

(3) Obtain the required I/O power/ground cell number

The number of power/ground cells for I/O would be:

In SSO case,

ground cell number = 7.258 ⇨ 8

power cell number = 7.258 / 1.1 = 6.598 ⇨ 7

So, we need 8 ground cells and 7 power cells for I/O in SSO case.

In Non-SSO case,

ground cell number = 7.258 / 1.5 = 4.839 ⇨ 5

power cell number = 7.258 / 1.6 = 4.537 ⇨ 5

So, we need 5 ground cells and 5 power cells for I/O in Non-SSO case.

5.4 Time to Valid State

It's known that the SSN peak amplitude shall decrease with the time. If the design with simultaneously switching outputs does not have enough power/ground cells for I/O due to pin count restriction, designers should sampled the data after a period of time to ensure the correctness of the sampled data. We call this period of time as "time to valid state". There are look up tables in the datasheet of each I/O libraries to provide the timing required for SSO noise to settle down to the acceptable value (Vil) in case that the number of power/ground cell for I/O is not enough. Note that the table is characterized with only one pair of I/O power/ground cells.

5.5 Tips to Reduce SSN

1. Don't use stronger output buffers than what is necessary.
2. Use slew-rate controlled output cells wherever possible.
3. Insert the power and ground cells for I/O as many as possible. It is recommended to place the I/O power cell near the middle of the output buffers.
4. Place noise sensitive I/O cells (such as Oscillator I/O cells, analog I/O cells) away from SSO IOs.
5. Consider using double bonding on the same or duplicated power/ground cells to reduce inductance.

6. ESD CONSIDERATION

6.1 Dummy Power/Ground Cells Insertion

In TSMC standard I/O library, ESD clamping circuits are embedded in each of power/ground cell for full-chip ESD protection scheme as below.

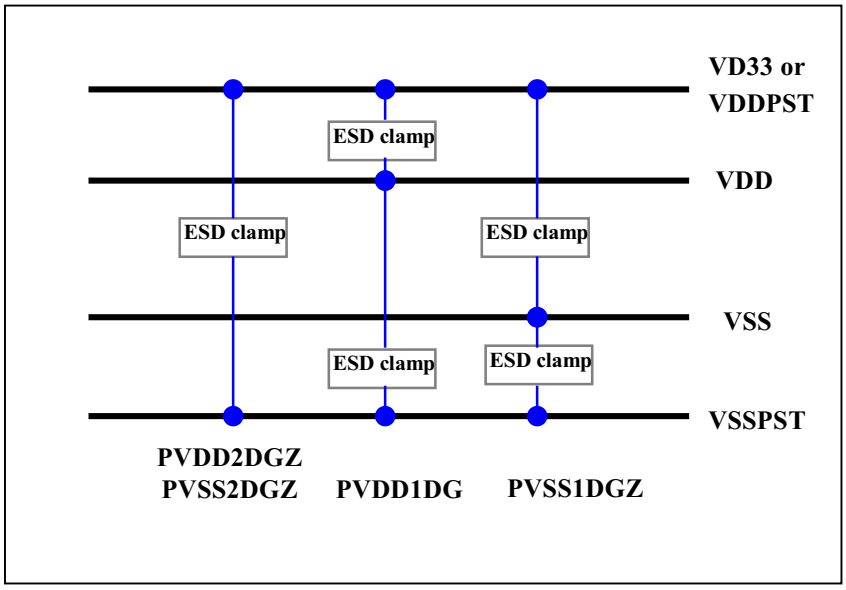

Fig. 7 The ESD protection scheme of power/ground cells

In ESD test model, we have HBM (human body model), MM (machine model) and CDM (charge device model). For HBM and MM, the test mode includes PD/PS (positive to VDD/VSS), ND/NS (negative to VDD/VSS), pin-to-pin (positive/negative), and power-to-ground (positive/negative). Many of them require the ESD discharge path from power (VD33 or VDDPST) to ground (VSSPST) rail. To provide the shortest ESD path, we strongly suggest users to put dummy power/ground cells on the I/O pad ring if there is space to. As shown in Fig.8, these dummy power/ground cells act just like fat filler cells. The benefit is that they provide the short ESD paths while filler cells don't. In the package phase, these power/ground cells are not bonded, so no impact to the total pin count. Please insert dummy PVDD2DGZ or PVSS2DGZ as many as possible to provide the better ESD protection scheme for different ESD test modes.

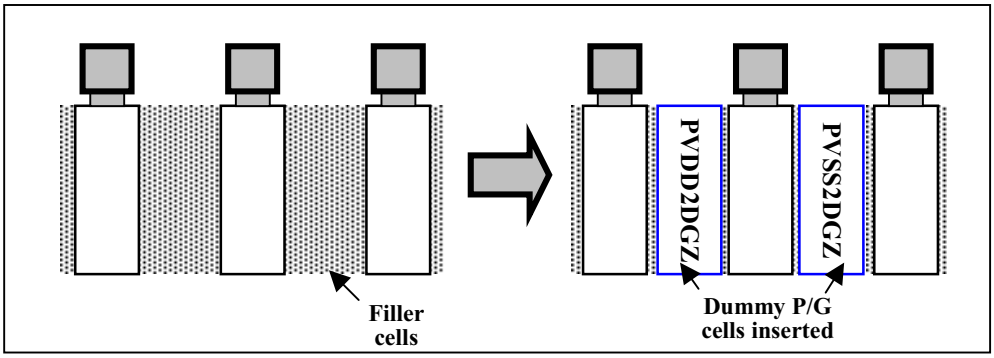

Fig. 8 Add dummy power/ground I/O cells for better ESD

6.2 Separated Power Domains

In the mixed-voltage design, there can be several I/O power domains with different voltages for either digital or analog I/O sections. The most straightforward approach is to cut the I/O pad ring into several sections but may result in poor ESD performance when ESD event occurs between the different power domains. TSMC provide a whole chip ESD protection scheme with so-called "power-cut I/O cell" to connect different power domains. In the power-cut cell, the I/O ground rails are connected by back-to-back diodes, while the I/O power rails are left open as shown in Fig.9. To provide an ESD discharge path between I/O power rails, please make sure there are PVDD2DGZ or PVSS2DGZ placed near the power-cut I/O cell in both sides. For the details of the usage of power-cut I/O cell between digital and analog power domains, please refer to "TSMC analog I/O application notes".

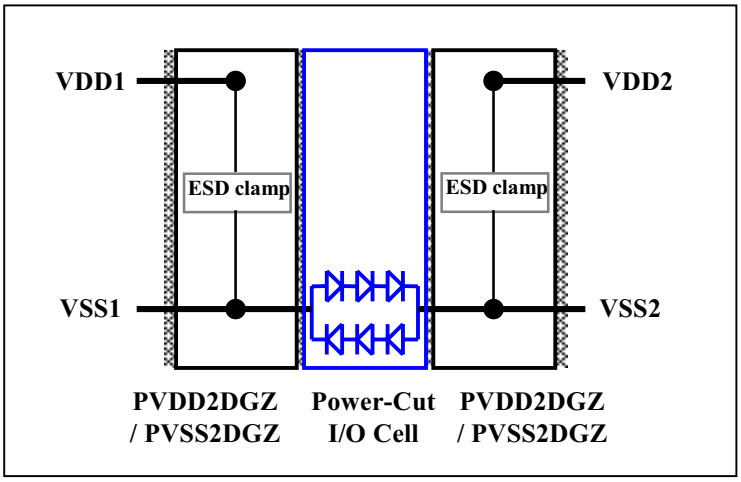

Fig. 9 The power-cut I/O cell provides ESD path for power domains

7. NO PIN I/O CELL USAGE

In TSMC standard I/O libraries, there are some I/O cells with no pin and requires special care in front-end and back-end kits usage. User can check the following for these no port cells.

7.1 Filler Cell and Corner Cell

If you check the front-end kits like Verilog and Synopsys, there are no filler cells (***PFEEDx***), nor the corner cell (***PCORNERx***). However, they exist in back-end kits like Apollo, Silicon Ensemble, and GDSII. The arrangement comes in that they got no pin, no transistor, no functions, but only for power/ground bus connection. Users should not include these cells in their netlist for simulation, but they should be instantiated when doing physical layout. For LVS, users don't need SPICE netlist to match layout because there is no transistor in these cells.

The principle of inserting filler cells is to put the slotted fillers as many as possible. A good reason to do so is there could be metal slot DRC violation with random filler insertion. Since the fat fillers always got slots, it's a good practice to insert fat fillers first and then the thinner ones. For some standard I/O libraries, only the fat filler cells like PFEED50, PFEED35, and PFEED22 got the metal slots. In this case, users should insert the fat fillers as many as possible before inserting other thinner ones.

7.2 I/O Power/Ground Cell

The purpose of I/O power/ground cells (PVDD2DGZ/PVSS2DGZ) is to supply the I/O pad ring. There is no pin on the phantom to connect to the core side. For front-end kits like Verilog and Synopsys, they are modeled as black box with no pin, no function to consist with back-end kits. Since there are ESD protection circuits embedded, the SPICE netlist is necessary for LVS check.

8. PULL-UP/DOWN I/O CELL USAGE

In TSMC standard I/O libraries, there are some cells with internal pull-up and pull-down. Because of high-voltage tolerant architecture as shown in Fig.10, these I/O cells are very weak pull-high to the “PAD” side, so we don’t recommend to use them as drivers during switching, neither to pull up the external loads. Another reason to discourage the usage above is that the pull-up/down resistance varies in a wide range depending on the process corners.

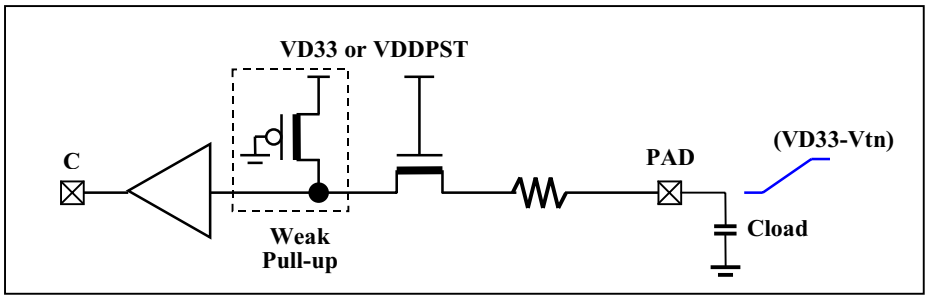

Fig. 10 Weak pull-up in high voltage tolerant architecture

The main purpose of TSMC pull-up/down IO is to tie the net connected to "C" port (the port connected to chip core) to a stable value when the PAD is unconnected. This is useful for some PADs such as "scan_in" which is used only during testing and not connected on the PCB. In such a case the unused PAD "scan_in" can be pulled-up/down to avoid a floating net on the chip core. Due to the reasons described above, the Verilog model for TSMC IOs with pull-up/down are modeled with the following properties:

When OEN=1 and no other driver is driving the "PAD" pin (pull-up/down situation), the model will have following behavior:

1) The effect of pull-up/down can’t go through the "PAD" pin. The "PAD" pin remains in the "Z" state.

2) The effect of pull-up/down can be seen on the "C" pin only after 10uS delay.

The purpose of this modeling is to discourage designers from using the effect of pull-up/down during signal switching or for pull-up/down of chip external loads. Electrically, the "PAD" pin may never reach the post-driver voltage (VD33 or VDDPST) for the high voltage tolerant architecture. A very long pull-up/down time for "C" pin is set because the timing of the pull-up/down cannot be guaranteed due to process variations.

If pull-up/down is needed for signal switching or for pull-up/down of external load, then it is recommended to add "external" pull-up/down resistors on the PCB. In that case, the effect of this external pull-up/down should be modeled in the Verilog test bench (which normally model the chip environment). If customers would like to have "internal" pull-up/down to drive external load, please do not use the standard pull-up/down cells and should contact your field AE for customized I/O service.

9. OSCILLATOR I/O CELL USAGE

There are several oscillator I/O cells in TSMC standard I/O library. Basically, they are designed to oscillate from 2MHz to 30MHz in fundamental mode. These cells are not designed to work in the KHz band oscillation. For the applications over 30MHz, please contact your field AE to get the recommendations.

Users should select the proper oscillator I/O cell according to their crystal or resonator specifications. The tank circuit for fundamental oscillation is provided only for reference. Notes for pin order check and back-annotation are also addressed in the following sections.

9.1 Select the Oscillator I/O cell

There are three sets of oscillator I/O cell, ***PDXO01DG/PDXOE1DG***, ***PDXO02DG/PDXOE2DG***, and ***PDXO03DG/PDXOE3DG***. Each set contains the cells with or without enable signal. The increasing number in the cell name indicates the growing driving strength and so does the small signal gain (g_m). To ensure the oscillation start up, the tank circuit must provide the negative resistance (***-Re***) at least five times the equivalent series resistance (***ESR***) of the crystal or resonator sample. The greater the negative resistance provided, the faster the crystal/resonator will start up. For the same load capacitance (***CL***), the higher g_m provides larger negative resistance and thus can start up the crystal with higher ESR, but the power consumption is also higher. Users should check the drive level (***DL***) specification of their sample to prevent from damaging the part.

To select the proper oscillator I/O cell, the specification of the applied crystal or resonator is important. The key parameters to start up are: CL and the maximum ESR in the target frequency. It is known that reducing the CL can help increase the negative resistance of the tank circuit, but if CL is too small, the deviation from the target frequency will increase because of the growing percentage of the capacitance variation. So, there is a trade-off between short start-up time and small frequency deviation in deciding CL value. The smaller ESR also helps reduce start-up time but

the price is usually higher. Once the CL and ESR are specified, users can check Table 3 for selection guide. Note this table is for reference and is applicable only when typical VD33 (or VDDPST) is 3.3V. Basically, if the start-up time is not critical, the smaller g_m set is preferred for less power consumption. Some conditions would require higher g_m set. For example, the application that is start-up time sensitive or the crystal (or resonator) got much higher CL (or ESR) compared to the table below. According to Table 3, if we have a 14.31818MHz crystal part with CL=12pF and maximum ESR=80Ω, set (I) is the first choice. However, if CL=32pF, then set (II) is recommended, especially when start-up time is also concerned. For advanced selection guide, please contact your local field AE.

Table 3. Selection guide of oscillator I/O cells for various frequencies

Target Freq (Hz)	*2M~3M*	*3M~6M*	*6M~10M*	*10M~20M*	*20M~30M*
CL (pF)	*32*	*20*	*16*	*12*	*10*
Maximum ESR (Ω)	*1K*	*400*	*100*	*80*	*40*
Osc I/O Sets	***(I)***	***(I) (II)***	***(I) (II)***	***(I) (II)***	***(II) (III)***

⇨ (I) PDXO01DG/PDXOE1DG, (II) PDXO02DG/PDXOE2DG, (III) PDXO03DG/PDXOE3DG

9.2 Oscillating Tank Circuits

Fig.11 shows the reference tank circuit for fundamental mode crystal oscillating. The circuit is to connect the oscillator I/O cell and some external component to ensure the oscillation start-up, and keep it stable and precise.

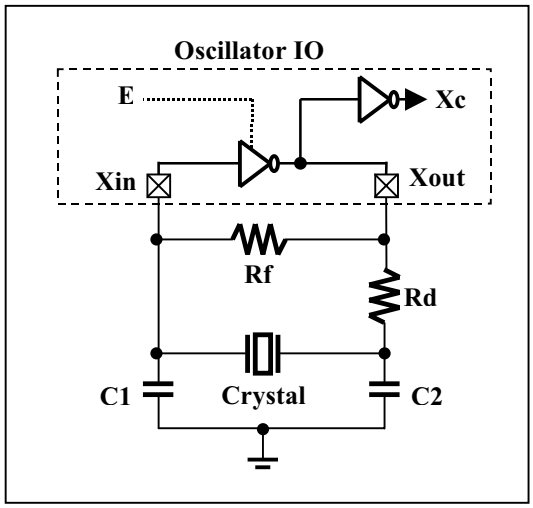

Fig. 11 Tank circuit for fundamental mode oscillation

From the figure above, there are several components that decide the behavior of oscillating and they affect the loop in many aspects. ***Rf*** represents the feedback resistor to bias the inverter in the high gain region. The Rf cannot be too low or the loop may fail to oscillate. Normally, Rf of 1MΩ is good enough for MHz band applications. ***Rd*** stands for the damping resistor that helps increase stability, save power and suppress the gain in the high frequency area. What paid of inserting Rd is the reduction of negative resistance. So, Rd cannot be too large, or the loop could fail to oscillate. Sometimes users may drop Rd in high frequency applications to reduce cost in production. ***C1*** and ***C2*** are decided according to the crystal or resonator CL specification. In the steady state of oscillating, CL is defined as (C1×C2)/(C1+C2). Actually, the I/O ports, bond pad, and package pin all contribute the parasitic capacitance to C1 and C2. So, we can rewrite CL to be $(C1^{*}\times C2^{*})/(C1^{*}+C2^{*})$, where $C1^{*}=(C1+C_{in,\ stray})$ and $C2^{*}=(C2+C_{out,\ stray})$. In this case, the required C1 and C2 will be reduced.

Note this tank circuit is for parallel resonate only since series resonate crystal needs no C1, C2 and no CL specified. Because C1, C2, Rd, and Rf vary with the crystal (or resonator) specifications and the selected oscillator IO cell, there is no magic number for each application. For the reference values, please contact your local field AE with the crystal specifications.

9.3 Note for Pin Order

There are two pins labeled "XIN" and "XOUT" for each oscillator I/O cell and the layout is symmetrical. Sometimes, it happens that the cell is mirrored and the pin order of "XIN" and "XOUT" is reversed. In this case, the LVS may not be able to warn about it. Though the mirrored oscillator I/O is functional equivalent but it could cause problem in test mode (bypass mode) that the external clock signal is supposed to trigger "XIN" not "XOUT". To prevent from this problem, pin order should be checked carefully when user is dropping text on the corresponding I/O pin.

9.4 Note for Back Annotation

For oscillator I/O cells, the XC output is derived from the XOUT through an inverting buffer as Fig.11 shows. So, the delay paths are characterized for

(A) XIN ⇨ XOUT and (B) XOUT ⇨ XC

Path delay for XIN ⇨ XC is calculated by the delay of (A) + (B). This characterization is required because XIN ⇨ XC delay is depending on both XOUT load and XC load. Synopsys is modeled as described above. That is, XIN ⇨ XOUT has one timing table and XOUT ⇨ XC has another timing table. If only one table of XIN ⇨ XC is used, the delay would depend only on XC load, which is not the real case. Here is a SDF example output by Synopsys:

```
IOPATH  XIN  XOUT  (A)  (A)  (A)
IOPATH  XOUT XC    (B)  (B)  (B)
```

The XIN ⇨ XC path delay will be (A+B) when back annotated to Synopsys.

Verilog cannot specify delays from output to output. All delay paths must be from input to output. Therefore, the timing path in Verilog is modeled as XIN ⇨ XC instead of XOUT ⇨ XC. This causes back-annotation problem when annotating delays with Synopsys SDF to Verilog. There will be message: "SDFA Error: Could not find path XOUT to XC". The workaround solution to this problem is to modify the SDF output from Synopsys as below and users can annotate this SDF correctly in Verilog.

```
IOPATH   XIN   XOUT   (A)     (A)     (A)
IOPATH   XIN   XC     (A+B)   (A+B)   (A+B)
```

10. OPEN DRAIN EMULATION

TSMC standard I/O does not provide open drain type I/O cells. However, users can emulate the open drain behavior with tri-state output IO. As Fig.12 shows, input port (I) is tied to ground “0”, and the output signal is connected to enable port (EN) to transfer a “0” or “Hi-Z” to the PAD. When EN=”0”, the output is enabled and the PAD is equal to I as “0”. When EN=”1”, the output is disabled (Hi-Z) and the PAD is pulled high by the external resistor Rx.

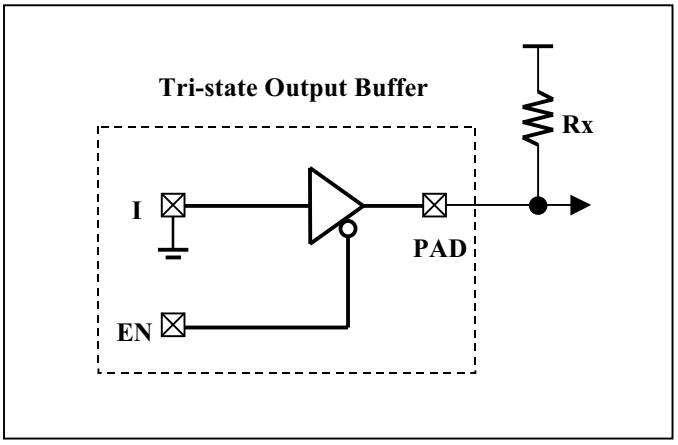

Fig. 12 The open drain emulation diagram

11. LIBRARY INTEGRATION NOTES

11.1 Library PVT Factors Integration

Due to library vendors could characterize their libraries in different process (P), voltage (V), and temperature (T), the blind integration of these PVT factors is very likely to cause inaccurate timing calculations in Synopsys because of derating. A common example is the integrating of I/O cell and core cell library. Because the I/O voltage and core voltage are different, users will suffer the unexpected voltage derating to the path delay no matter what operating condition is set. That's because Synopsys allow only one operating condition in one design, but there are many characterization (or nominal) conditions for each library, so derating happens. To solve this issue, users can comment the derating factors in each library as described in more details below.

(1) Voltage factor

Synopsys defined the characterizing voltage as "nom_voltage", representing for nominal voltage. For TSMC standard I/O library, the nom_voltage is VD33 (or VDDPST) in typical case (+/- 10% for best and worst case), while core cell library got lower nom_voltage as VDD. If users set the operating voltage different from the nom_voltage of the library, derating will be performed when <k_voltage_*> factors are specified in the library, and the path delay will increase by:

$$\Delta t_v = (V_{operating} - V_{nominal}) \times \text{<k\_voltage\_*>}$$

Note that the k factors of voltage are negative, so the higher the operating voltage, the smaller the path delay. For example, if we have a chip that integrate I/O and core libraries with nominal voltage of VD33 and VDD respectively, and we set the operating voltage to be VDD, the core cells timing won't be affected but the I/O cell timing will be over-estimated by the amount of (VDD-VD33)×<k_voltage_*>. So, no matter what operating condition is set, the mix-power applications always suffer from the unwanted derating with the voltage difference.

(2) Process factor

The similar problem happens to the characterizing process attribute, "nom_process". For different libraries, the number of nominal process may not be the same. Basically, we don't want the path delay to have process derating because we have characterized the timing in three corners. However, if the nominal process factors are different in libraries, Synopsys will perform derating with <k_process_*> no matter what operating condition is specified. The path delay will increase by:

$$\Delta t_p = (P_{operating} - P_{nominal}) \times \text{<k\_process\_*>}$$

For example, if users set the worst operating condition (WCCOM) according to the I/O library whose nom_process=1.188 and <k_process_*>=1. Then, no derating will be performed on the I/O path delay because the operating condition complies with the nominal process number of I/O library. However, if we integrate the core cell library with "nom_process=1.0, the path delay of the core cells will be derating with (1.188-1.0)×1=0.188; that is, the core cell path delay will be 18.8% worse than characterized, which is incorrect.

(3) Temperature factor

In Synopsys, "nom_temperature" represent the characterizing temperature. Various libraries could be characterized in different temperatures but Synopsys only allow one operating temperature being set. In this case, the temperature derating will be applied with <k_temp_*> factors and the path delay will increase by:

$$\Delta t_t = (T_{operating} - T_{nominal}) \times \text{<k\_temp\_*>}$$

For example, if there is one library characterized in 0ºC and another in –40ºC (best condition), setting the operating condition to 0ºC will change the timing of the –40ºC one and increase the path delay by (0-(-40))×0.00082=0.0328 for <k_temp_*>=0.00082.

(4) Solution

In most of the library integrating applications, users prefer no derating since all design-kits contains three timing files with tables characterized in each corner. To prevent Synopsys from performing unwanted derating, it's suggested to remove all derating factors defined in the libraries. This could be done with a single UNIX command below to eliminate k-factors and then compile it to db in Synopsys. For users who do not have Synopsys library compiler, please contact your local filed AE.

```
grep -v 'k_' <lib>.lib > <lib>_noderating.lib
```

For TSMC standard I/O library users, the k-factors are commented and thus no need to re-compile the db file. But users have to make sure all the k-factors in the other libraries are removed before performing synthesis or timing analysis.

11.2 Library Tape-out Layer Integration

With the progress of technology, the process steps and mask tooling become complicated and expensive. Users may suffer from the extra cost and schedule delay if the GDSII layers and mask tooling are not properly taped out. To correctly tape out with TSMC standard I/O library, users must refer to the corresponding "***Masking Layers & Bias***" document from TSMC online (Online ⇨ Foundry Design Documents Locator ⇨ Logic ⇨ Masking Layers & Bias) for the most updated mask tooling layers, digitized tone, and operation/bias equations. Here are some important notes that users must check before chip taping out. For more details, please check the "***Tape Out Layer Special Notes***" of each library for advanced information.

(1) GDSII number mapping

For the libraries from different vendors, the GDSII numbers defined for each process layer and dummy layers could be different. Please follow the definition in "***GDS Layer Usage Description File***" of the corresponding technology that is downloadable from TSMC online (Online ⇨ Technology Files Locator ⇨ Download Technology / Command Files ⇨ Layer mapping & Layout Editor Technology Files ⇨ GDS Layer Usage Description File). Mixing or wrong mapping GDSII layers could result in serious mask problem and silicon fail.

(2) OD mask

According to the "GDS Layer Usage Description File", there are two ways to define OD region in GDSII: one is to use DIFF, another is to use (PDIFF+NDIFF). Note that different libraries may have their preference and users must tape out all the GDSII layers related to OD mask or the chip may fail for that. So, it's suggested to tape out the OD layer with **(DIFF or PDIFF or NDIFF)** to ensure all the OD layout styles are covered to the OD mask tooling.

(3) LDD mask

Though users could find some polygons of LDD layers (say N3V, NLDDMV[‡]) in TSMC standard I/O cell, it's still recommended to use the logical operation defined in "Masking Layers & Bias" table to generate the LDD masks. That's because some other libraries may have no LDD layers drawn and taping out with drawing LDD will make the wrong mask.

(4) ESD mask

There are different GDSII layers defined for ESD implant masks (110) and (111). Though the ESD implant is optional in process steps, taping out the ESD mask (111) is strongly recommended to improve ESD margins. Please make sure all the ESD related GDSII layers are taped out correctly according to the "Masking Layers & Bias" table. For TSMC 0.13um standard I/O libraries, the special equation is required to generate ESD mask (111). Please check the release note for the special equation.

(5) Poly resistor

To ensure the poly resistance and SPICE model match to each other, there are some dummy layers (like DMN2V, DMP2V, or RHDMY[§]) to ensure/avoid the LDD pattern on the poly resistors. Users must check the "Masking Layers & Bias" table to tape out the corresponding dummy layer with TSMC standard I/O library.

(6) GDSII change to mask revision

Even the minor change of the GDSII layers may result in major change of masks, especially in base layers of process. For example, the modification of OD2 GDSII layer not only change the OD2 mask but also the other masks like LDD, POLY, RPO, ESD, and so on, depending on the technology. So, users must check the "Masking Layers & Bias" document to tape out all the masks related to the changing GDSII layers.

[‡] N3V polygon exists in 0.25um, 0.18um technologies, and NLDDMV polygon exists in 0.15um.

[§] DMN2V/DMP2V are used in 0.18um, 0.15um technologies to ensure LDD pattern, but RHDMY is used to avoid the LDD pattern in 0.13um technology.

12. CONTACT US

TSMC standard I/O libraries are released after passing the standard quality assurance (QA) procedure. The specific checking environment, including the EDA tool version and technology files are included in the released database. If users found any errors or encountered any problem with these models, please check the "release note" and "designkit.info" for the known issues first. Users should also make sure that their tool version, design rule manual, and DRC/LVS command files all comply with TSMC's QA condition. For advanced issues, please contact the distributor or TSMC local field AE.