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## TSMC 0.13 UM TECHNOLOGY OVERVIEW (MPW):

Technology	Logic	Logic	MS/RF	MS/RF
Geometry	0.13um	0.13um	0.13um	0.13um
Device Application	General Purpose	General Purpose	General Purpose	General Purpose
Core Voltage (V)	1.2	1.2	1.2	1.2
I/O Voltage (V)	2.5	3.3	2.5	3.3
Poly Layers	1	1	1	1
Metal Layers (Min)	3	3	3	3
Metal Layers (Max)	8	8	8	8
RO Speed (ps/gate)	19	19	19	19
BEOL Dielectric	FSG (k=3.6)	FSG (k=3.6)	FSG (k=3.6)	FSG (k=3.6)
BEOL Metal	CU	CU	CU	CU
PROCESS FEATURE				
Well Formation	Retrograde well	Retrograde well	SSR	SSR
Isolation	STI	STI	STI	STI
Gate Materials	Silicide	Silicide	Silicide	Silicide
Silicide Material	Co-salicide	Co-salicide	Co-Salicide	Co-Salicide
Gate Dielectric tox(core)	20A	20A	20	20
Gate Dielectric tox(I/O)	50A	70A	50	70
Emb-6T SRAM cell (um2)	2.43	2.43	2.43	2.43
DEVICE CHART (CORE)				
nMOS--Isat (uA/um)	535	535	535	535
nMOS--Vt(V)	0.34	0.34	0.34	0.34
nMOS--Ioff_max (nA/um)	1	1	1	1
pMOS--Idsat (uA/um)	235	235	235	235
pMOS--Vt(V)	-0.36	-0.36	-0.36	-0.36
pMOS--Ioff_max (nA/um)	1	1	1	1
DEVICE CHART (I/O)				
Vdd(V)	2.5	3.3	2.5	3.3
nMOS--Isat (uA/um)	620	590	620	590
nMOS--Vt(V)	0.48	0.61	0.48	0.61
nMOS--Ioff_max (nA/um)	0.1	0.1	0.1	0.1
pMOS--Idsat (uA/um)	285	315	285	315
pMOS--Vt(V)	-0.51	-0.61	-0.51	-0.61
pMOS--Ioff_max (nA/um)	0.1	0.1	0.1	0.1
MS/RF PROCESS MODULE				
Core transistor Vt	std-Vt, high-Vt, low-Vt	std-Vt, high-Vt, low-Vt	high, std, low, native	high, std, low, native
PiP	N/A	N/A	N/A	N/A
MiM	N/A	N/A	Q > 50 for C=0.9pf C=1.00pf/um^2 @2.4GHz	Q > 50 for C=0.9pf C=1.00pf/um^2 @2.4GHz
Inductor	N/A	N/A	3.0um(Cu) Q > 9 for L=4nH @2.4GHz	3.0um(Cu) Q > 9 for L=4nH @2.4GHz
Hi Resistors	N/A	N/A	1000ohm/sq	1000ohm/sq
Varactor	N/A	N/A	MOS and Junction Varactors available	MOS and Junction Varactors available
Triple well	N/A	N/A	Available	Available
BJT DEVICE				
Hfe	N/A	N/A	N/A	N/A

VA(V)	N/A	N/A	N/A	N/A
BV ceo(V)	N/A	N/A	N/A	N/A
Ft(GHz)	N/A	N/A	N/A	N/A
Fmax(GHz)	N/A	N/A	N/A	N/A
Ipeak(mA)	N/A	N/A	N/A	N/A
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Default # of masks (exclusive opt. masks)	36	36	23 (must) 12 (removable)	23 (must) 12 (removable)
# optional masks	8	8	+/-15 (for 1P8M)	+/-15 (for 1P8M)
All Optional masks	DNW,VTL_N,VTL_P, VTH_N,VTH_P,ESD, VIAD,MD,FW,PM	DNW,VTL_N,VTL_P, VTH_N,VTH_P,ESD, VIAD,MD,FW,PM	DNW,VTL_N,VTH_N, VTL_N2V,VTL_P, VTH_P,VTL_P2V,ESD, CTM,CBM,VIAD,MD, CBD,FW,PM	DNW,VTL_N,VTH_N, VTL_N2V,VTL_P, VTH_P,VTL_P2V,ESD, CTM,CBM,VIAD,MD, CBD,FW,PM
EP MPW optional masks	DNW,ESD,FW,PM	DNW,ESD,FW,PM	DNW,ESD,CTM,CBM, ,CBD,FW,PM	DNW,ESD,CTM,CBM, ,CBD,FW,PM
Made in Fab	Fab12 (12inch), Fab6 (8inch)	Fab12 (12inch), Fab6 (8inch)	Fab12 (12inch), Fab6 (8inch)	Fab12 (12inch), Fab6 (8inch)
Gate density (based on TSMC's standard cell library)	219 Kgate/mm²	219 Kgate/mm²	219 Kgate/mm²	219 Kgate/mm²
Available PDK for Cadence	1 PDK for Logic (CL013G) This PDK provide PDK for (CL013G + CL013LP + CM013G + CL013LV)		1 PDK for MS/RF (CR013G)	
Available PDK for Mentor	1 PDK available (CR013G) BUT not for RF process			