SECTION 2
Transmission Line Theory

Introduction

The ECLinPS family has pushed the world of ECL into the realm of picoseconds. When output transitions move into this picosecond region it becomes necessary to analyze system interconnects to determine if transmission line phenomena will occur. A handy rule of thumb to determine if an interconnect trace should be considered a transmission line is if the interconnect delay is greater than 1/8th of the signal transition time, it should be considered a transmission line and afforded all of the attention required by a transmission line. If this rule is applied to the ECLinPS product line a typical PCB trace will attain transmission line behaviors for any length >1/4″. Thus, a brief overview of transmission line theory is presented, including a discussion of distributed and lumped capacitance effects on transmission lines. For a more thorough discussion of transmission lines the reader is referred to Motorola's MECL Systems Design Handbook.

Background

Exact transmission line analysis can be both tedious and time consuming; therefore, assumptions for simplifying these types of calculations must be made. A reasonable assumption is that interconnect losses caused by factors such as bandwidth limitations, attenuation, and distortion are negligible for a typical PCB trace. The basis for this assumption is that losses due to the interconnect conductor are only a fraction of the total losses in the entire interface scheme. In addition, the conductivity of insulating material is very small; as a result, the dielectric losses are minimal. A second, and more fundamental, assumption is that transmission line behavior can be described by two parameters: line characteristic impedance (Z_O), and propagation delay (T_{PD})

Characteristic Impedance

An interconnect which consists of two conductors and a dielectric, characterized by distributed series resistances and inductances along with distributed parallel capacitances between them, is defined as a transmission line. These transmission lines exhibit a characteristic impedance over any length for which the distributed parameters are constant. Since the contribution of the distributed series resistance to the overall impedance is minimal, this term can be neglected when expressing the characteristic impedance of a line. The characteristic impedance is a dynamic quantity defined as the ratio of the transient voltage to the transient current passing through a point on the line. Thus, Z_O can be expressed in terms of the distributed inductance and capacitance of the line as shown by Equation 1.

$$Z_O=V/I=\sqrt{(L_O/C_O)} \qquad \text{(Equation 1)}$$

where:

L_O = Inductance per unit length (H)
C_O = Capacitance per unit length (F)

Propagation Delay

Propagation delay (T_{PD}) is also expressed as a function of both the inductance and capacitance per unit length of a transmission line. The propagation delay of the line is defined by the following equation:

$$T_{PD}=\sqrt{(L_O*C_O)} \qquad \text{(Equation 2)}$$

If L_O is expressed as microHenry's per unit length and capacitance as picoFarad's per unit length, the units for delay are nanoseconds per unit length. The propagation velocity is defined as the reciprocal of the propagation delay:

$$\nu=1/T_{PD}=1/\sqrt{(L_O*C_O)}$$

L_O and C_O can be determined using the easily measured parameters of line delay (T_D), line length (L), and the line characteristic impedance (Z_O) in conjunction with Equations 1 and 2. The propagation delay is defined as the ratio of line delay to line length:

$$T_{PD}=T_D/L$$

Combining equations 1 and 2 yields:

$$C_O=T_{PD}/Z_O \qquad \text{(Equation 3)}$$
$$L_O=T_{PD}*Z_O \qquad \text{(Equation 4)}$$

Termination and Reflection Theory

Figure 2.1 shows an ECLinPS gate driving a lossless transmission line of characteristic impedance Z_O, and terminated with resistance R_T. Modifying the circuit of Figure 2.1 such that the driving gate is represented by its equivalent circuit gives the configuration shown in Figure 2.2.

For a positive step function V_{IN}, a voltage step V_S, travels down the transmission line. The initial current in the transmission line is determined by the ratio V_S/Z_O. When the traveling wave arrives at the termination resistor R_T, Ohm's

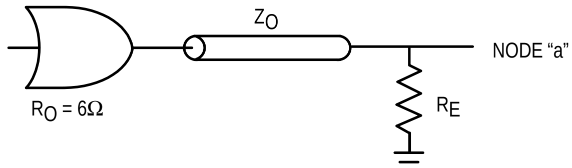

Figure 2.1. Typical Transmission Line Driving Scenario

Law must be maintained. If the line characteristic impedance and the termination resistance match (i.e. $Z_O=R_T$),the traveling wave does not encounter a discontinuity at the line-load interface; thus, the total voltage across the termination resistance is the incident voltage V_S. However, if mismatches between the line characteristic impedance and the termination resistance occur, a reflected wave must be set up to ensure Ohm's Law is obeyed at the line-load interface. In addition, the reflected wave may also encounter a discontinuity at the interface between the transmission line and the source resistance, thereby sending a re-reflected wave back towards the load. When neither the source nor the load impedance match the line characteristic impedance multiple reflections occur with the reflected signals being attenuated with each passage over the transmission line. The output response of this configuration appears as a damped oscillation, asymptotically approaching the steady state value, a phenomenon often referred to as ringing.

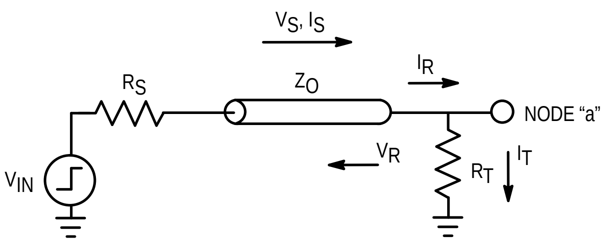

Figure 2.2. Thevenin Equivalent Circuit of Figure 2.1

In performing transmission line analysis, designers may encounter one of three impedance situations:

1. $R_S < Z_O$; $R_T \neq Z_O$
2. $R_S \leq Z_O$; $R_T = Z_O$
3. $R_S = Z_O$; $R_T \neq Z_O$

where:

R_S = Source Resistance

R_T = Termination Resistance

Case 1: $R_S < Z_O$; $R_T \neq Z_O$

The initial current in the transmission line is determined by the ratio V_S/Z_O. However, the final steady state current is determined by the ratio V_S/R_T, assuming ohmic losses in the transmission line are negligible. For case 1, an impedance discontinuity exists at the line-load interface which causes a reflected voltage and current to be generated at the instant the initial signal arrives at this interface. To determine the fraction of the traveling wave that will be reflected from the line-load interface, Kirchoff's current law is applied to node "a" in Figure 2.2. This results in the following:

$I_T = I_S + I_R$ where:

$I_T = V_T/R_T$

$I_S = V_S/Z_O$

$I_R = -V_R/Z_O$

Using substitution:

$$V_T/R_T = V_S/Z_O - V_R/Z_O \quad \text{(Equation 5)}$$

Since only one voltage can exist at node "a" at any instant in time:

$$V_T = V_S + V_R \quad \text{(Equation 6)}$$

Combining Equations 5 and 6, and solving for V_R yields:

$$(V_S + V_R)/R_T = V_S/Z_O - V_R/Z_O$$

$$V_R = ((R_T-Z_O)/(R_T+Z_O))*V_S$$

$$V_R/V_S = \rho_L = (R_T-Z_O)/(R_T+Z_O) \quad \text{(Equation 7)}$$

Therefore:

$$V_R = \rho_L*V_S$$

The term ρ_L referred to as the load reflection coefficient, represents the fraction of the voltage wave arriving at the lineload interface that is reflected back toward the source.

Similarly, a source reflection coefficient can be derived as:

$$\rho_S = (R_S-Z_O)/(R_s+Z_O) \quad \text{(Equation 8)}$$

From equations 7 and 8 it is apparent that multiple reflections will occur when neither the source nor the load impedances match the characteristic impedance of the line. A general equation for the total line voltage as a function of time and distance is expressed by Equation 9.

$$\begin{aligned} V(x,t) \quad & V_A(t)*[U(t-T_{PD}*x) + \rho_L*U(t-T_{PD}(2L-x) + \\ & \rho_L*\rho_S*U(t-T_{PD}(2L+x)) + \\ & (\rho_L**2)*(\rho_S*U(t-T_{PD}(4L-x)) + \\ & (\rho_L**2)*\rho_S**2)*U(t-T_{PD}(4L+x)) + \ldots] + \\ & V_{DC} \quad \text{(Equation 9)} \end{aligned}$$

where:

V_A = Voltage Entering the Transmission Line
T_{PD} = Propagation Delay of the Line
L = Total Line Length
x = Distance to an Arbitrary Point on the Line
V_{DC} = Initial Quiescent Voltage of the Line

Finally, the output voltage, V_T can be derived from the reflection coefficient by combining Equations 6 and 7:

$$V_T=(1+(R_T-Z_O)/(R_T+Z_O))*V_S$$

$$V_T=(2*R_T/(R_T+Z_O))*V_S$$

The two possible configurations for the Case 1 conditions are $R_T > Z_O$ and $R_T < Z_O$. The following paragraphs will describe these two conditions in detail.

Configuration 1: $R_T > Z_O$

For the case in which $R_T > Z_O$, ρ_L is positive, and the initial current at node “a” is greater than the final quiescent current:

$$I_{INITIAL} > I_{FINAL}$$

Hence:

$$V_S/Z_O) > (V_S/R_T)$$

Thus, a reflected current, I_R, must flow toward the source in order to attain the final steady state current as shown in Figure 2.3.

An example of a line mismatched at both ends, with the termination resistance greater than the load resistance is shown

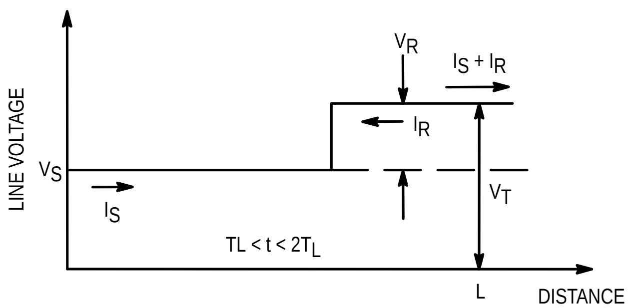

Figure 2.3. Reflected Voltage Wave for $R_T > Z_O$

in Figure 2.4. The initial steady state output voltage is given by:

$$V_{TI} = (65/71)^*(–1.75) = –1.60V$$

The final steady state output voltage is given by:

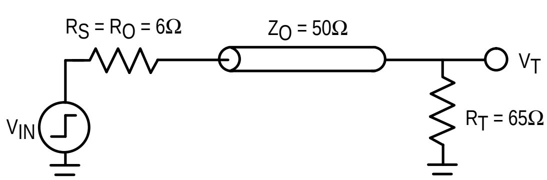

Figure 2.4. Transmission Line Model for $R_T > Z_O$

$$V_{TF} = (65/71)^*(– 0.9) = – 0.82V$$

The input voltage is a ramp from –1.75V to – 0.9V. The initial voltage traveling down the line is:

$$V_S = (50/56)^*0.85 = 0.76V$$

From Equations 7 and 8:

$$\rho_L = (R_T – Z_0)/(R_T+Z_0) = (65 – 50)/(65+50) = 0.13$$

$$\rho_S = (R_S – Z_0)/(R_S+Z_0) = (6 – 50)/(6+50) = – 0.79$$

From Equation 9, the output voltage V_T after one line delay is:

$$V_T(L,T_{PD}) = V_A(t)^*[1 + \rho_L] + V_{DC} = – 0.71V$$

Likewise, after a time equal to three times the line delay, the output voltage V_T is

$$V_T(L,3T_{PD}) = V_A(t)^*[\rho_L{}^*\rho_S + \rho_L{}^{**}2^*\rho_S] + V_T(L,T_{PD}) = – 0.83V$$

Additional iterations of Equation 9 can be performed to show that the ringing asymptotically approaches the final line voltage of – 0.82V. Ringing is a characteristic response for transmission lines mismatched at both ends with $R_T > R_O$. A SPICE representation of configuration 1 is illustrated in Figure 2.5.

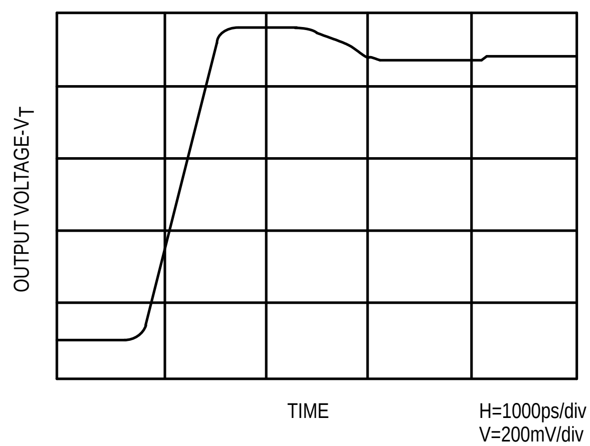

Figure 2.5. SPICE Results for Circuit of Figure 2.4

Configuration 2: $R_T < Z_O$

For the case in which $R_T<Z_O$, ρ_L is negative, and the initial current at node “a” is less than the final quiescent current.

$$I_{INITIAL} < I_{FINAL}$$

Hence:

$$(V_S/Z_O) < (V_S/R_T)$$

The reflected current, I_R, flows in the same direction as the initial source current in order to attain the final steady state current. The unique characteristic of configuration 2 is the negative reflection coefficient at both the source and load ends of the transmission line (Figure 2.6). Thus, signals approaching either end of the line are reflected with opposite polarity. In addition, the line voltage is a function of the pulse duration yielding steps of decreasing magnitude for input pulse durations greater than the line delay, and a series of attenuated pulses for input pulse durations less than the line delay.

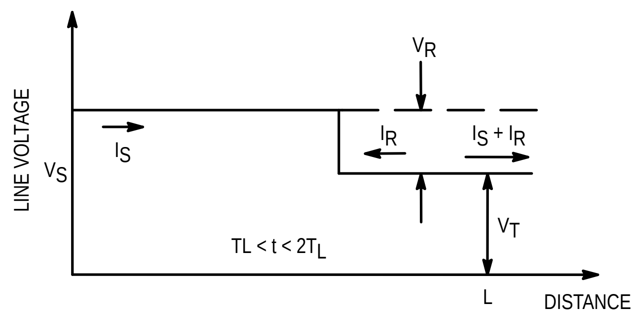

Figure 2.6. Reflected Voltage Wave for $R_T < Z_O$

An example of a line mismatched at both ends, with the termination resistance less than the line resistance, and the input pulse width greater than the line delay is shown in Figure 2.7.

The initial steady state output voltage is defined as:

$V_{TI} = (35/41)^*(–1.75) = –1.49V$

The final steady state output voltage is given by

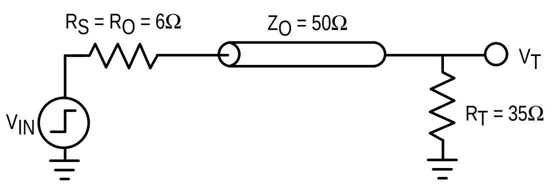

Figure 2.7. Transmission Line Model for $R_T < Z_O$

$V_{TF} = (35/41)^*(– 0.9) = – 0.77V$

For an input pulse from –1.75V to – 0.9V the initial voltage traveling down the line is:

$V_S = (50/56)^*0.85 = 0.76V$

From Equations 7 and 8,

$\rho_L = (35 – 50)/(35+50) = – 0.18$

$\rho_S = (6 – 50)/(6+50) = – 0.79$

From Equation 9, the output voltage V_T after one line delay is:

$V_T(L,T_{PD}) = V_A(t)^*[1 + \rho_L] + V_{DC} = – 0.87V$

Likewise, after a time equal to three times the line delay, the output voltage V_T is:

$V_T(L,3T_{PD})=V_A(t)^*[\rho_L{}^*\rho_L+\rho_L{}^{**}2^*\rho_S]+V_T(L,T_{PD})=$ –0.78V

Additional iterations of Equation 9 can be performed to show that the output response asymptotically approaches – 0.77 volts. Stair-steps are characteristic responses for transmission lines mismatched at both ends with $R_T < Z_O$, and a pulse width greater than the line delay. Figure 2.8 shows the results of a SPICE simulation for the case described by configuration 2.

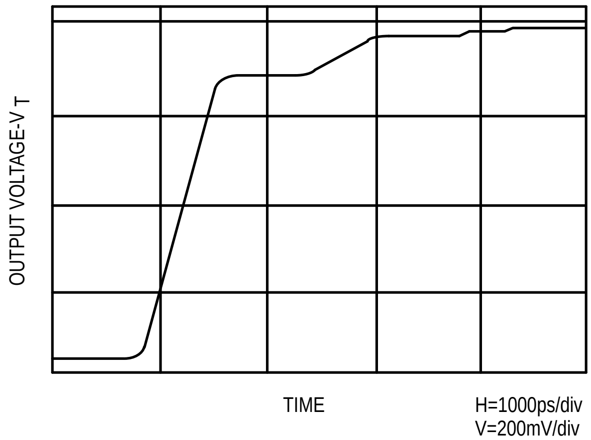

Figure 2.8. SPICE Results for Circuit of Figure 2.7 with Input Pulse Width > Line Delay

Figure 2.9 shows the line response for the same circuit as above, but for the case in which the input pulse width is less than the line delay. As in the previous example, the initial steady state voltage across the transmission line is –1.49 volts, and the reflection coefficients are – 0.18 and – 0.79 for the load and source respectively. However, the intermediate voltage across the transmission line is a series of positive-going pulses of decreasing amplitude for each round trip of the reflected voltage, until the final steady state voltage of 1.49 volts is reached.

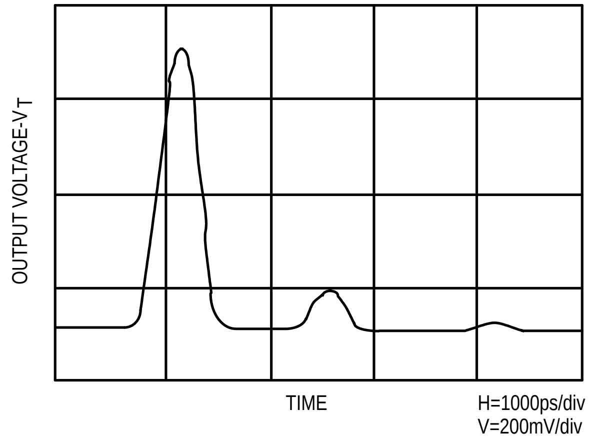

Figure 2.9. SPICE Results for Circuit of Figure 2.7 with Input Pulse < Line Delay

Shorted Line

The shorted line is a special case of configuration 2 in which the load reflection coefficient is –1.0, and the reflections tend toward the steady state condition of zero line voltage and a current defined by the source voltage and the source resistance.

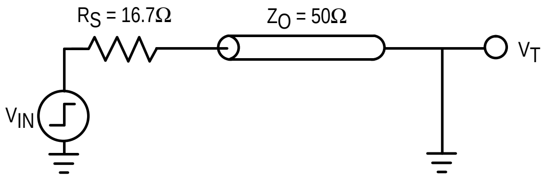

Figure 2.10. Transmission Line Model for Shorted Line

An example of a shorted line is shown in Figure 2.10. The transmission line response for the case in which the input pulse width is greater than the line delay is shown in Figure 2.11. The initial and final steady state voltages across the transmission line are zero. The source is a step function with a 0.85 volt amplitude. The initial voltage traveling down the line is:

$$V_S = (50/66.7)^*0.85 = 0.64V$$

From Equations 7 and 8,
ρ_L = (0–50)/(0+50) = –1

$$\rho_S = (16.7–50)/(16.7+50) = – 0.5$$

Upon reaching the shorted end of the line, the initial voltage waveform is inverted and reflected toward the source. At the source end, the voltage is partially reflected back toward the shorted end in accordance with the source reflection coefficient. Thus, the voltage at the shorted end of the transmission line is always zero while at the source end, the voltage is reduced for each round trip of the reflected voltage. The voltage at the source end tends toward the final steady state condition of zero volts across the transmission line. The values of the source and line characteristic impedances in this example are such that the amplitude decreases by 50% with each successive round trip across the transmission line.

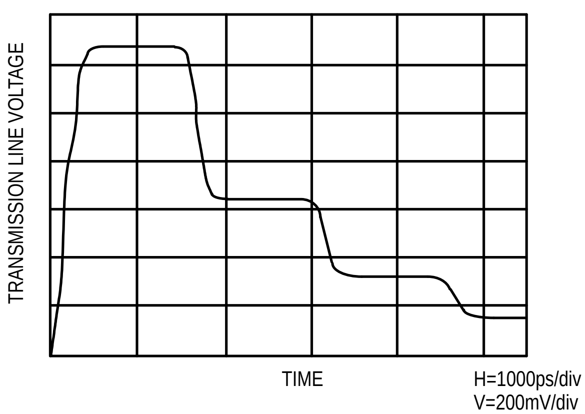

Figure 2.11. SPICE Results for Shorted Line with the Input Pulse Width > Line Delay

Figure 2.12 shows the line response for the same circuit as above, but for the case in which the input pulse width is less than the line delay. As in the previous example, the initial and final steady state voltages across the transmission line are zero, and the reflection coefficients are –1.0 and – 0.5 for the load and source respectively. However, the intermediate voltage across the transmission line is a series of negative pulses with the amplitude of each pulse decreasing for each round trip of the reflected voltage until the final steady state voltage of zero volts is attained. Again, for this example, the amplitude of the output response decreases by 50% for each successive reflection

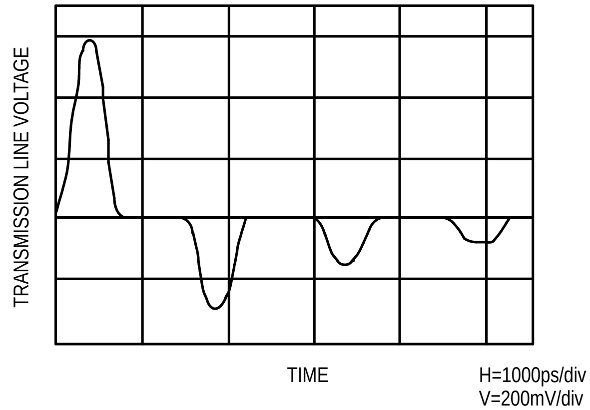

Figure 2.12. SPICE Results for Shorted Line with the Input Pulse Width < Line Delay

due to the choice of source and transmission line characteristic impedances.

Case 2: $R_S \le Z_O$; $R_T = Z_O$

As in Case 1, the initial current in the transmission line is determined by the ratio of V_S/Z_O. Similarly, since $R_T = Z_O$ the final steady state current is also determined by the ratio V_S/Z_O. Because a discontinuity does not exist at the line-load interface, all the energy in the traveling step is absorbed by the termination resistance, in accordance with Ohm's Law. Therefore, no reflections occur and the output response is merely a delayed version of the input waveform.

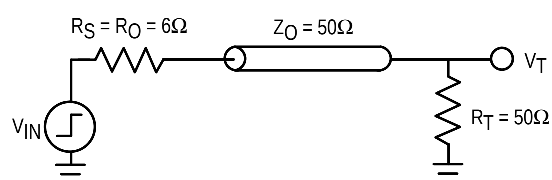

Figure 2.13. Transmission Line Model for Matched Termination

An example of a line mismatched at the source but matched at the load is shown in Figure 2.13. For an input pulse of –1.75V to – 0.9V is given by:

$$V_{TI} = (50/56)^*(–1.75) = –1.56V$$

The final steady state output voltage is given by

$$V_{TF} = (50/56)^*(– 0.9) = – 0.80V$$

The source is a step function with an 0.85 volt amplitude. The initial voltage traveling down the line is:

$$V_S = (50/56)^*0.85 = 0.76V$$

From Equations 7 and 8,

$\rho_L = (50–50)/(65+50) = 0$

$\rho_S = (6–50)/(6+50) = – 0.79$

From Equation 9, the output voltage V_T after one line delay is:

$V_T(L,T_{PD}) = V_A(t)^*[1 + \rho_L] + V_{DC} = – 0.80V$

Likewise, after a time equal to three times the line delay, the output voltage V_T is:

$V_T(L,3T_{PD}) =$
$V_A(t)^*[\rho_L{}^*\rho_S + \rho_L{}^{**}2^*\rho_S] + V_T(L,T_{PD}) = – 0.80V$

Thus, the output response attains its final steady state value (Figure 2.14) after only one line delay when the termination

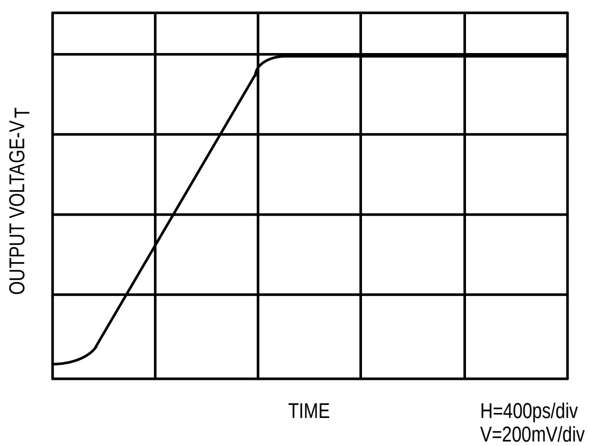

Figure 2.14. SPICE Results for Matched Termination

resistance matches the line characteristic impedance. Ringing or stair-step output responses do not occur since the load reflection coefficient is zero.

Case 3: $R_S = Z_O$; $R_T = Z_O$

When the termination resistance does not match the line characteristic impedance reflections arising from the load will occur. Fortunately, in case 3, the source resistance and the line characteristic impedance are equal, thus, the reflection coefficient is zero and the energy in these reflections is completely absorbed at the source; thus, no further reflections occur.

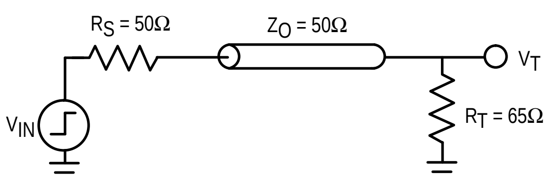

Figure 2.15. Transmission Line Model for $V_S = Z_O$

An example of a line mismatched at the load but matched at the source is shown in Figure 2.15. For an input pulse of –1.75V to – 0.9V the initial steady state output voltage is given by:

$V_{TI} = (65/115)^*(–1.75) = – 0.99V$

The final steady state output voltage is given by

$V_{TF} = (65/115)^*(– 0.9) = – 0.51V$

The source is a step function with a 0.85 volt amplitude. The initial voltage traveling down the line is:

$V_S = (50/100)^*0.85 = 0.43V$

From Equations 7 and 8,

$\rho_L = (65–50)/(65+50) = 0.13$

$\rho_S = (50–50)/(50+50) = 0$

From Equation 9, the output voltage V_T after one line delay is:

$V_T(L,T_{PD}) = V_A(t)^*[1 + \rho_L] + V_{DC} = – 0.51V$

Likewise, after a time equal to three times the line delay, the output voltage V_T is:

$V_T(L,3T_{PD}) = V_A(t)^*[\rho_L{}^*\rho_S + \rho_L{}^{**}2^*\rho_S] + V_T(L,T_{PD}) =$
$– 0.51V$

Thus, the output response attains its final steady state value after one line delay when the source resistance matches the line characteristic impedance. Again, ringing or a stair-step output does not occur since the load reflection coefficient is zero (Figure 2.16).

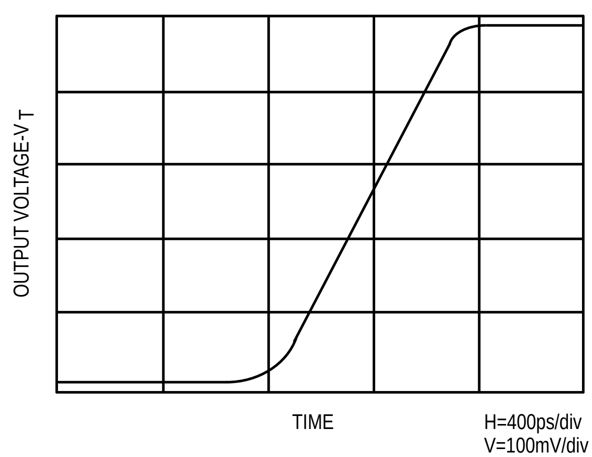

Figure 2.16. SPICE Results for Circuit of Figure 2.15

Series Termination

Series termination represents a special subcategory of Case 3 in which the load reflection coefficient is +1 and the source resistance is made equal to the line characteristic impedance by inserting a resistor, R_{ST}, between and in series with, the transmission line and the source resistance R_O. The reflections tend toward the steady state conditions of zero current in the transmission line, and an output voltage equal to the input voltage. This type of termination is illustrated by the circuit configuration of Figure 2.17. The initial voltage down the line will be only half the amplitude of the input signal due to the voltage division of the equal source and line impedances.

$V_S = (Z_O/(2^*Z_O))^*V_{IN} = V_{IN}/2$ (Equation 10)

The load reflection coefficient tends to unity, thus, a voltage wave arriving at the load will double in amplitude, and a reflected wave with the same amplitude as the incident wave

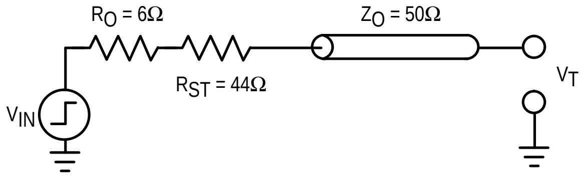

Figure 2.17. Series Terminated Transmission Line

will be reflected toward the source. Since the source resistance matches the line characteristic impedance all the energy in the reflected wave is absorbed, and no further reflections occur. This "source absorption" feature reduces the effects of ringing, making series terminations particularly useful for transmitting signals through a backplane or other interconnects where discontinuities exist.

As stated previously, the signal in the line is only at half amplitude and the reflection restores the signal to the full amplitude. It is important to ensure that all loads are located near the end of the transmission line so that a two step input signal is not seen by any of the loads.

For the series terminated circuit of Figure 2.17 with R_O + $R_{ST} = Z_O$ and an input pulse rising from –1.75V to – 0.9V, the initial line voltage, V_{TI} is –1.325V and the final line voltage, V_{TF}, is – 0.9V. The source is a step function with a 0.85 volt amplitude. The initial voltage traveling down the line is:

$V_S = (50/100)^*0.85 = 0.43V$

From Equations 7 and 8,

$\rho_L = (\infty - 50)/(\infty+50) = 1$

$\rho_S = (50 - 50)/(50+50) = 0$

From Equation 9, the output voltage V_T after one line delay is:

$V_T(L,T_{PD}) = V_A(t)^*[1 + \rho_L] + V_{DC} = - 0.9V$

Likewise, after a time equal to three times the line delay, the output voltage V_T is:

$V_T(L,3T_{PD}) = V_A(t)^*\rho_L{}^*\rho_S + \rho_L{}^{**}2^*\rho_S] + V_T(L,T_{PD}) = - 0.9V$

Since the load reflection coefficient is unity, the voltage at the output attains the full ECL swing, whereas the voltage at the beginning of the transmission line does not attain this level until the reflected voltage arrives back at the source termination (Figures 2.17 and 2.18). No other reflections occur because the source impedance and line characteristic impedance match.

Capacitive Effects on Propagation Delay

Lumped Capacitive Loads

The effect of load capacitance on propagation delay must

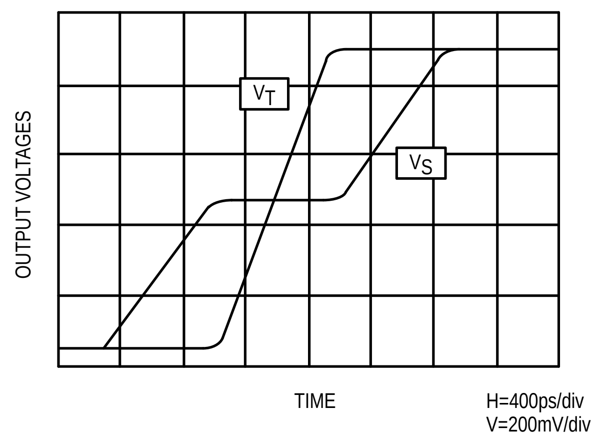

Figure 2.18. SPICE Results for Series Terminated Line

be considered when using high performance integrated circuits such as the ECLinPS family. Although capacitive loading affects both series and parallel termination schemes, it is more pronounced for the series terminated case. Figure 2.19a illustrates a series terminated line with a capacitive load C_L. Under the no load condition, C_L=0, the delay between the 50% point of the input waveform to the 50% point of the output waveform is defined as the line delay T_D. A capacitive load

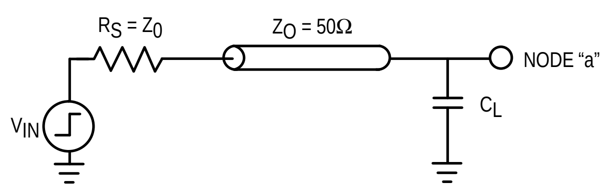

Figure 2.19a. Lumped Load Transmission Line Model

placed at the end of the line increases the rise time of the output signal, thereby increasing TD by an amount ΔT_D (Figure 2.19b). Figure 2.20 shows the increase in delay for load capacitances of 0, 1, 5, 10 and 20 picoFarads.

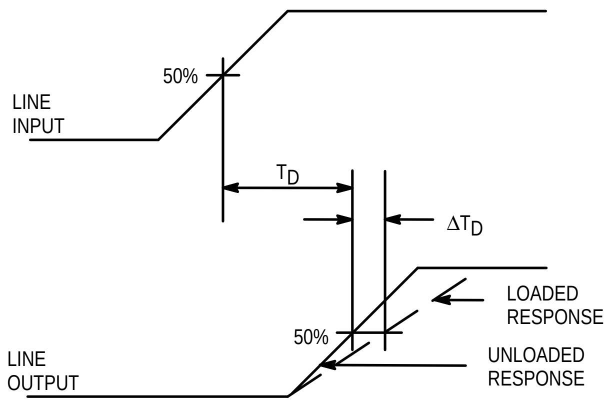

Figure 2.19b. ∆TD Introduced by Capacitive Load

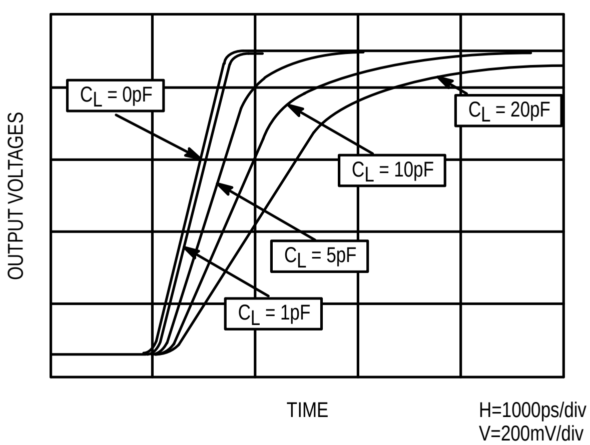

Figure 2.20. Line Delay vs Lumped Capacitive Load

The increase in propagation delay can be determined by using Thevenin's theorem to convert the transmission line into a single time constant network with a ramp input voltage. The analysis applies to both series and parallel terminations, since both configurations can be represented as a single time constant network with a time constant, τ, and a Thevenin impedance Z'.

Figure 2.21 shows the Thevenized versions for the series and parallel terminated configurations. The Thevenin impedance for the series configuration is approximately twice that for the parallel terminated case, thus the time constant will be two times greater for the series terminated configuration. Since τ is proportional to the risetime, the rise time will also be two times greater; thus the reason for the larger impact of capacitive loading on the series terminated configuration.

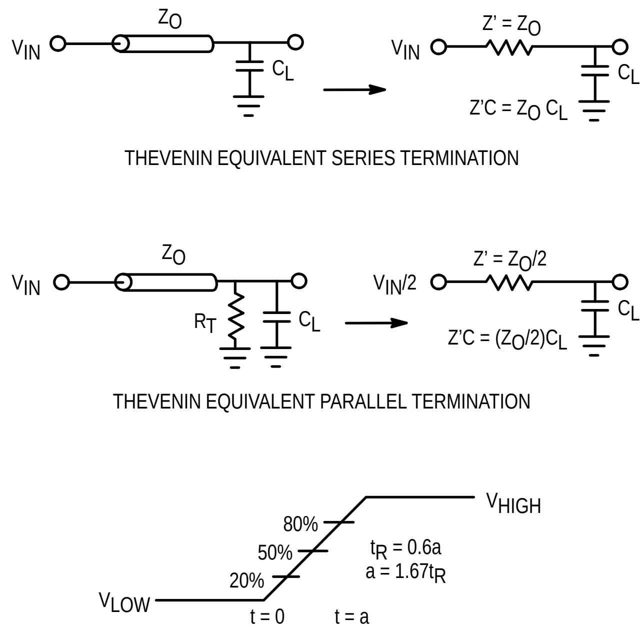

Figure 2.21. Thevenin Equivalent Lumped Capacitance Circuits

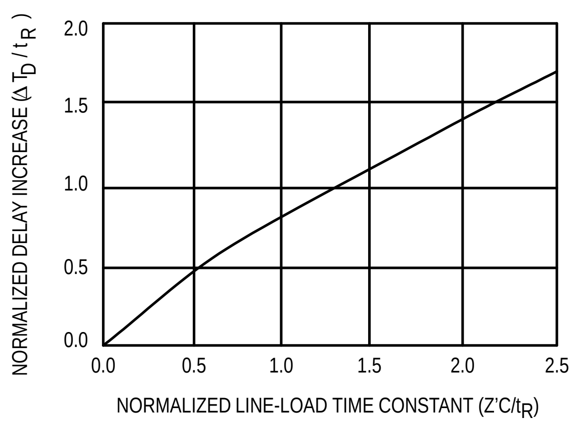

Figure 2.22. Normalized Delay Increase Due to Lumped Capacitive Load

The relationship between the change in delay and the line-load time constant is shown in Figure 2.22. Both the delay change (ΔT_D) and the line-load time constant (Z'C) are normalized to the 20–80% risetime of the input signal. This chart provides a convenient graphical approach for approximating delay increases due to capacitive loads as illustrated by the following example.

Given a 100Ω series terminated line with a 5pF load at the end of the line and a no load rise time of 400ps, the increase in delay, ΔT_D, can be determined using Figure 2.22. The normalized line-load time constant is:

$Z'C/t_R = 100\Omega * 5pF/400ps = 1.25$

Using this value and Figure 2.22:

$\Delta T_D/t_R = 0.9$

Therefore:

$\Delta T_D = 0.9^* 400ps = 360ps$

Thus, 360ps is added to the no load delay to arrive at the approximate delay for a 5pF load. For a 100Ω line employing a matched parallel termination scheme, Z' = 50Ω, the added delay is only 240ps. This added delay is significantly less than the one encountered for the series terminated case.

Thus, when critical delay paths are being designed it is incumbent on the designer to give special consideration to the termination scheme, lumped loading capacitance and line impedance to optimize the delay performance of the system.

Distributed Capacitive Loads

In addition to lumped loading, capacitive loads may be distributed along transmission lines. There are three consequences of distributed capacitive loading of transmission lines: reflections, lower line impedance, and increased propagation delay. A circuit configuration for observing distributed capacitive loading effects is shown in Figure 2.23.

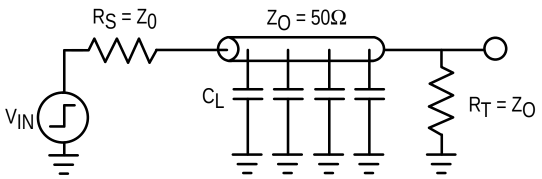

Figure 2.23. Transmission Line Model for Distributed Capacitive Load

Each capacitive load connected along a transmission line causes a reflection of opposite polarity to the incident wave. If the loads are spaced such that the risetime is greater than the time necessary for the incident wave to travel from one load to the next, the reflected waves from two adjacent loads will overlap. Figure 2.24 shows the output response for a transmission line with two distributed capacitive loads of 2.0pF separated by a line propagation time of 750ps. The upper trace, with a 20–80% input signal risetime of 400ps, shows two distinct reflections. The middle and lower traces with 20–80% risetimes of 750 ps and 950ps, respectively, show that overlap occurs as the risetime becomes longer than the line propagation delay.

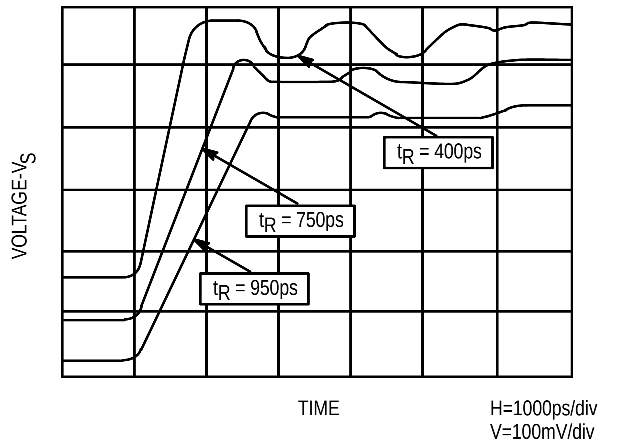

Figure 2.24. Reflections Due to Distributed Capacitance

Increasing the number of distributed capacitive loads effectively decreases the line characteristic impedance as demonstrated by Figure 2.25. The upper trace shows that reflections occur for approximately 3.5ns, during which time the characteristic impedance of the line appears lower(≈76Ω) than actual due to capacitive loading. After the reflections have ended, the transmission line appears as a short and the final steady state voltage is reached. The middle trace shows that decreasing the termination resistance to match the effective line characteristic impedance produces a response typical of a properly terminated line. Finally, the lower trace shows that the original steady state output can be attained by changing the source resistance to match the load resistance and the effective characteristic capacitance.

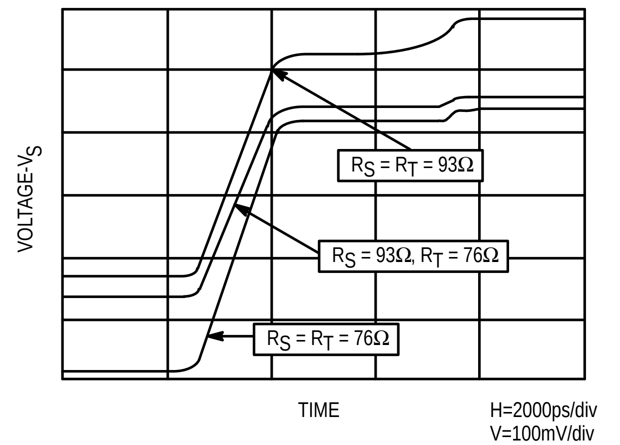

Figure 2.25. Characteristic Impedance Changes Due to Distributed Capacitive Loads

Reduced Line Characteristic Impedance

To a first order approximation the load capacitance (C_L) is represented as an increase in the intrinsic line capacitance along that portion of the transmission line for which the load capacitances are distributed. If the length over which the load capacitances are distributed is defined as “L” the distributed value of the load capacitance (C_D) is given by

$$C_D = C_L/L \qquad \text{(Equation 11)}$$

The reduced line impedance is obtained by adding C_D to C_O in Equation 1.

$$Z_O \sqrt{(L_O/C_O)}$$

$$Z_O' \sqrt{(L_O/(C_O + C_D))} = \sqrt{(L_O/(C_O{}^*(1+C_D/C_O)))}$$

$$Z_O' = Z_O/\sqrt{(1 + C_D/C_O)} \qquad \text{(Equation 12)}$$

For the circuit used to obtain the traces in Figure 2.25, the distributed load capacitance is 4pF. From Equation 3, C_O is calculated as

$$C_O = 750ps/93\Omega = 8pF$$

Hence:

$$Z_O' \ 93\Omega/\sqrt{(1 + 4pF/8pF)} = 76\Omega$$

Thus, the effective line impedance is 17Ω lower than the actual impedance while reflections are occurring on the line.

Line Delay Increase

The increase in line delay caused by distributed loading is calculated by adding the distributed capacitance (C_D) to the intrinsic line capacitance in Equation 2.

$$T_{PD} = \sqrt{(L_O{}^*C_O)}$$

$$T_{PD}' = \sqrt{(L_O{}^*(C_O+C_D))}$$

$$T_{PD}' = T_{PD}{}^*\sqrt{(1 + C_D/C_O)} \qquad \text{(Equation 1 3)}$$

Once again, for the circuit used to obtain the traces in Figure 2.25, the distributed load capacitance is 4pF. From the previous example, the intrinsic line capacitance is 8pF therefore,

$$T_{PD}' = 750ps{}^*\sqrt{(1 + 4pF/8pF)} = 919ps$$

Thus, the effect of distributed load capacitance on line delay is to increase the delay by 169ps. From Equation 13 it is obvious that the larger the C_O of the line the smaller will be the increase in delay due to a distributive capacitive load. Therefore, to obtain the minimum impedance change and lowest propagation delay as a function of gate loading, the lowest characteristic impedance line should be used as this results in a line with the largest intrinsic line capacitance.