CMOS processes [17], where there is little substrate effect, compared to typical values of $n = 1.3$–1.4 for bulk CMOS processes. As shown later, n decreases slightly with increasing V_{GS} and V_{SB}. While n given in the table is an implicit expression since it appears inside the expression itself, it converges rapidly. A value of $n = 1.4$ can be assumed initially with the results of that calculation used for the next calculation. Two calculations usually render a value for n within 1 % of its converged value.

Figure 3.2 shows the calculated n for nMOS devices in a 0.18 µm CMOS process having parameters of $\gamma = 0.56\,\mathrm{V}^{1/2}$, $PHI = 2\phi_F = 0.85\,\mathrm{V}$, $V_{TO} = 0.42\,\mathrm{V}$, and $U_T = 25.9\,\mathrm{mV}$ $(T = 300\,\mathrm{K})$ listed in Table 3.2. n is calculated for $V_{SB} = 0\,\mathrm{V}$ and 1 V using the expressions in Table 3.6. For $V_{SB} = 0\,\mathrm{V}$, n is 1.3 near the onset of weak inversion where V_{GS} is 72 mV below the threshold voltage. It decreases slightly to 1.28 in the center of moderate inversion where V_{GS} is 40 mV above the threshold voltage. n continues dropping slightly to 1.26 near the onset of strong inversion where V_{GS} is approximately 225 mV above the threshold voltage, and it continues dropping to 1.24 and 1.21 deeper in strong inversion where V_{GS} is 0.5 and 1 V above the threshold voltage. n is within ±1.6 % of its moderate inversion value from the onset of weak inversion to the onset of strong inversion. Since n is a slight function of the gate–source voltage, and correspondingly the inversion level, we will often approximate it as a constant at its moderate inversion value. This approximation improves for low-voltage processes where V_{GS} and the level of MOS inversion are necessarily limited.

As shown in Figure 3.2, n decreases approximately by 6 % in moderate inversion for $V_{SB} = 1\,\mathrm{V}$. This drop, which is greater in weak inversion, is a result of reverse, source–body bias that reduces the depletion capacitance. Since V_{SB} is necessarily limited in low-voltage design, n can be expected to vary only slightly with V_{SB}.

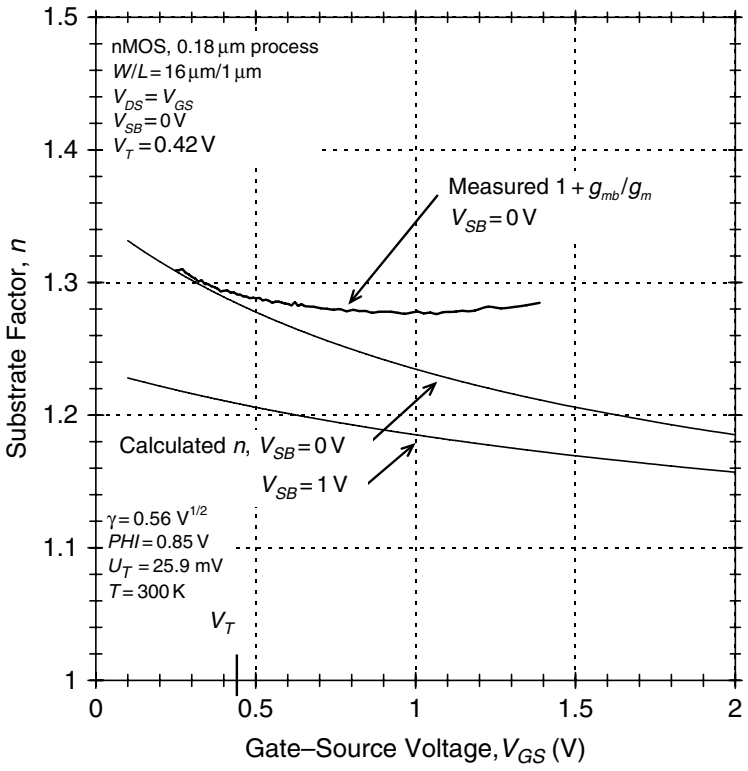

Figure 3.2 Predicted substrate factor, n, versus gate–source voltage with overlay of measured $1 + g_{mb}/g_m$ for nMOS devices in a 0.18 µm CMOS process. The measured $1 + g_{mb}/g_m$ overlay tracks n in weak inversion before leveling off in strong inversion. n decreases by 3 % from the onset of weak inversion to the onset of strong inversion and decreases by approximately 6 % for a source–body voltage of $V_{SB} = 1\,\mathrm{V}$. n is slightly higher for pMOS devices due to an increase in process γ