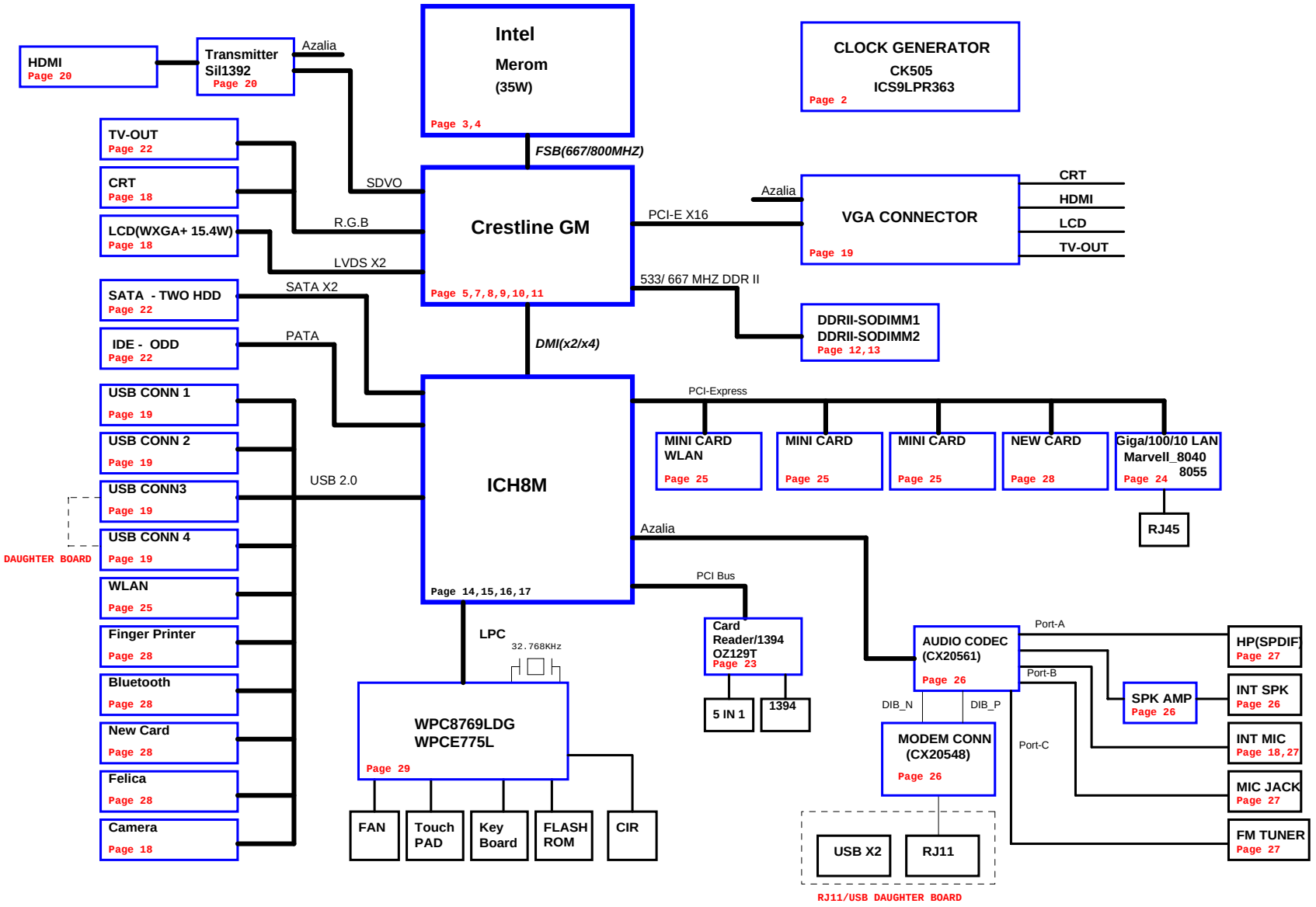
BL5S Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

- VCC_CORE
- +1.5V
- +1.05V
- +1.25V
- +1.8VSUS
- +3VPCU
  +3V_S5
  +3VSUS
  +3V
  +5VPCU
  +5V_S5
  +5V
  SMDDR_VTERM
  SMDDR_VREF

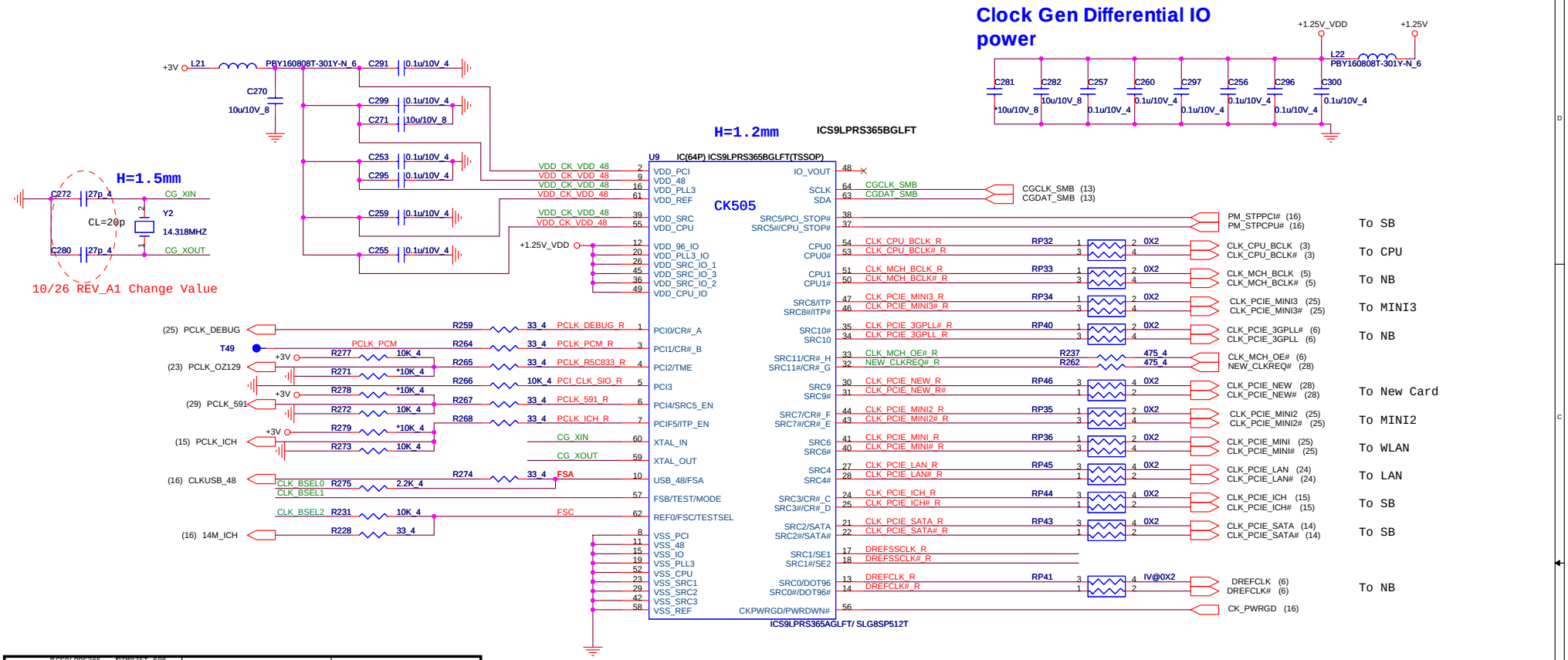


Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	Block Diagram	1A

Date: Tuesday, January 22, 2008 Sheet 1 of 37

Clock Generator



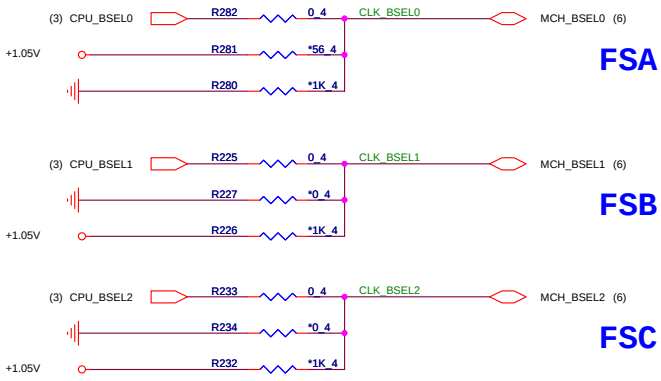
Clock Gen Differential IO power

	ICS9LPRS365 (ALPRS365K13)	RTM8751-606 (AL000875K06)	PULL HIGH	PULL DOWN
Pin 4	PCI2/TME	PCI2/TME internal PD	NO OVERCLOCKING (default)	NORMAL RUN
Pin 5	PCI-3	PCI-3/SRC5_EN internal PD	PIN37/38 IS SRC5	PIN37/38 IS PCI_STOP/CPU_STOP (default)
Pin 6	PCI-4/27M_SEL	PCI-4/27M_SEL internal PD	PIN 17/18 IS 27MHz	PIN 17/18 IS SRC/DOT (default)
Pin 7	PCIF-5/ITP_EN	PCIF-5/ITP_EN internal PD	PIN 46/47 IS CPUITP	PIN 46/47 IS SRC8 (default)

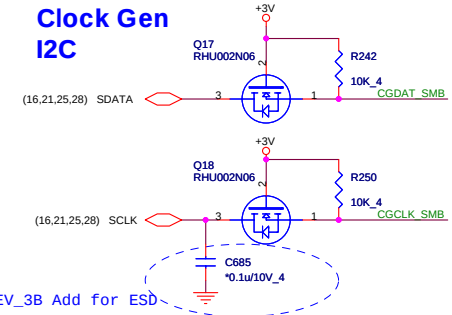
CPU Clock select

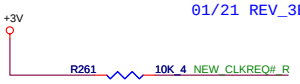
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



Clock Gen I2C





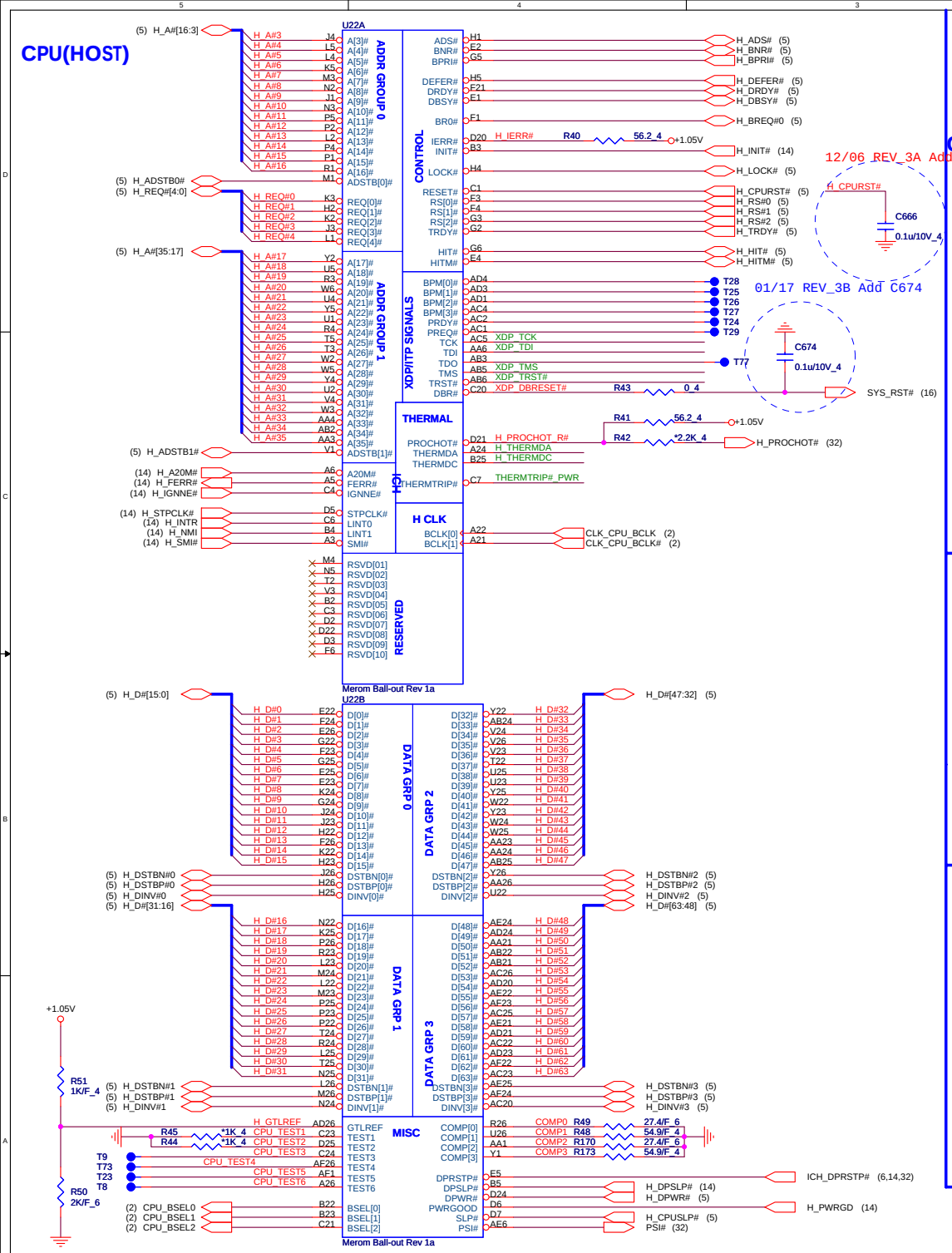
Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

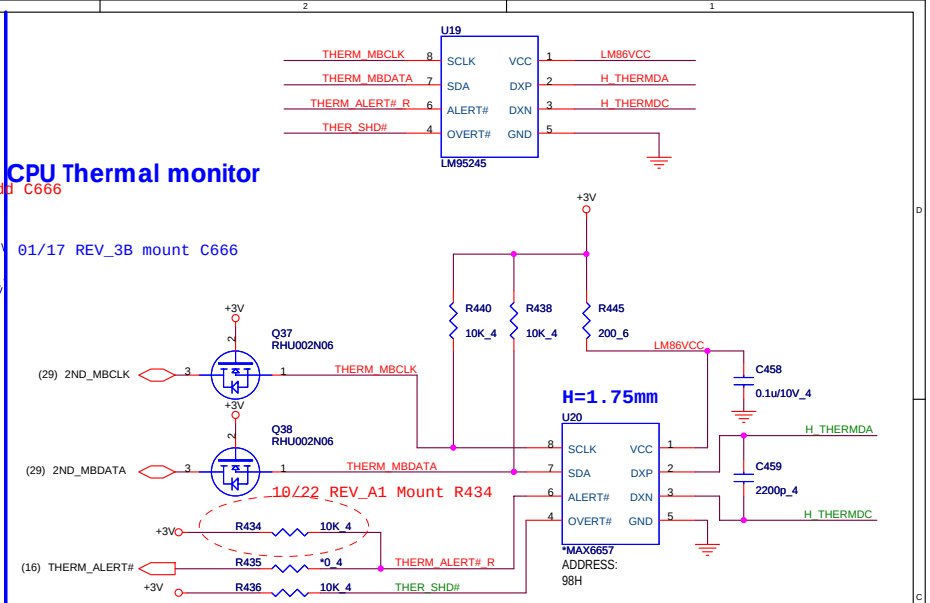
Size	Document Number	Rev
	CLK. GEN./ CK505	1A

Date: Tuesday, January 22, 2008 Sheet 2 of 37

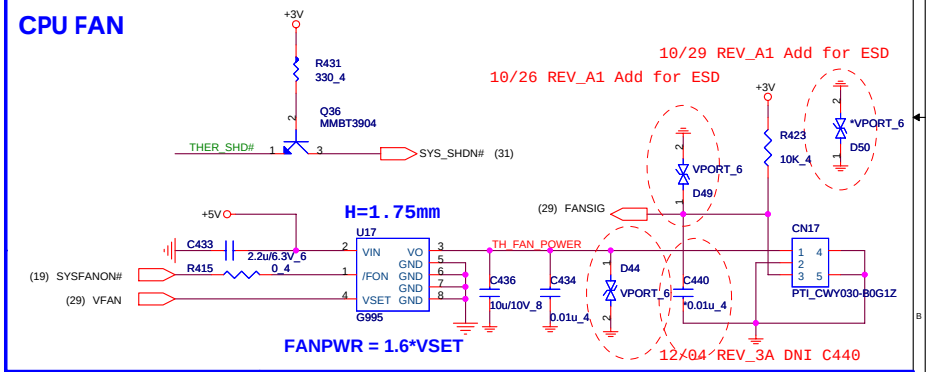
CPU(HOST)



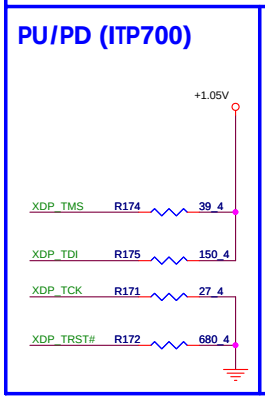
CPU Thermal monitor



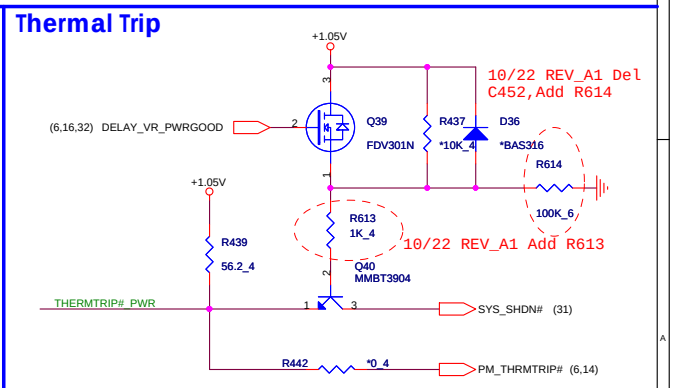
CPU FAN



PU/PD (ITP700)



Thermal Trip



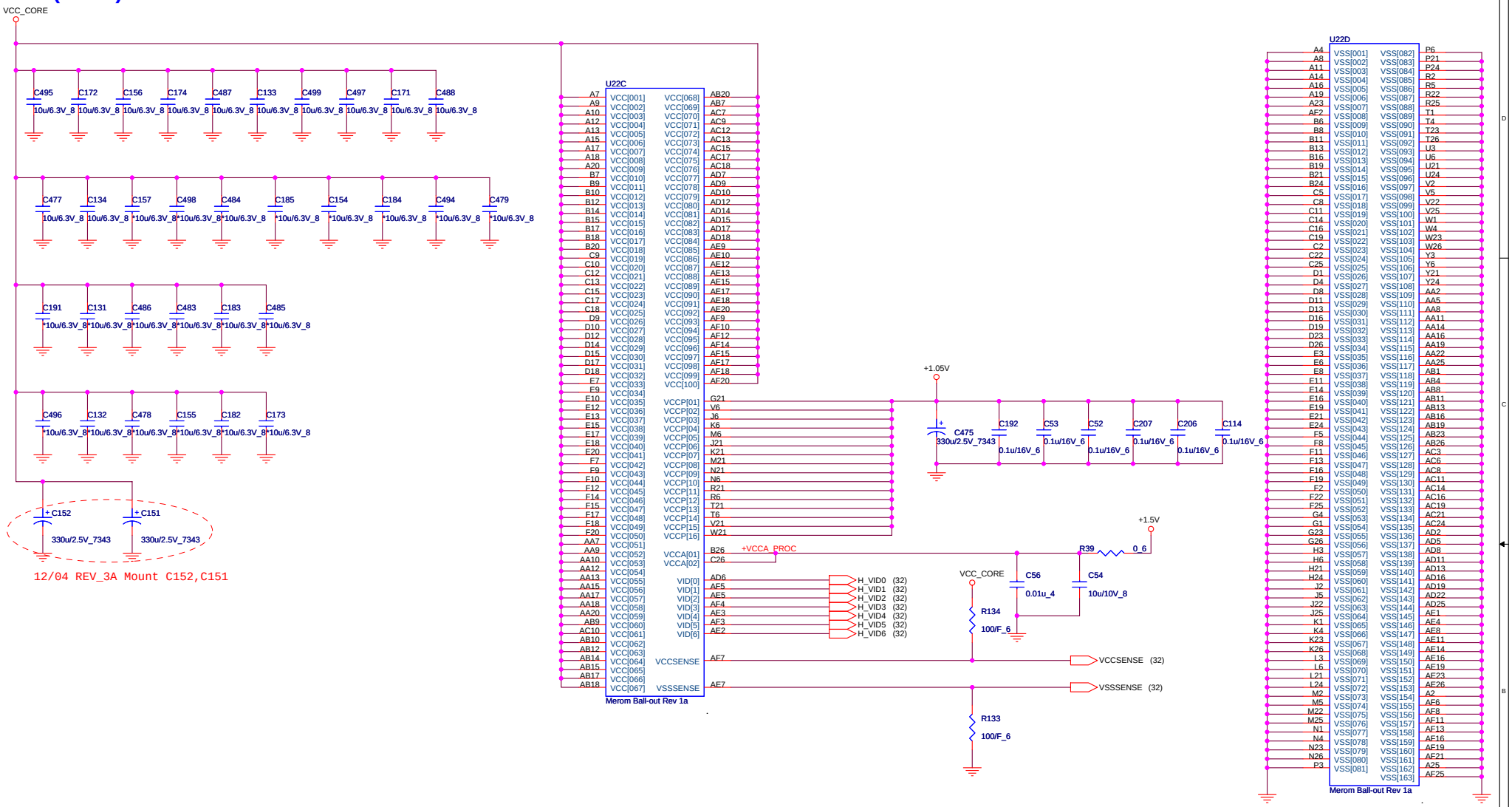
Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	CPU(1 of 2)/FAN/Thermal	1A

Date: Tuesday, January 22, 2008 Sheet 3 of 37

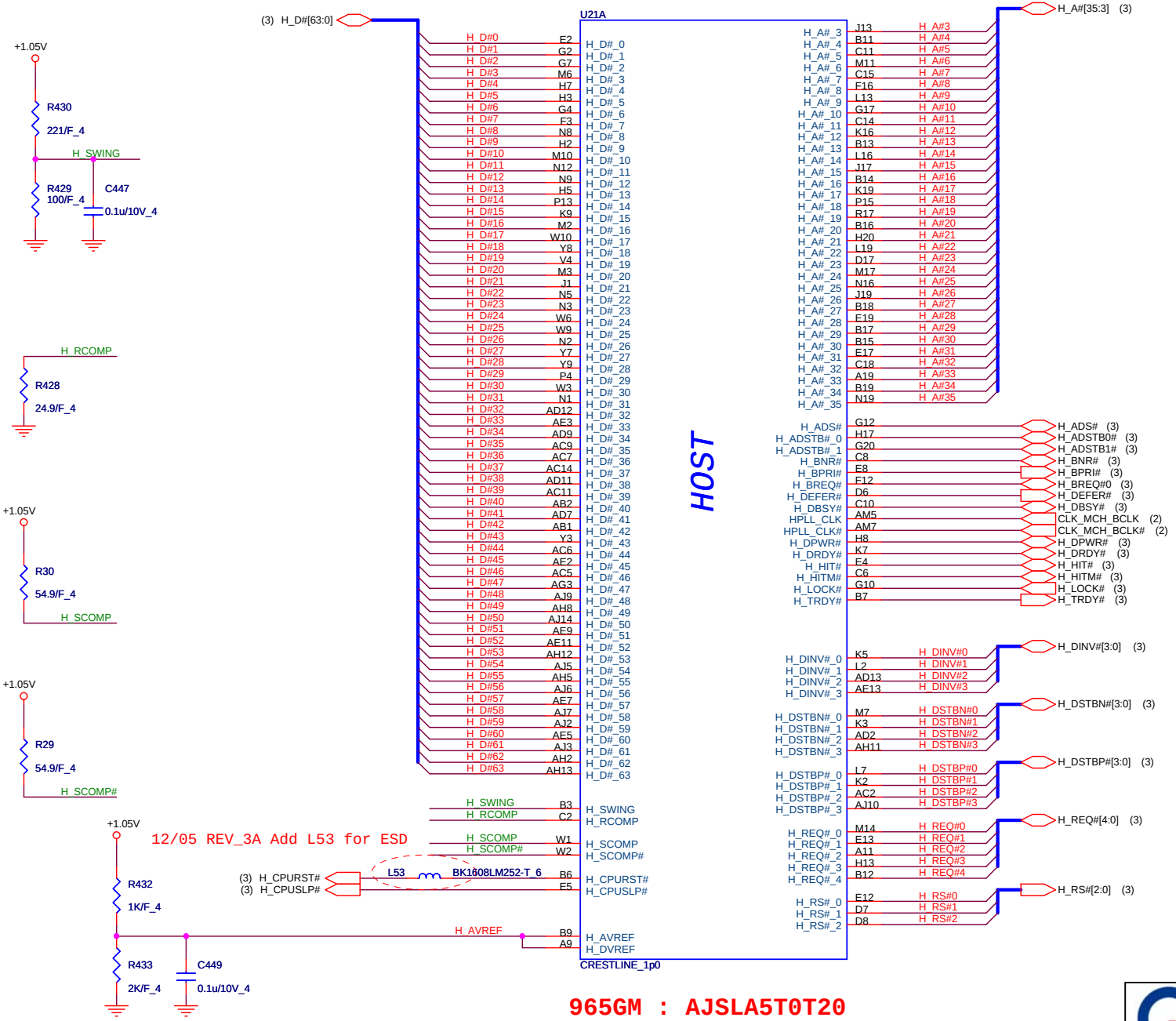
CPU(Power)



12/04 REV_3A Mount C152,C151

Quanta Computer Inc.			
PROJECT : BL5S Santa Rosa			
Size	Document Number		Rev
	CPU(2 of 2)		1A
Date: Tuesday, January 22, 2008	Sheet 4 of 37		

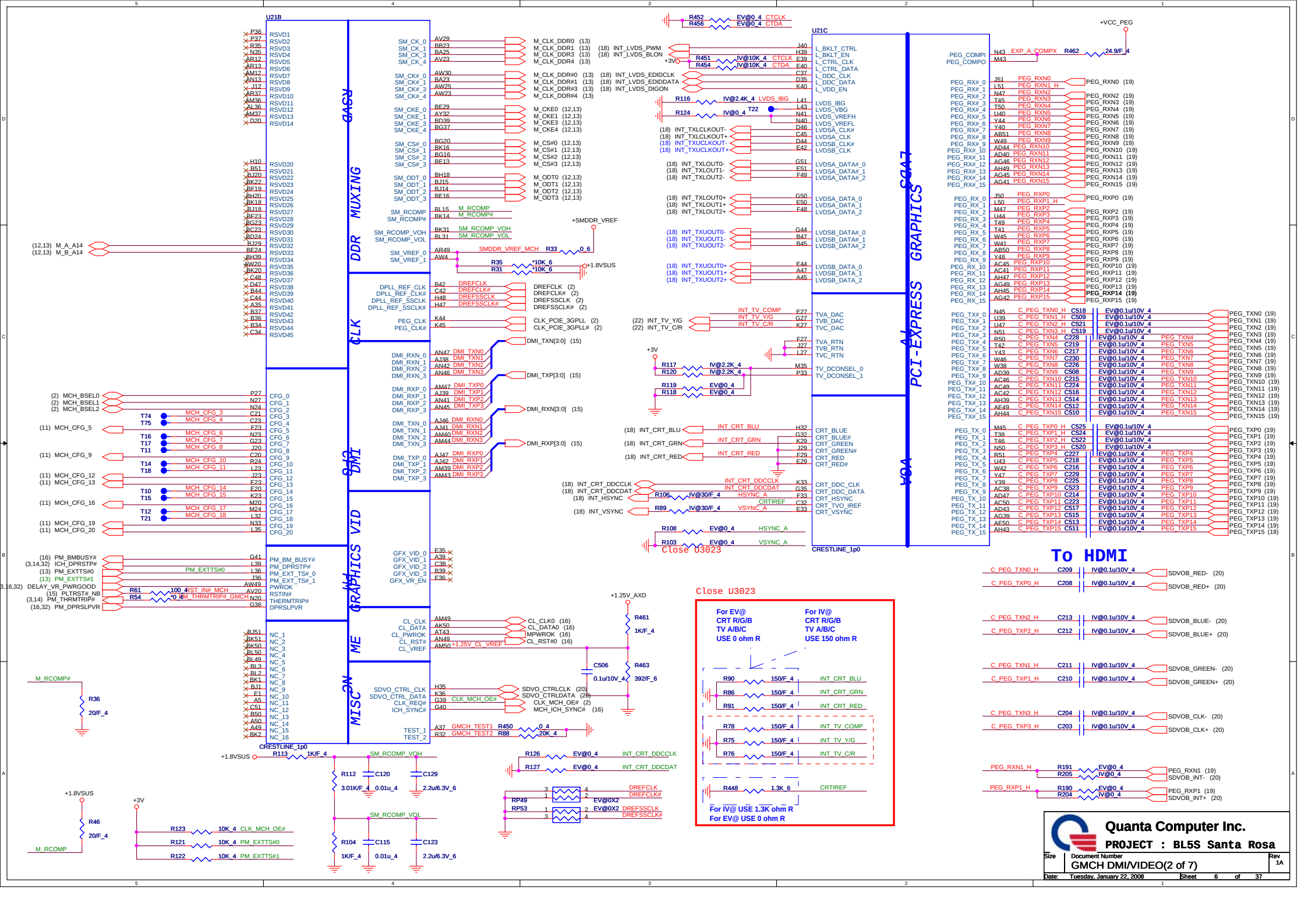
NB(HOST)



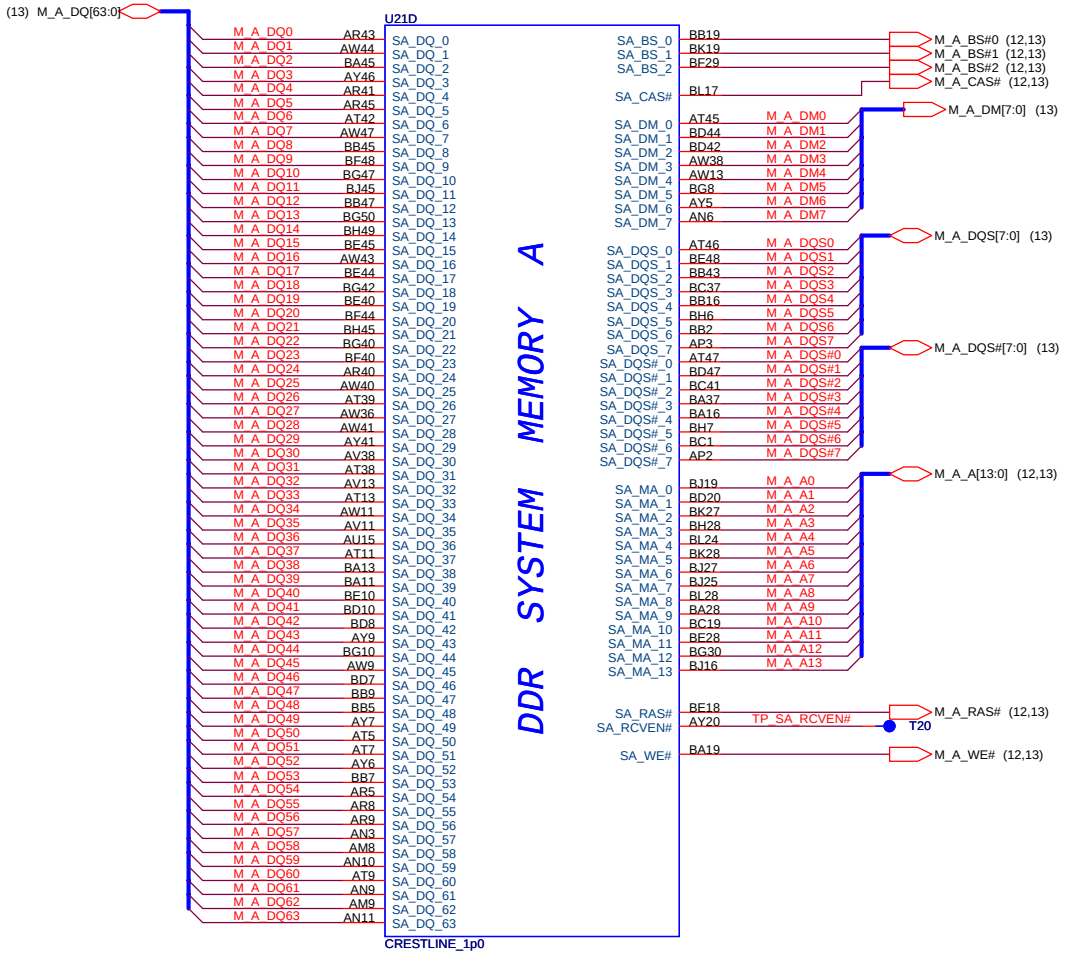
965GM : AJSLA5T0T20
965PM : AJSLA5U0T25
960GL : AJSLA5V0T09

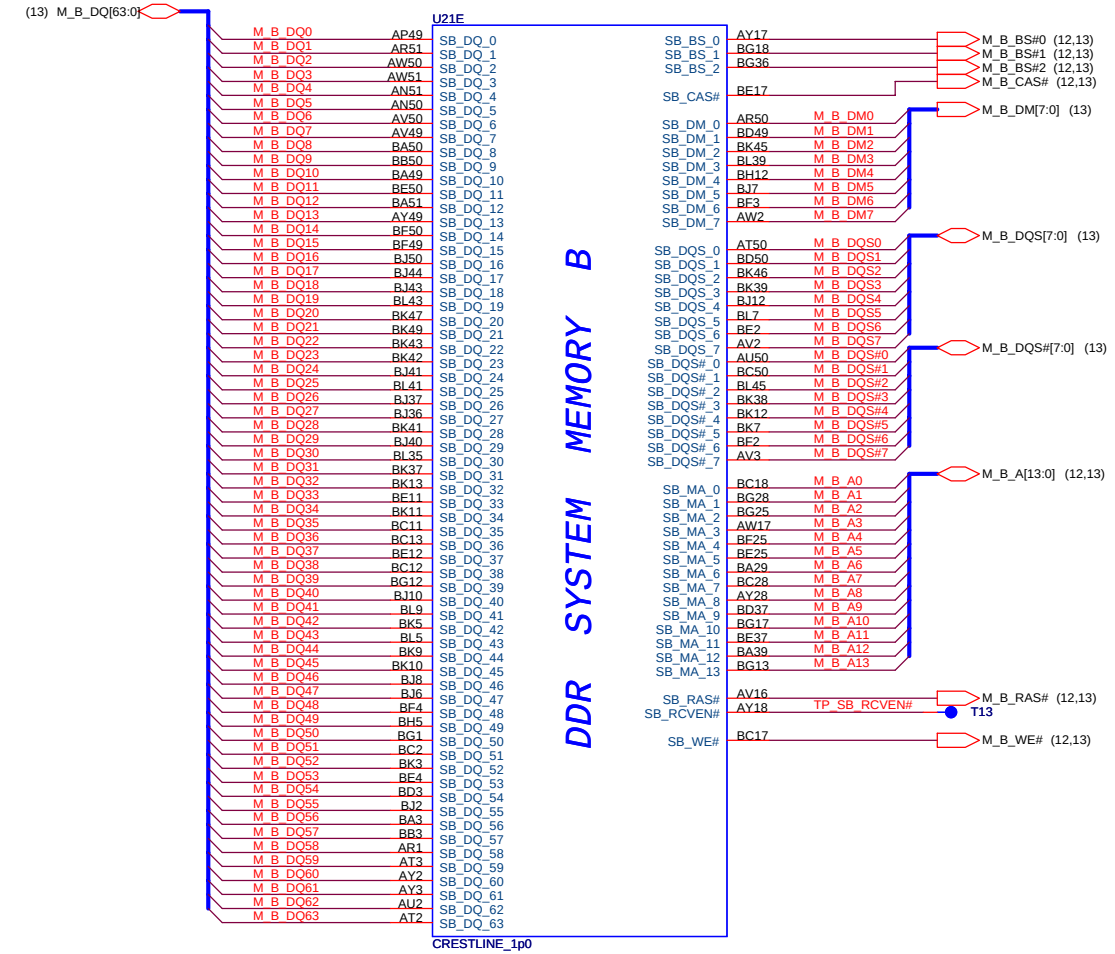
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	GMCH HOST(1 of 7)	1A
Date: Tuesday, January 22, 2008	Sheet 5 of 37	


U21B
U21C
CRESTLINE_1p0
CRESTLINE_1p0
EASY
DDR MUXING
CLK
DMI
GRAPHICS VID
MISC
PCI-EXPRESS GRAPHICS
VGA
To HDMI
Close U3023
Close U3023
For EV@ CRT R/G/B TV A/B/C USE 0 ohm R
For IV@ CRT R/G/B TV A/B/C USE 150 ohm R
For IV@ USE 1.3K ohm R
For EV@ USE 0 ohm R
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
GMCH DMI/VIDEO(2 of 7)
Size
Document Number
Rev 1A
Date: Tuesday, January 22, 2008
Sheet 6 of 37

NB(Memory controller)





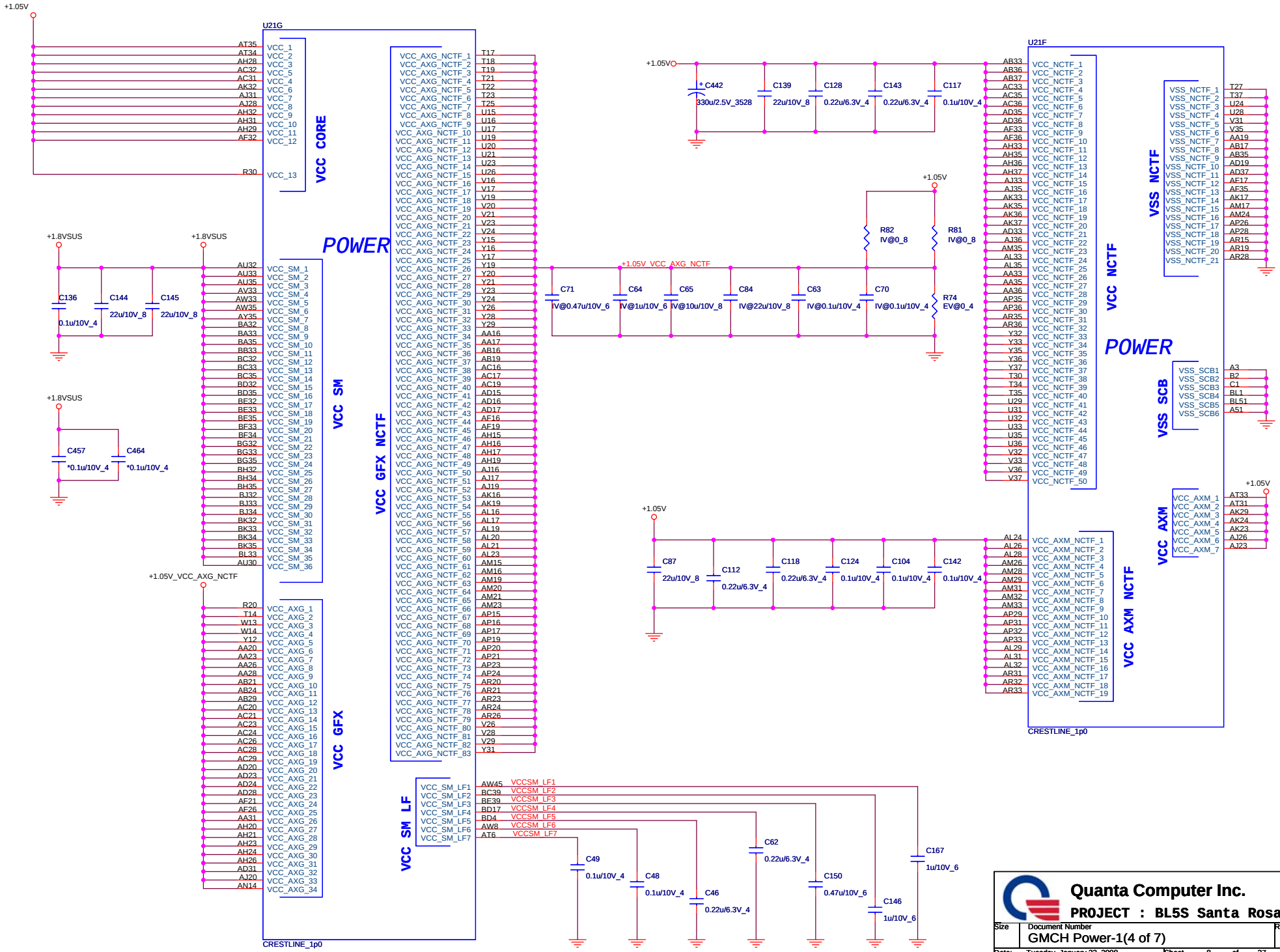
Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	MCH DDR(3 of 7)	1A

Date: Tuesday, January 22, 2008 Sheet 7 of 37

NB(Power-1)


+1.05V
U21G
VCC CORE
VCC_1
VCC_2
VCC_3
VCC_5
VCC_4
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
R30
POWER
+1.8VSUS
VCC SM
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
VCC_SM_7
VCC_SM_8
VCC_SM_9
VCC_SM_10
VCC_SM_11
VCC_SM_12
VCC_SM_13
VCC_SM_14
VCC_SM_15
VCC_SM_16
VCC_SM_17
VCC_SM_18
VCC_SM_19
VCC_SM_20
VCC_SM_21
VCC_SM_22
VCC_SM_23
VCC_SM_24
VCC_SM_25
VCC_SM_26
VCC_SM_27
VCC_SM_28
VCC_SM_29
VCC_SM_30
VCC_SM_31
VCC_SM_32
VCC_SM_33
VCC_SM_34
VCC_SM_35
VCC_SM_36
C136
0.1u/10V_4
C144
22u/10V_8
C145
22u/10V_8
C457
*0.1u/10V_4
C464
*0.1u/10V_4
+1.05V_VCC_AXG_NCTF
VCC GFX
VCC_AXG_1
VCC_AXG_2
VCC_AXG_3
VCC_AXG_4
VCC_AXG_5
VCC_AXG_6
VCC_AXG_7
VCC_AXG_8
VCC_AXG_9
VCC_AXG_10
VCC_AXG_11
VCC_AXG_12
VCC_AXG_13
VCC_AXG_14
VCC_AXG_15
VCC_AXG_16
VCC_AXG_17
VCC_AXG_18
VCC_AXG_19
VCC_AXG_20
VCC_AXG_21
VCC_AXG_22
VCC_AXG_23
VCC_AXG_24
VCC_AXG_25
VCC_AXG_26
VCC_AXG_27
VCC_AXG_28
VCC_AXG_29
VCC_AXG_30
VCC_AXG_31
VCC_AXG_32
VCC_AXG_33
VCC_AXG_34
VCC GFX NCTF
VCC_AXG_NCTF_1
VCC_AXG_NCTF_2
VCC_AXG_NCTF_3
VCC_AXG_NCTF_4
VCC_AXG_NCTF_5
VCC_AXG_NCTF_6
VCC_AXG_NCTF_7
VCC_AXG_NCTF_8
VCC_AXG_NCTF_9
VCC_AXG_NCTF_10
VCC_AXG_NCTF_11
VCC_AXG_NCTF_12
VCC_AXG_NCTF_13
VCC_AXG_NCTF_14
VCC_AXG_NCTF_15
VCC_AXG_NCTF_16
VCC_AXG_NCTF_17
VCC_AXG_NCTF_18
VCC_AXG_NCTF_19
VCC_AXG_NCTF_20
VCC_AXG_NCTF_21
VCC_AXG_NCTF_22
VCC_AXG_NCTF_23
VCC_AXG_NCTF_24
VCC_AXG_NCTF_25
VCC_AXG_NCTF_26
VCC_AXG_NCTF_27
VCC_AXG_NCTF_28
VCC_AXG_NCTF_29
VCC_AXG_NCTF_30
VCC_AXG_NCTF_31
VCC_AXG_NCTF_32
VCC_AXG_NCTF_33
VCC_AXG_NCTF_34
VCC_AXG_NCTF_35
VCC_AXG_NCTF_36
VCC_AXG_NCTF_37
VCC_AXG_NCTF_38
VCC_AXG_NCTF_39
VCC_AXG_NCTF_40
VCC_AXG_NCTF_41
VCC_AXG_NCTF_42
VCC_AXG_NCTF_43
VCC_AXG_NCTF_44
VCC_AXG_NCTF_45
VCC_AXG_NCTF_46
VCC_AXG_NCTF_47
VCC_AXG_NCTF_48
VCC_AXG_NCTF_49
VCC_AXG_NCTF_50
VCC_AXG_NCTF_51
VCC_AXG_NCTF_52
VCC_AXG_NCTF_53
VCC_AXG_NCTF_54
VCC_AXG_NCTF_55
VCC_AXG_NCTF_56
VCC_AXG_NCTF_57
VCC_AXG_NCTF_58
VCC_AXG_NCTF_59
VCC_AXG_NCTF_60
VCC_AXG_NCTF_61
VCC_AXG_NCTF_62
VCC_AXG_NCTF_63
VCC_AXG_NCTF_64
VCC_AXG_NCTF_65
VCC_AXG_NCTF_66
VCC_AXG_NCTF_67
VCC_AXG_NCTF_68
VCC_AXG_NCTF_69
VCC_AXG_NCTF_70
VCC_AXG_NCTF_71
VCC_AXG_NCTF_72
VCC_AXG_NCTF_73
VCC_AXG_NCTF_74
VCC_AXG_NCTF_75
VCC_AXG_NCTF_76
VCC_AXG_NCTF_77
VCC_AXG_NCTF_78
VCC_AXG_NCTF_79
VCC_AXG_NCTF_80
VCC_AXG_NCTF_81
VCC_AXG_NCTF_82
VCC_AXG_NCTF_83
VCC SM LF
VCC_SM_LF1
VCC_SM_LF2
VCC_SM_LF3
VCC_SM_LF4
VCC_SM_LF5
VCC_SM_LF6
VCC_SM_LF7
VCCSM_LF1
VCCSM_LF2
VCCSM_LF3
VCCSM_LF4
VCCSM_LF5
VCCSM_LF6
VCCSM_LF7
C49
0.1u/10V_4
C48
0.1u/10V_4
C46
0.22u/6.3V_4
C62
0.22u/6.3V_4
C150
0.47u/10V_6
C146
1u/10V_6
C167
1u/10V_6
CRESTLINE_1p0
+1.05V_VCC_AXG_NCTF
C71
IV@0.47u/10V_6
C64
IV@1u/10V_6
C65
IV@10u/10V_8
C84
IV@22u/10V_8
C63
IV@0.1u/10V_4
C70
IV@0.1u/10V_4
R82
IV@0_8
R81
IV@0_8
R74
EV@0_4
+1.05V
C442
330u/2.5V_3528
C139
22u/10V_8
C128
0.22u/6.3V_4
C143
0.22u/6.3V_4
C117
0.1u/10V_4
U21F
VCC_NCTF_1
VCC_NCTF_2
VCC_NCTF_3
VCC_NCTF_4
VCC_NCTF_5
VCC_NCTF_6
VCC_NCTF_7
VCC_NCTF_8
VCC_NCTF_9
VCC_NCTF_10
VCC_NCTF_11
VCC_NCTF_12
VCC_NCTF_13
VCC_NCTF_14
VCC_NCTF_15
VCC_NCTF_16
VCC_NCTF_17
VCC_NCTF_18
VCC_NCTF_19
VCC_NCTF_20
VCC_NCTF_21
VCC_NCTF_22
VCC_NCTF_23
VCC_NCTF_24
VCC_NCTF_25
VCC_NCTF_26
VCC_NCTF_27
VCC_NCTF_28
VCC_NCTF_29
VCC_NCTF_30
VCC_NCTF_31
VCC_NCTF_32
VCC_NCTF_33
VCC_NCTF_34
VCC_NCTF_35
VCC_NCTF_36
VCC_NCTF_37
VCC_NCTF_38
VCC_NCTF_39
VCC_NCTF_40
VCC_NCTF_41
VCC_NCTF_42
VCC_NCTF_43
VCC_NCTF_44
VCC_NCTF_45
VCC_NCTF_46
VCC_NCTF_47
VCC_NCTF_48
VCC_NCTF_49
VCC_NCTF_50
VCC NCTF
VSS NCTF
VSS_NCTF_1
VSS_NCTF_2
VSS_NCTF_3
VSS_NCTF_4
VSS_NCTF_5
VSS_NCTF_6
VSS_NCTF_7
VSS_NCTF_8
VSS_NCTF_9
VSS_NCTF_10
VSS_NCTF_11
VSS_NCTF_12
VSS_NCTF_13
VSS_NCTF_14
VSS_NCTF_15
VSS_NCTF_16
VSS_NCTF_17
VSS_NCTF_18
VSS_NCTF_19
VSS_NCTF_20
VSS_NCTF_21
POWER
VSS SCB
VSS_SCB1
VSS_SCB2
VSS_SCB3
VSS_SCB4
VSS_SCB5
VSS_SCB6
VCC AXM
VCC_AXM_1
VCC_AXM_2
VCC_AXM_3
VCC_AXM_4
VCC_AXM_5
VCC_AXM_6
VCC_AXM_7
VCC AXM NCTF
VCC_AXM_NCTF_1
VCC_AXM_NCTF_2
VCC_AXM_NCTF_3
VCC_AXM_NCTF_4
VCC_AXM_NCTF_5
VCC_AXM_NCTF_6
VCC_AXM_NCTF_7
VCC_AXM_NCTF_8
VCC_AXM_NCTF_9
VCC_AXM_NCTF_10
VCC_AXM_NCTF_11
VCC_AXM_NCTF_12
VCC_AXM_NCTF_13
VCC_AXM_NCTF_14
VCC_AXM_NCTF_15
VCC_AXM_NCTF_16
VCC_AXM_NCTF_17
VCC_AXM_NCTF_18
VCC_AXM_NCTF_19
C87
22u/10V_8
C112
0.22u/6.3V_4
C118
0.22u/6.3V_4
C124
0.1u/10V_4
C104
0.1u/10V_4
C142
0.1u/10V_4
CRESTLINE_1p0
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
Size
Document Number
GMCH Power-1(4 of 7)
Rev
1A
Date: Tuesday, January 22, 2008
Sheet 8 of 37

NB(Power-2)

CRT/TV Disable/Enable guideline

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V

EXTERNAL INTERNAL

IV&EV Dis/Enable setting

IV&EV Dis/Enable setting

IV&EV Dis/Enable setting

IV&EV Dis/Enable setting

U21H

CRESTLINE_1p0

POWER

CRT PLL LVDS PEG SM CK TV/CRT DMI VTTLF AXD AXF SM CK HV PEG

<FAE>
INT VGA disable
VCCD_TVDAC still
+1.5V

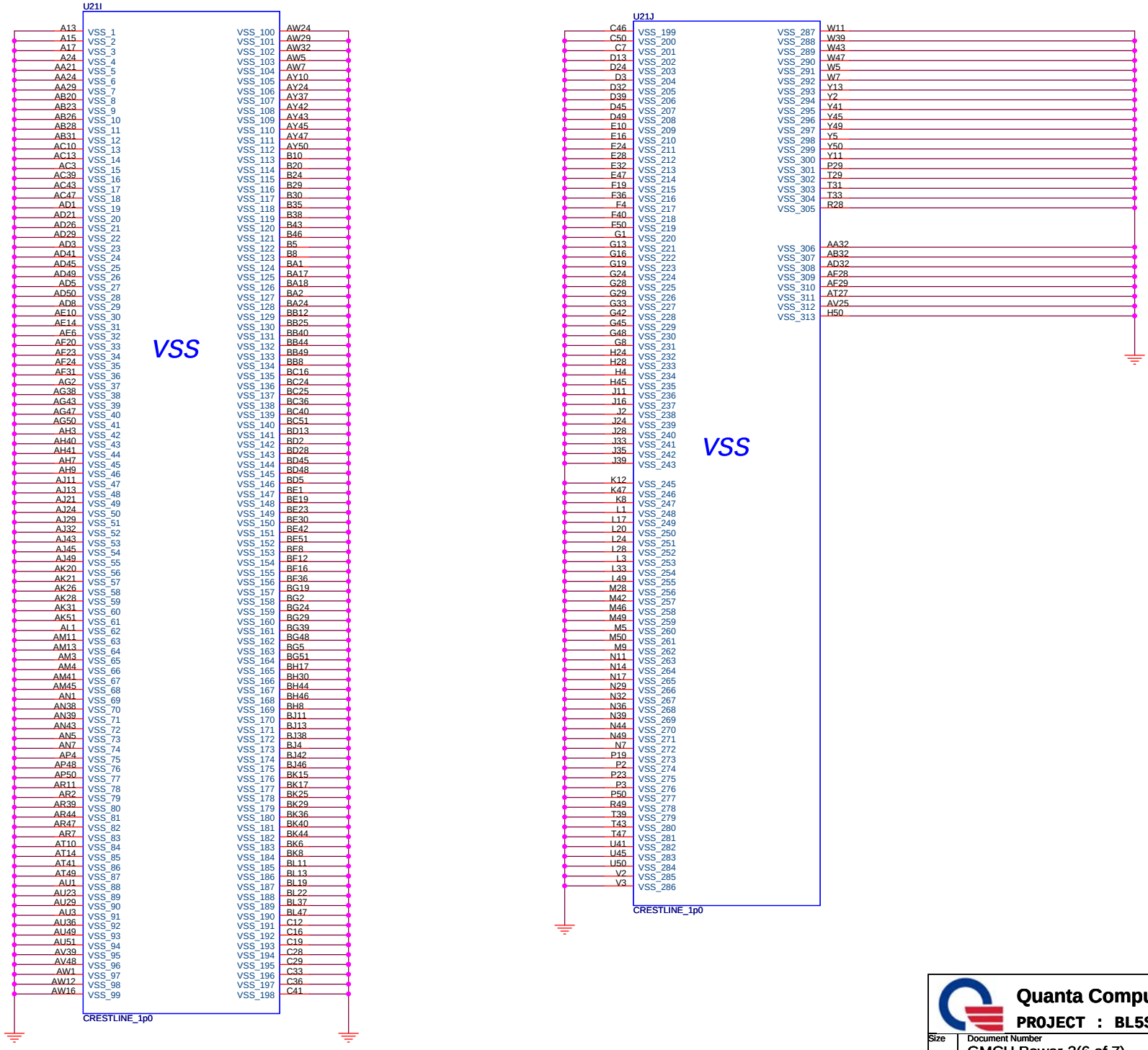
Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size | Document Number: GMCH Power-2(5 of 7) | Rev: 1A

Date: Tuesday, January 22, 2008 | Sheet 9 of 37

NB(Power-3)



Quanta Computer Inc.		
PROJECT : BL5S Santa Rosa		
Size	Document Number: GMCH Power-3(6 of 7)	Rev: 1A
Date: Tuesday, January 22, 2008	Sheet 10 of 37	

Strap table

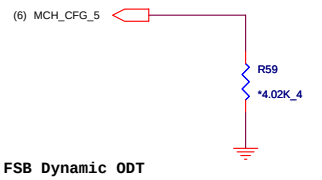
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

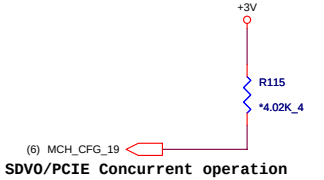
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

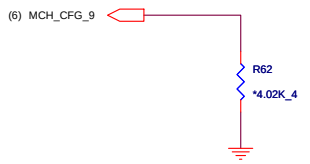


XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

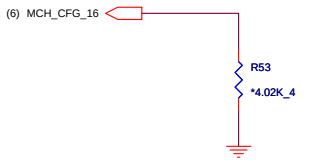


SDVO Present

Strap define at External DVI control page

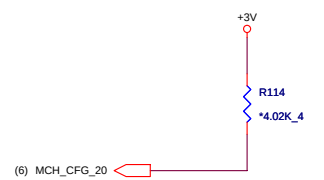
FSB Dynamic ODT

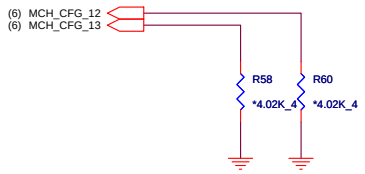
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port



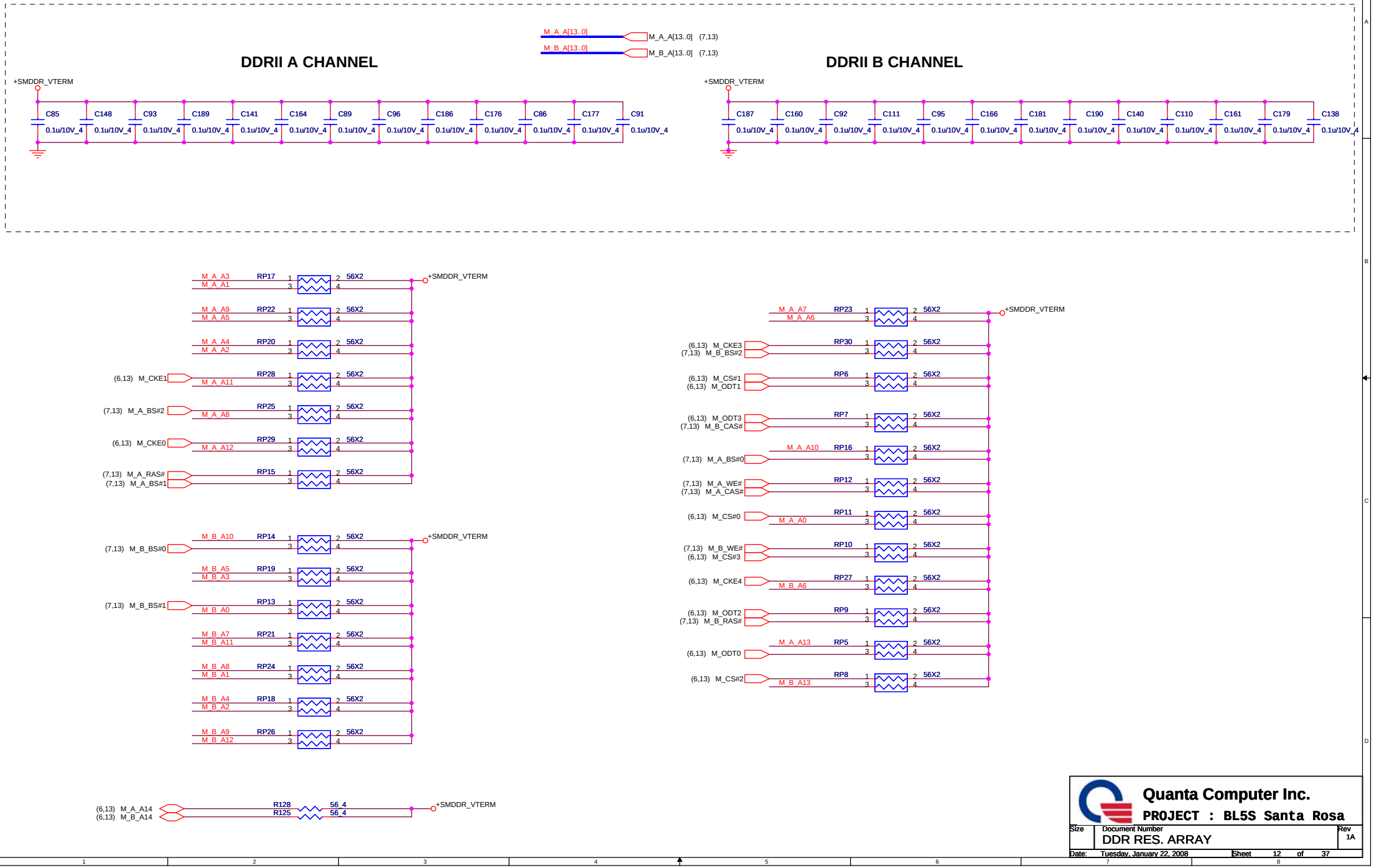


Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	GMCH Strap(7 of 7)	1A

Date: Tuesday, January 22, 2008 Sheet 11 of 37

DDR2 Dual channel A/B PU



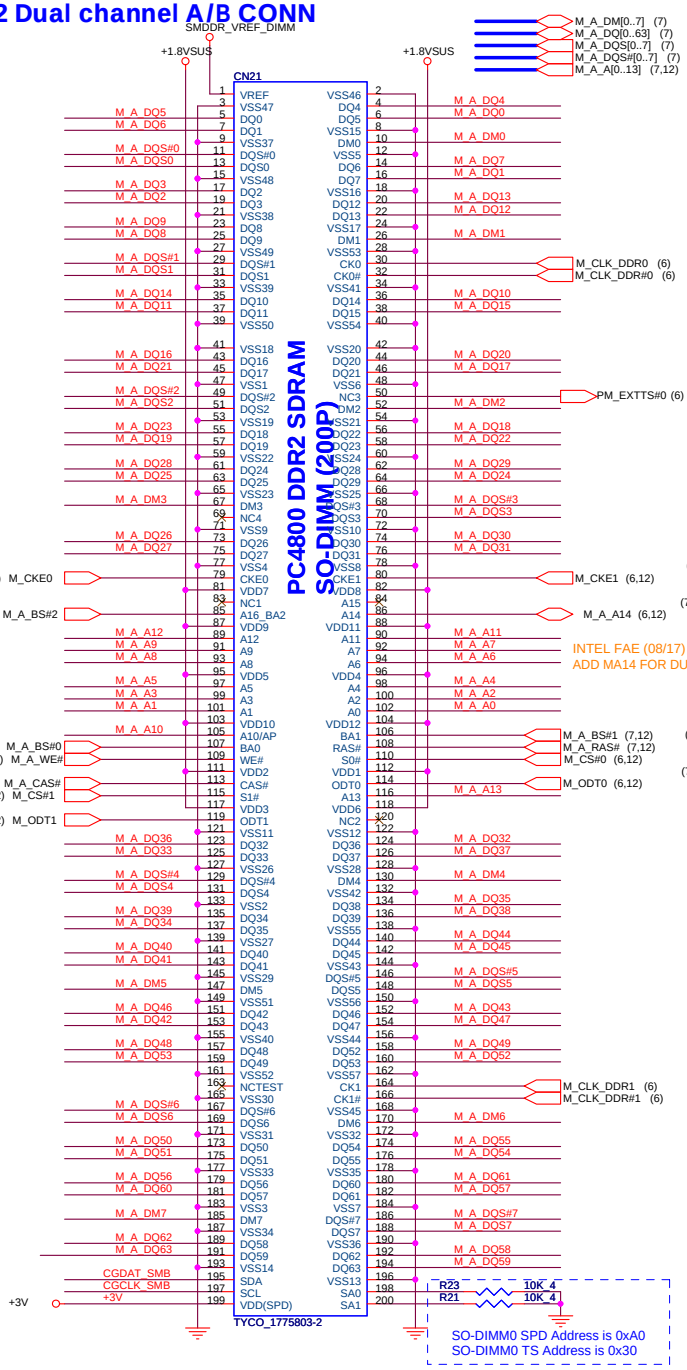
Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

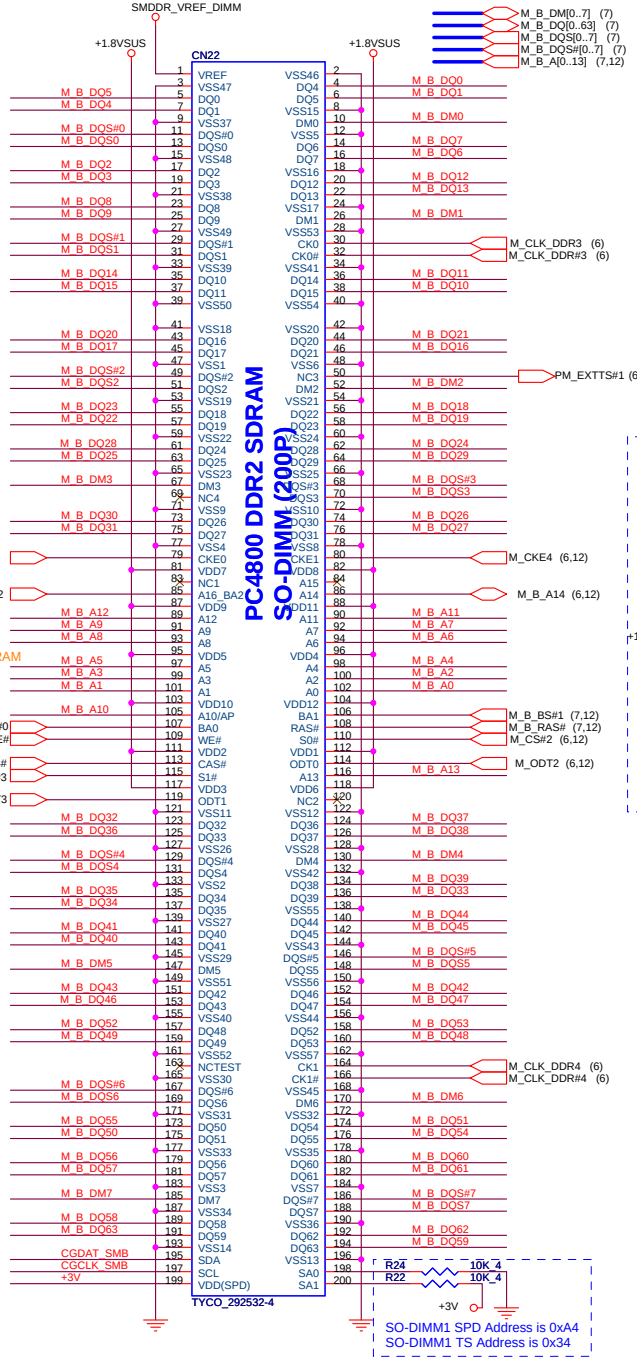
Size	Document Number	Rev
	DDR RES. ARRAY	1A

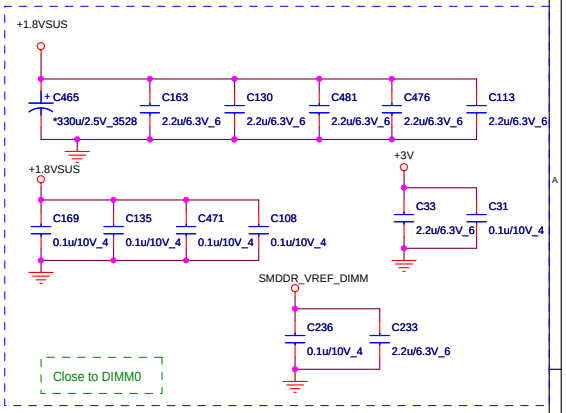
Date: Tuesday, January 22, 2008 Sheet 12 of 37

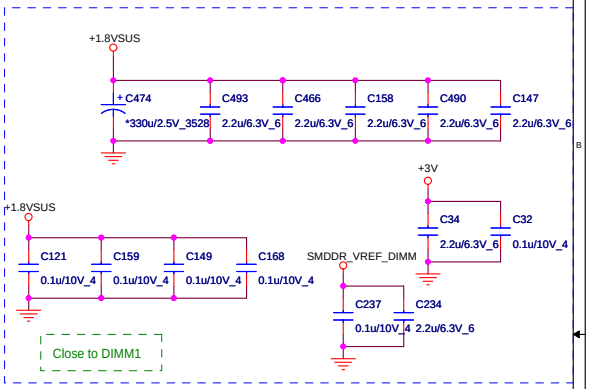
DDR2 Dual channel A/B CONN

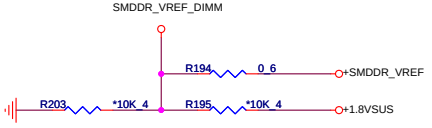


INTEL FAE (08/17)
ADD MA14 FOR DUAL LAYERS RAM









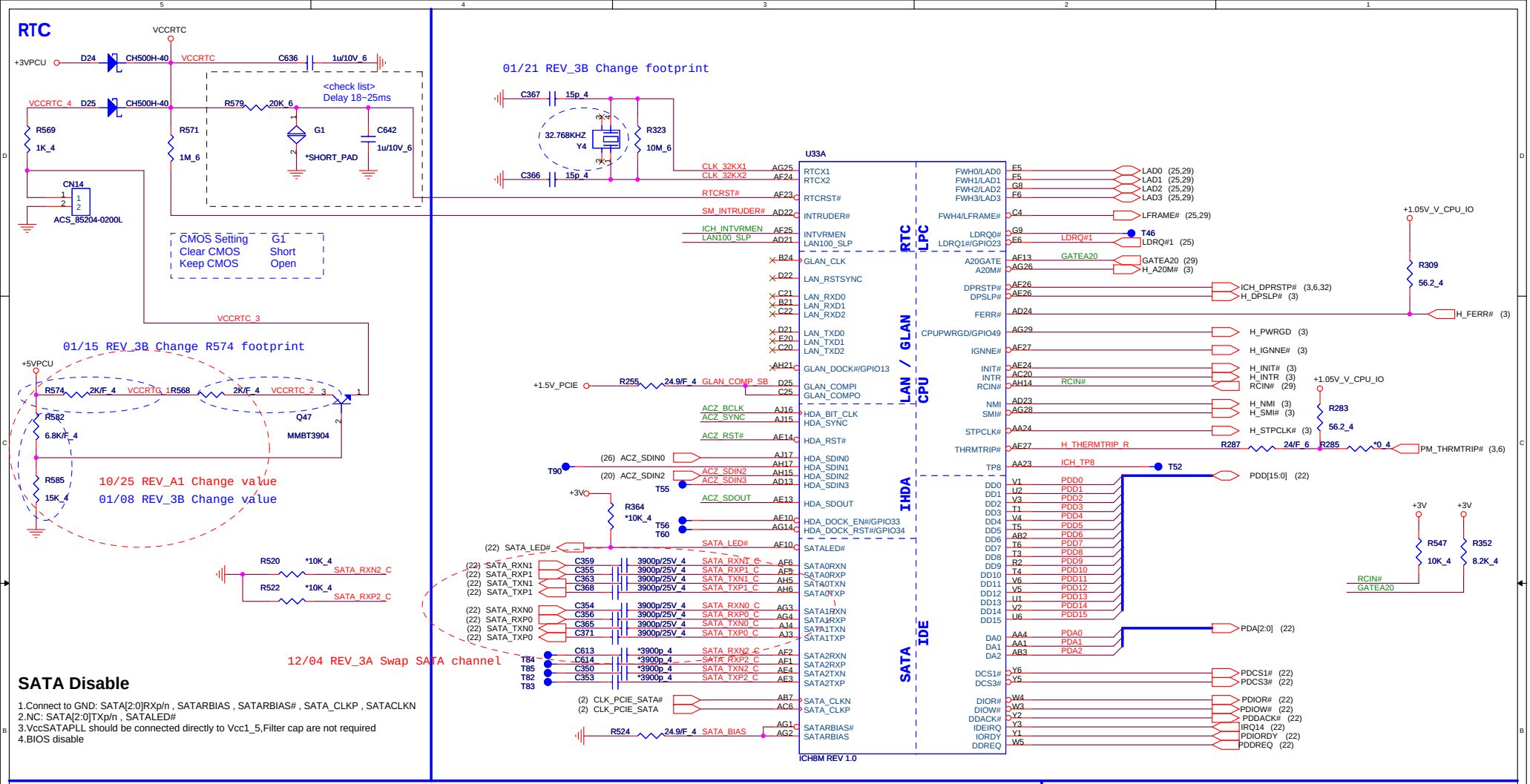
Standard Type H: 6.5mm

CLOCK 0,1
CKE 0,1

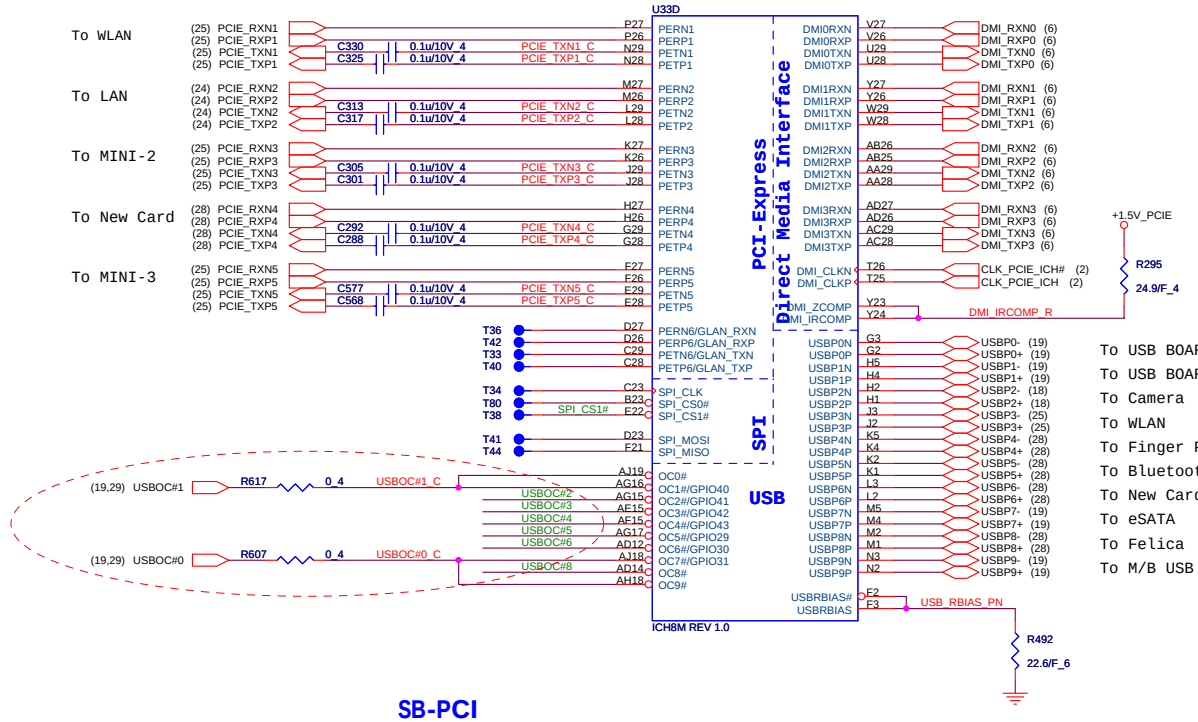
Standard Type H: 11mm

CLOCK 3,4
CKE 2,3

Quanta Computer Inc.	
PROJECT : BL5S Santa Rosa	
Size	Document Number: DDR SO-DIMM(200P) — Rev: 1A
Date: Tuesday, January 22, 2008	Sheet 13 of 37


RTC
VCCRTC
+3VPCU
D24
CH500H-40
C636
1u/10V_6
VCCRTC_4
D25
R579
20K_6
R569
1K_4
R571
1M_6
G1
C642
1u/10V_6
*SHORT_PAD
CN14
ACS_85204-0200L
<check list>
Delay 18~25ms
CMOS Setting G1
Clear CMOS Short
Keep CMOS Open
01/21 REV_3B Change footprint
C367
15p_4
C366
15p_4
32.768KHZ
Y4
R323
10M_6
CLK_32KX1
CLK_32KX2
RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
LAN100_SLP
U33A
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
IDE
ICH8M REV 1.0
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LAD0 (25,29)
LAD1 (25,29)
LAD2 (25,29)
LAD3 (25,29)
LFRAME# (25,29)
LDRQ#1
LDRQ#1 (25)
GATEA20
GATEA20 (29)
H_A20M# (3)
ICH_DPRSTP# (3,6,32)
H_DPSLP# (3)
H_FERR# (3)
H_PWRGD (3)
H_IGNNE# (3)
H_INIT# (3)
H_INTR (3)
RCIN# (29)
H_NMI (3)
H_SMI# (3)
H_STPCLK# (3)
H_THERMTRIP_R
ICH_TP8
PDD[15:0] (22)
PDA[2:0] (22)
PDCS1# (22)
PDCS3# (22)
PDIOR# (22)
PDIOW# (22)
PDDACK# (22)
IRQ14 (22)
PDIORDY (22)
PDDREQ (22)
+1.05V_V_CPU_IO
R309
56.2_4
R283
56.2_4
R287
24/F_6
R285
*0_4
PM_THRMTRIP# (3,6)
T52
+3V
R547
10K_4
R352
8.2K_4
RCIN#
GATEA20
01/15 REV_3B Change R574 footprint
+5VPCU
R574
2K/F_4
VCCRTC_1
R568
2K/F_4
VCCRTC_2
Q47
MMBT3904
R582
6.8K/F_4
R585
15K_4
10/25 REV_A1 Change value
01/08 REV_3B Change value
VCCRTC_3
+1.5V_PCIE
R255
24.9/F_4
GLAN_COMP_SB
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN2
ACZ_SDIN3
ACZ_SDOUT
SATA_LED#
T90
T55
T56
T60
T84
T85
T82
T83
+3V
R364
*10K_4
R520
*10K_4
SATA_RXN2_C
R522
*10K_4
SATA_RXP2_C
(22) SATA_RXN1
(22) SATA_RXP1
(22) SATA_TXN1
(22) SATA_TXP1
(22) SATA_RXN0
(22) SATA_RXP0
(22) SATA_TXN0
(22) SATA_TXP0
C359
C355
C363
C368
C354
C356
C365
C371
3900p/25V_4
C613
C614
C350
C353
*3900p_4
*3900p_4
*3900p_4
*3900p_4
SATA_RXN1_C
SATA_RXP1_C
SATA_TXN1_C
SATA_TXP1_C
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
SATA_RXN2_C
SATA_RXP2_C
SATA_TXN2_C
SATA_TXP2_C
12/04 REV_3A Swap SATA channel
(2) CLK_PCIE_SATA#
(2) CLK_PCIE_SATA
R524
24.9/F_4
SATA_BIAS
SATA Disable
1.Connect to GND: SATA[2:0]RXp/n , SATARBIAS , SATARBIAS# , SATA_CLKP , SATACLKN
2.NC: SATA[2:0]TXp/n , SATALED#
3.VccSATAPLL should be connected directly to Vcc1_5,Filter cap are not required
4.BIOS disable
SB Strap
ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)
INTVRMEN
Low = Internal VR disable
High = Internal VR enable(Default)
ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1.05)
LAN100_SLP
Low = Internal VR disable
High = Internal VR enable(Default)
XOR Chain Entrance Strap
ICH_RSV0 | HDA_SDOUT | Description
0 | 0 | RSVD
0 | 1 | Enter XOR Chain
1 | 0 | Normal opration(Default)
1 | 1 | Set PCIE port config bit 1
VCCRTC
R325
332K_6
ICH_INTVRMEN
R326
*0_4
VCCRTC
R303
332K_6
LAN100_SLP
R312
*0_4
+3V
R368
*1K_6
ACZ_SDOUT
ICH_TP3 (16)
R539
*1K_4
HDA
BIT_CLK_AUDIO
R370
*22_4
C387
*22p/50V_4
BIT_CLK_HDMI
R551
*22_4
C386
*22p/50V_4
ACZ_SDOUT
R372
33_4
ACZ_SDOUT_AUDIO (26)
R351
33_4
ACZ_SDOUT_HDMI (20)
ACZ_SYNC
R549
33_4
ACZ_SYNC_AUDIO (26)
R533
33_4
ACZ_SYNC_HDMI (20)
ACZ_BCLK
R550
33_4
BIT_CLK_AUDIO (26)
R535
33_4
BIT_CLK_HDMI (20)
ACZ_RST#
R371
33_4
ACZ_RST#_AUDIO (26)
R350
33_4
ACZ_RST#_HDMI (20)
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
Size
Document Number
ICH8M HOST(1 of 4)
Rev
1A
Date: Sunday, February 17, 2008
Sheet 14 of 37

SB-PCIE/USB/DMI



A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

GNT3# R251 *1K_4

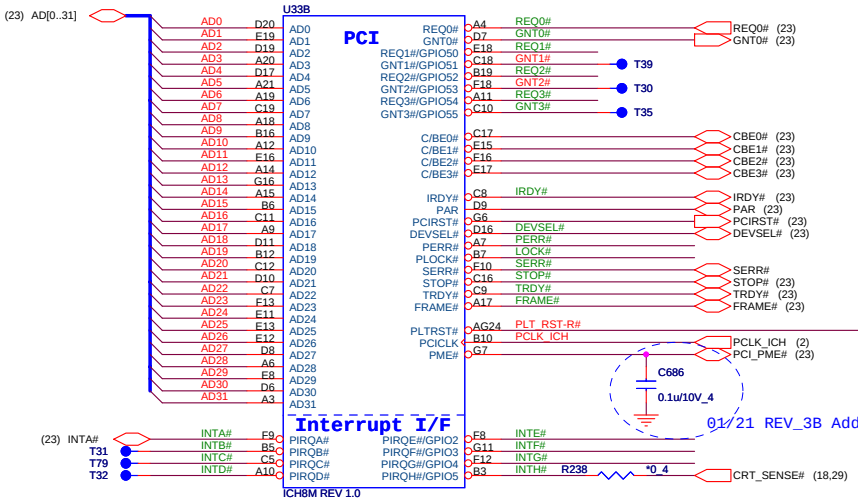
ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

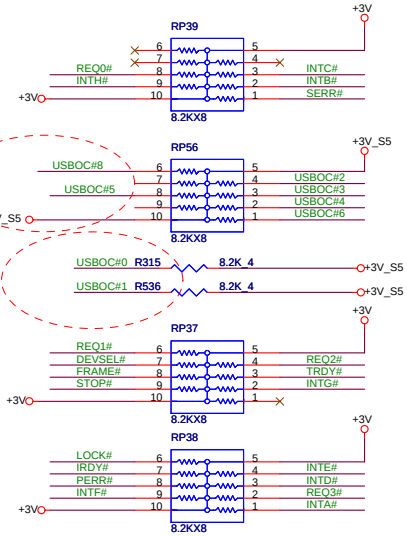
SPI_CS1# R258 *1K_4

GNT0# R253 *1K_4

SB-PCI



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#	OZ129



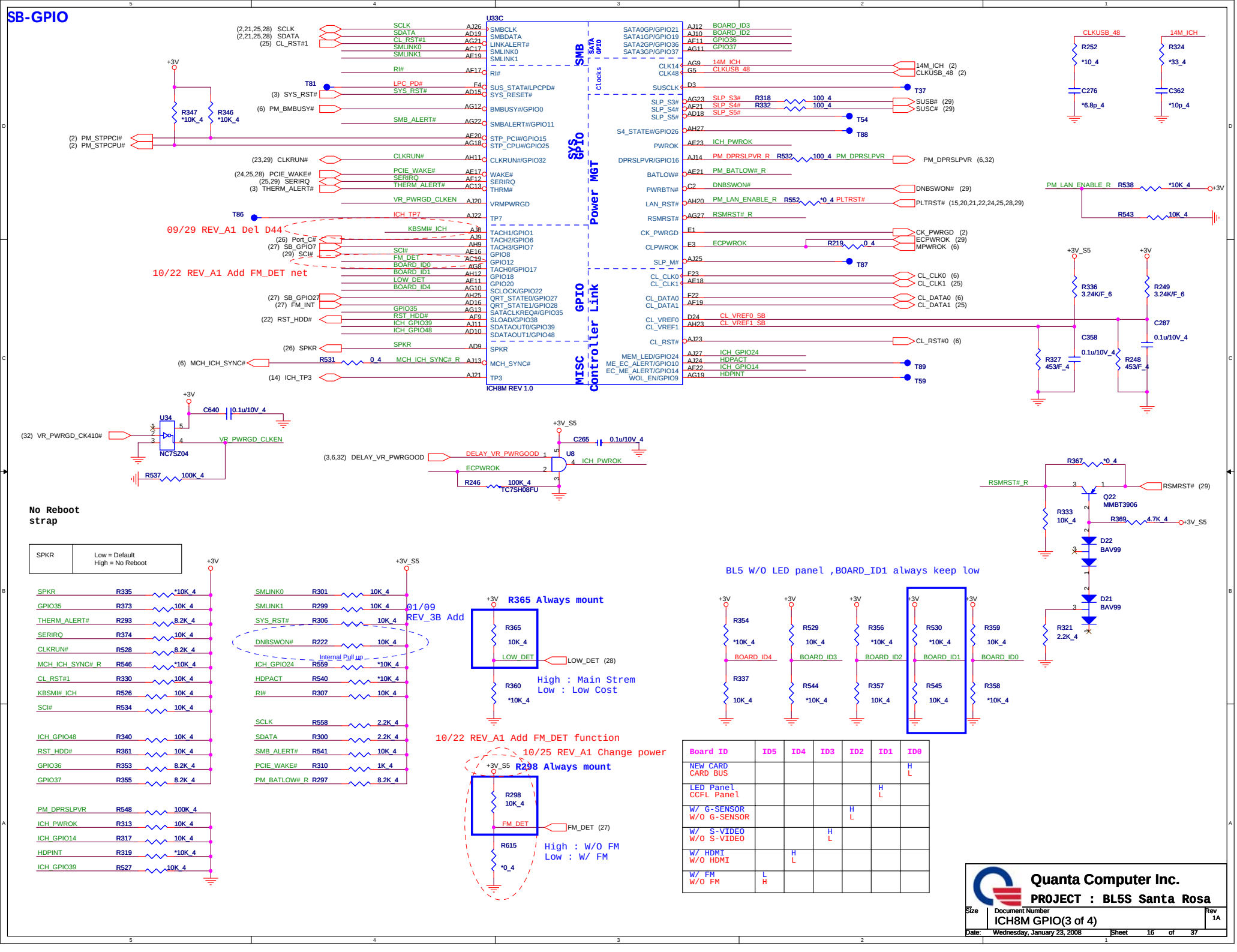
Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	ICH8M PCIE(2 of 4)/ BIOS	1A

Date: Tuesday, January 22, 2008 Sheet 15 of 37

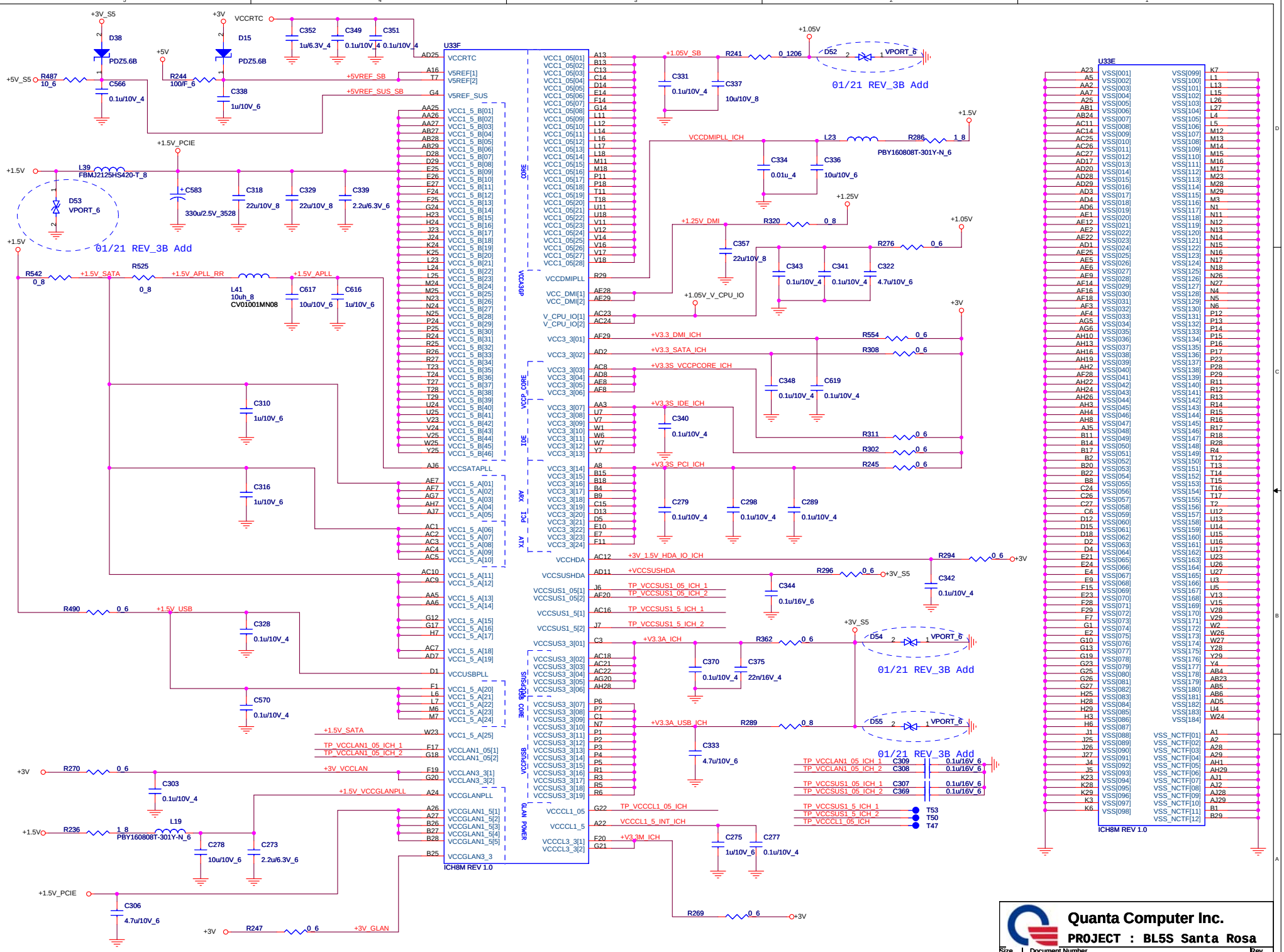
SB-GPIO



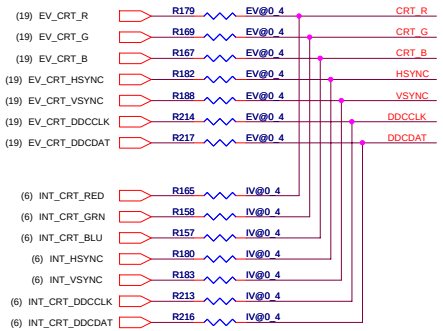
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

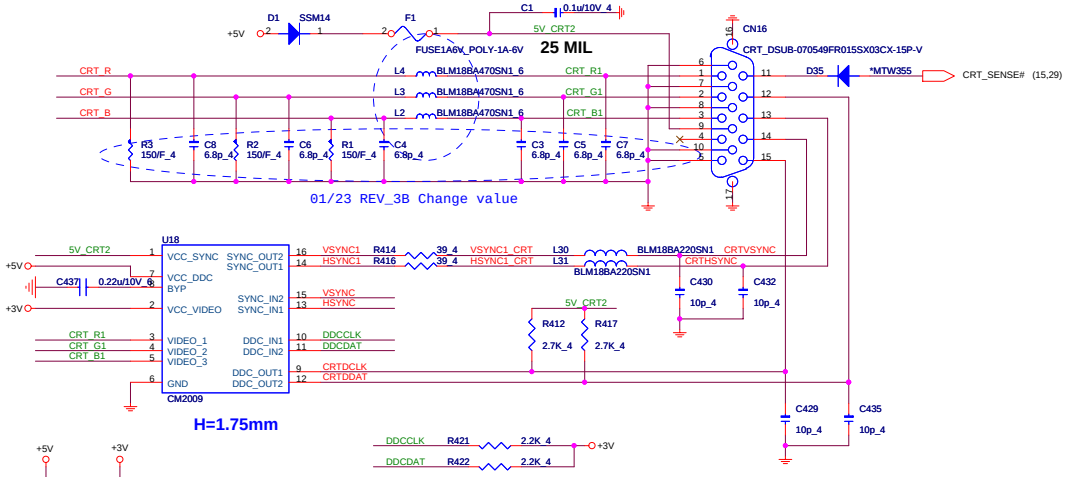
Size	Document Number	Rev
	ICH8M GPIO(3 of 4)	1A

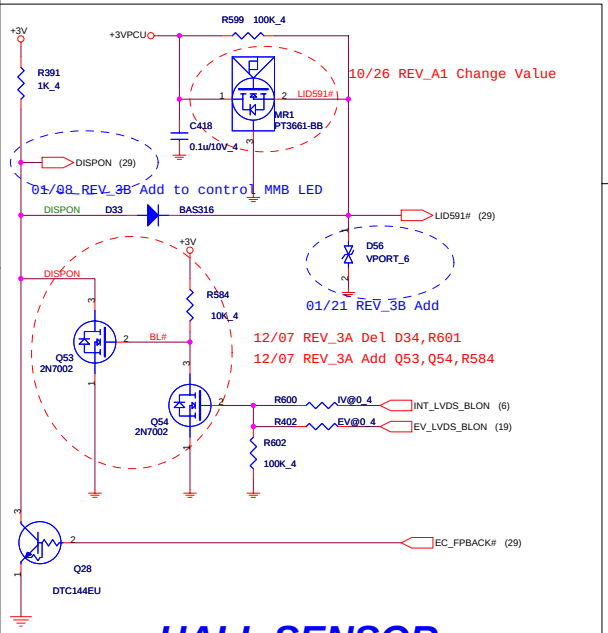
Date: Wednesday, January 23, 2008 Sheet 16 of 37


U33F
ICH8M REV 1.0
U33E
ICH8M REV 1.0
01/21 REV_3B Add
01/21 REV_3B Add
01/21 REV_3B Add
01/21 REV_3B Add
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
Size
Document Number
ICH8M Power(4 of 4)
Rev
1A
Date: Tuesday, January 22, 2008
Sheet 17 of 37

CRT PORT

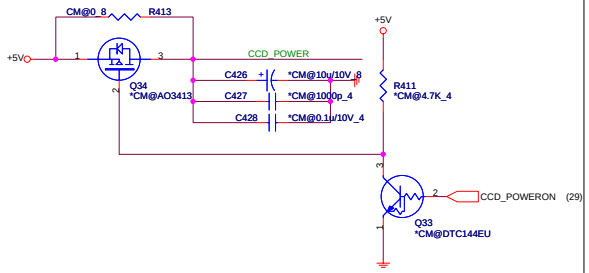


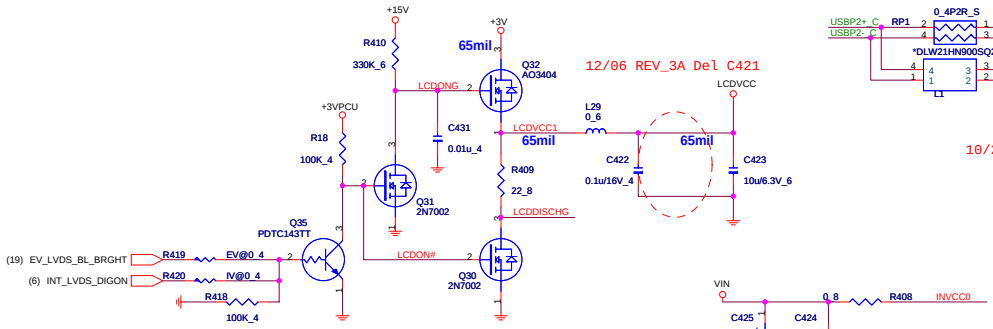


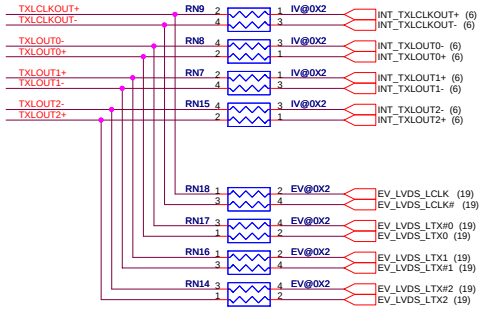


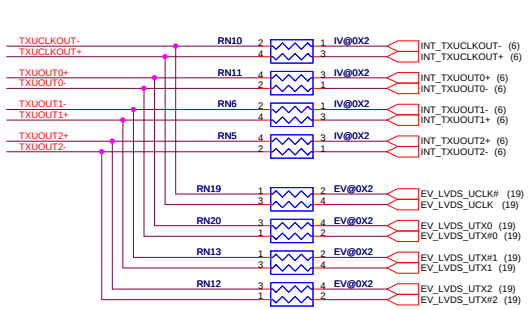
HALL SENSOR

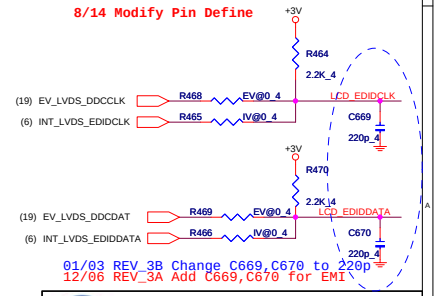
CAMERA MODULE









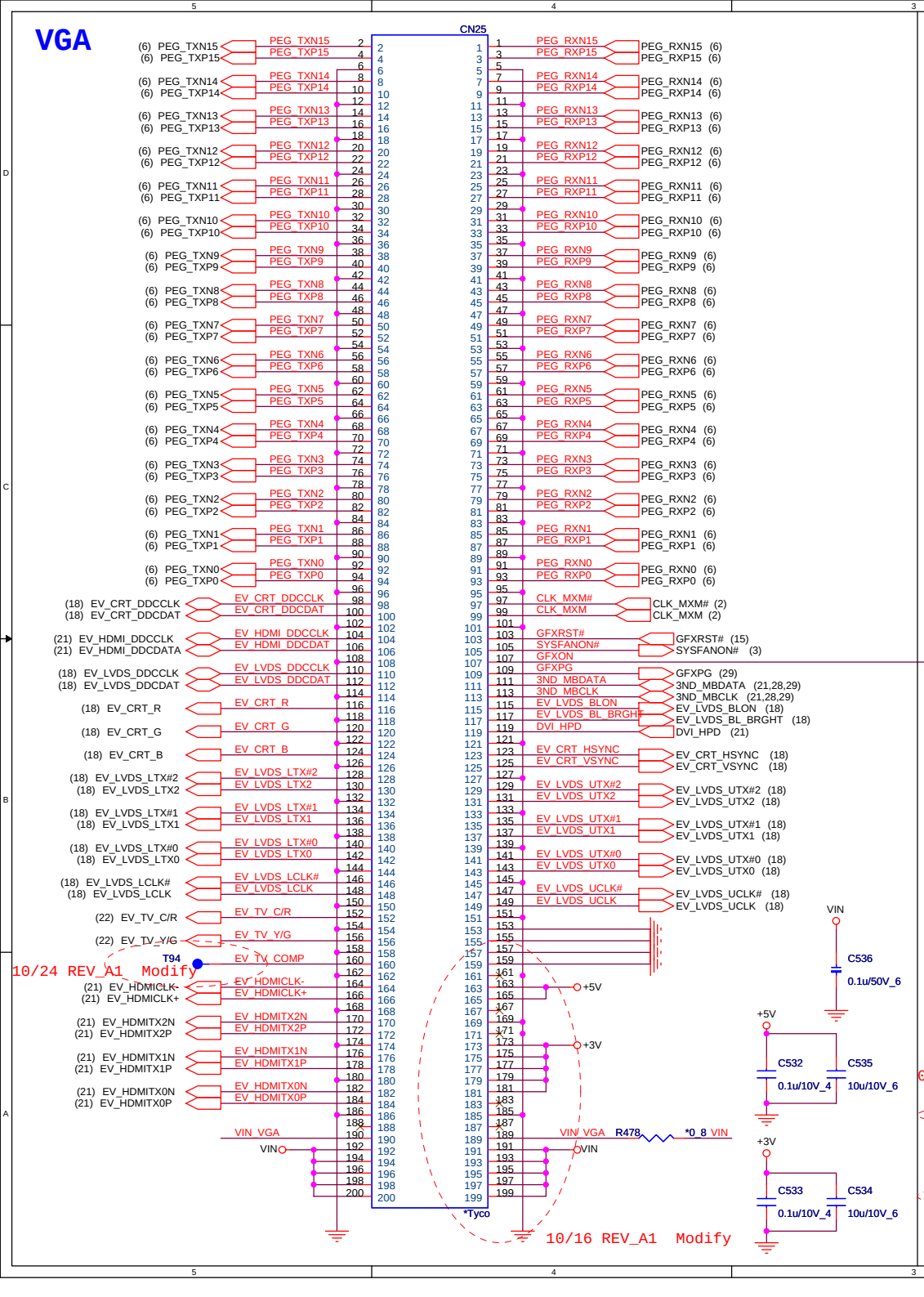


Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

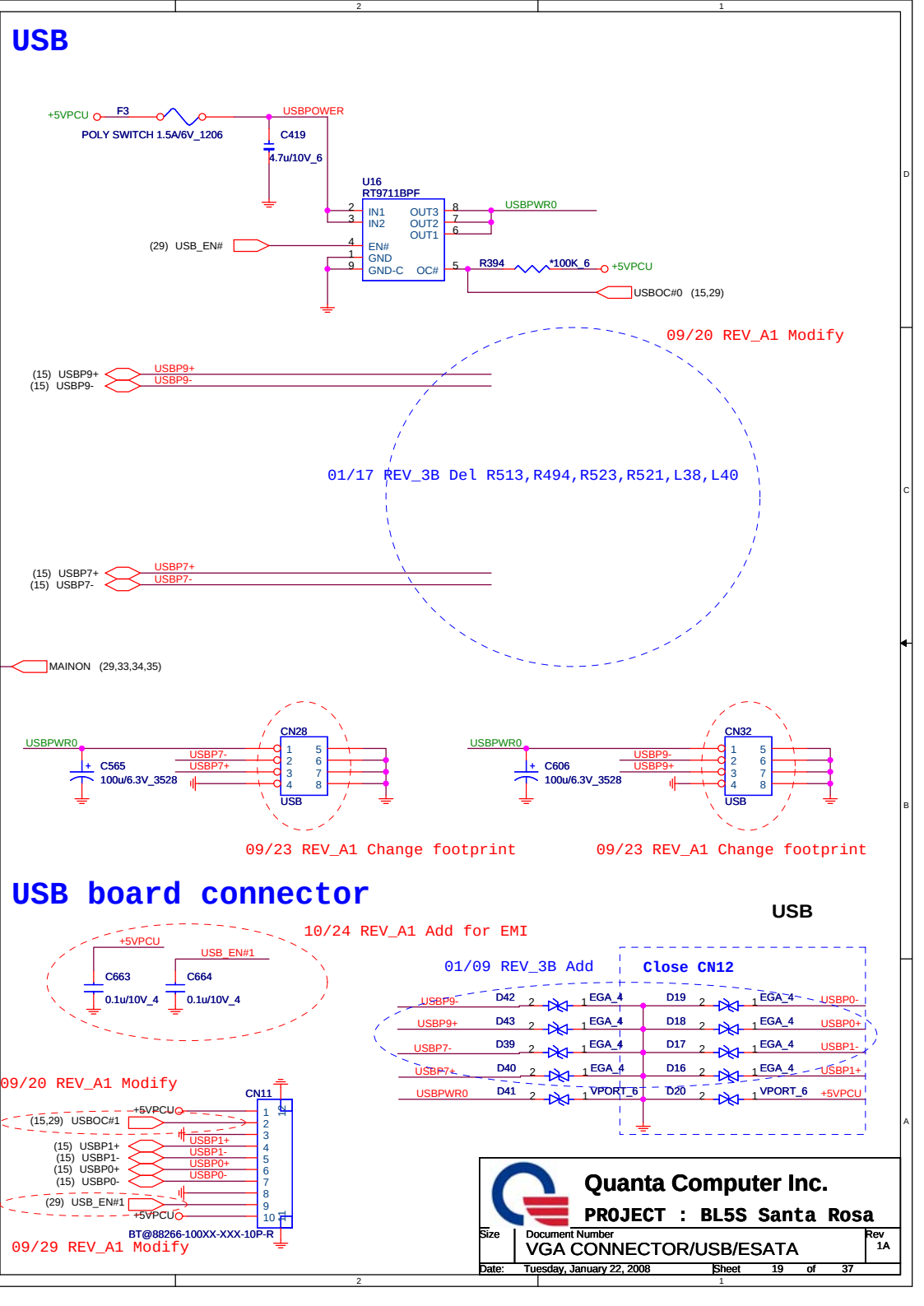
Size	Document Number	Rev
	LCD/CRT/LID/CAMERA	1A

Date: Sunday, February 17, 2008 Sheet 18 of 37

VGA



USB



USB board connector

Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	VGA CONNECTOR/USB/ESATA	1A

Date: Tuesday, January 22, 2008 Sheet 19 of 37

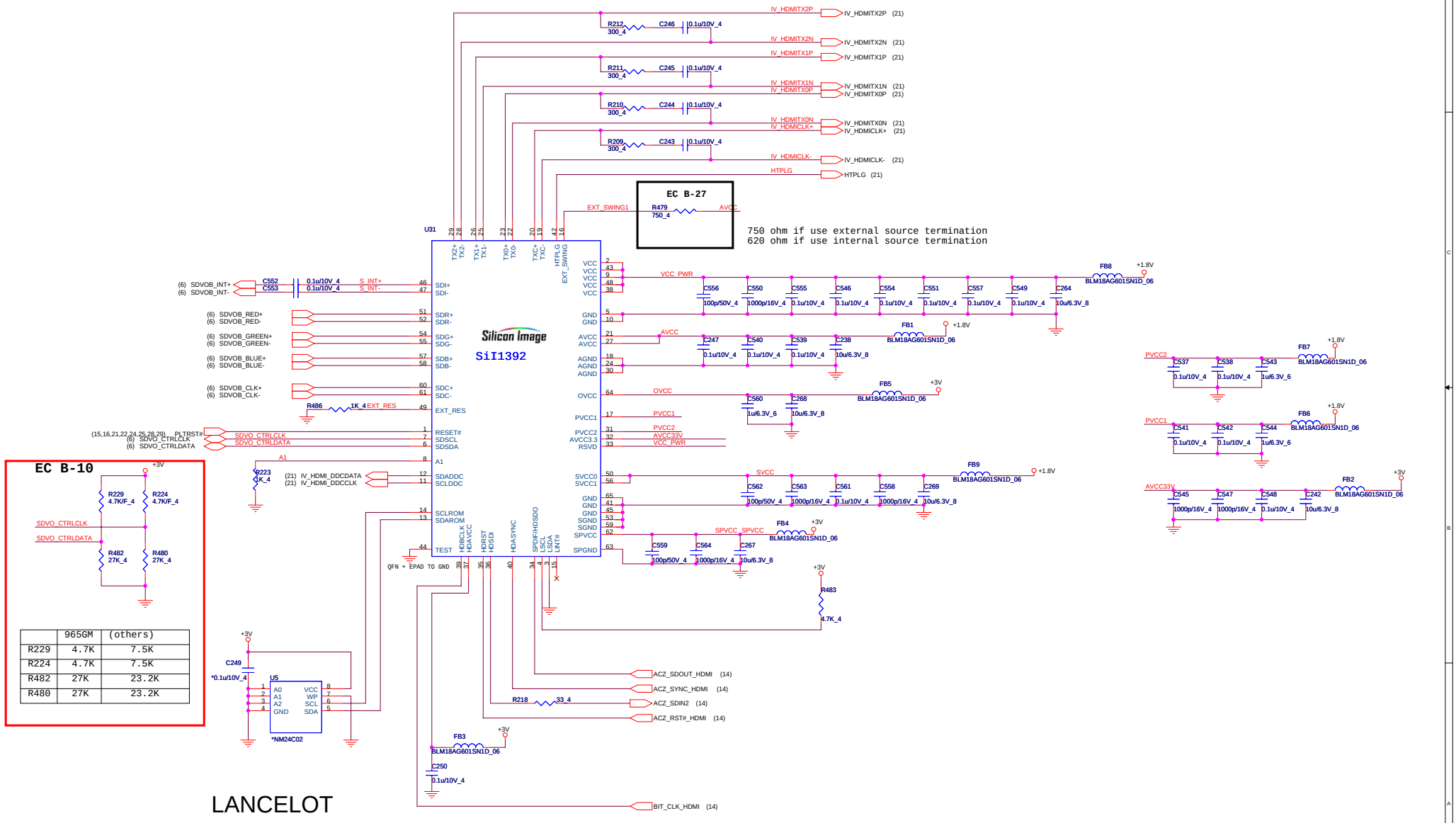
SiI1392 HDMI TX

LAYOUT RULES:

Route traces with 100 Ohm Differential Impedance

Avoid placing GND Copper or traces adjacent to TMDS Trace

Put these 4 resistors and 4 capacitors as close as possible to the TMDS output pins of the Sil1392



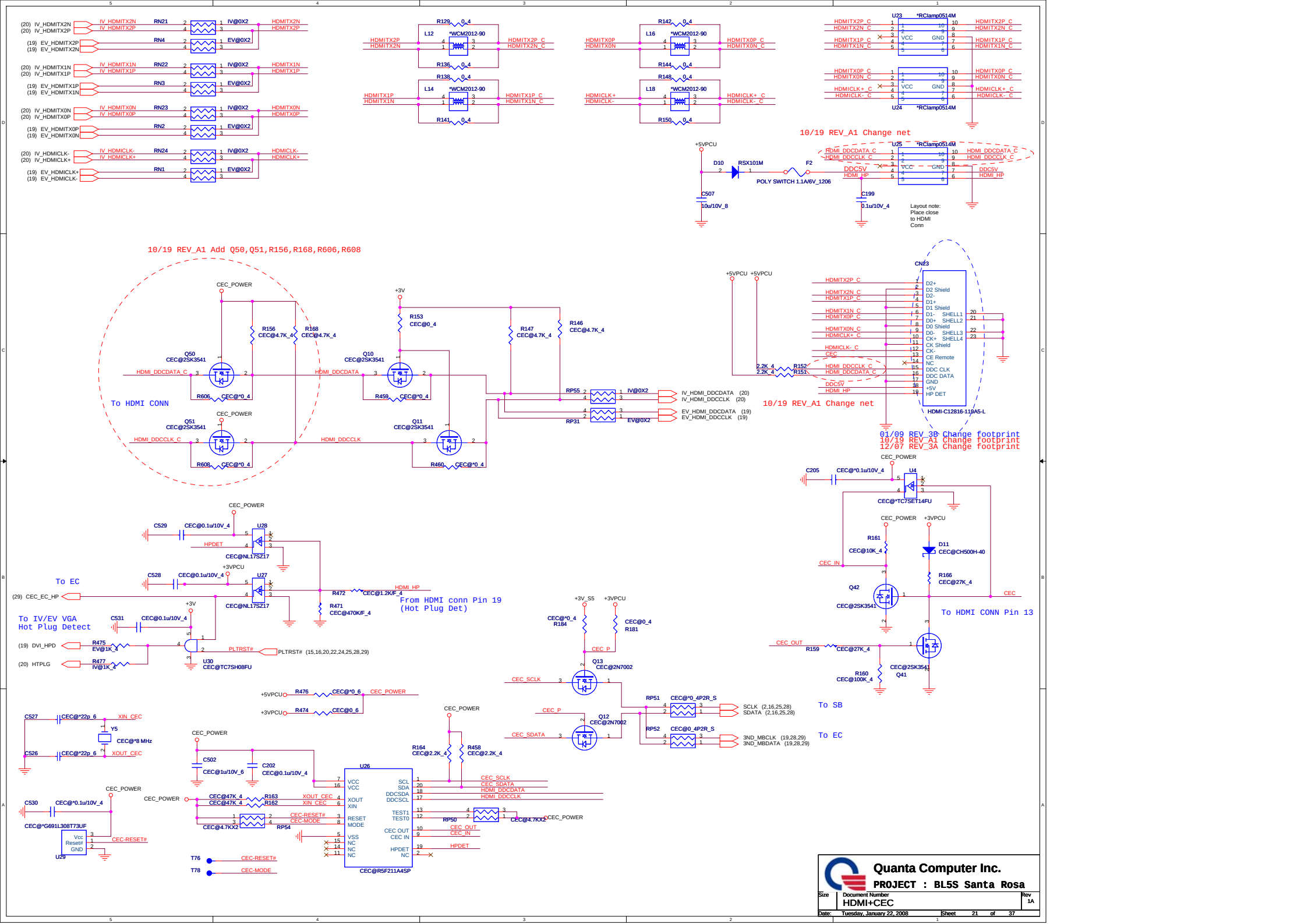
	965GM	(others)
R229	4.7K	7.5K
R224	4.7K	7.5K
R482	27K	23.2K
R480	27K	23.2K

Quanta Computer Inc.

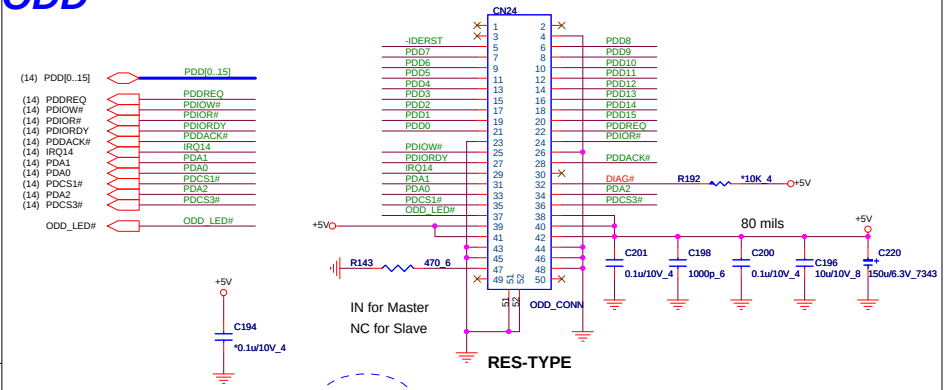
PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	Sil1392(HDMI)	1A

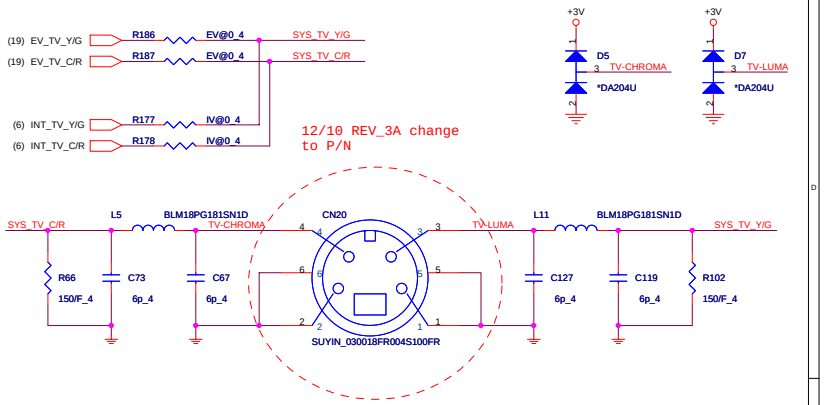
Date: Tuesday, January 22, 2008 Sheet 20 of 37


(20) IV_HDMITX2N
(20) IV_HDMITX2P
(19) EV_HDMITX2P
(19) EV_HDMITX2N
RN21
RN4
IV@0X2
EV@0X2
HDMITX2N
HDMITX2P
(20) IV_HDMITX1N
(20) IV_HDMITX1P
(19) EV_HDMITX1P
(19) EV_HDMITX1N
RN22
RN3
HDMITX1N
HDMITX1P
(20) IV_HDMITX0N
(20) IV_HDMITX0P
(19) EV_HDMITX0P
(19) EV_HDMITX0N
RN23
RN2
HDMITX0N
HDMITX0P
(20) IV_HDMICLK-
(20) IV_HDMICLK+
(19) EV_HDMICLK+
(19) EV_HDMICLK-
RN24
RN1
HDMICLK-
HDMICLK+
R129 0_4
L12 *WCM2012-90
R136 0_4
R138 0_4
L14 *WCM2012-90
R141 0_4
HDMITX2P_C
HDMITX2N_C
HDMITX1P_C
HDMITX1N_C
R142 0_4
L16 *WCM2012-90
R144 0_4
R148 0_4
L18 *WCM2012-90
R150 0_4
HDMITX0P_C
HDMITX0N_C
HDMICLK+_C
HDMICLK-_C
U23 *RClamp0514M
U24 *RClamp0514M
VCC
GND
10/19 REV_A1 Change net
+5VPCU
D10
RSX101M
F2
POLY SWITCH 1.1A/6V_1206
C507
10u/10V_8
C199
0.1u/10V_4
DDC5V
HDMI_HP
HDMI_DDCDATA_C
HDMI_DDCCLK_C
U25 *RClamp0514M
Layout note:
Place close
to HDMI
Conn
10/19 REV_A1 Add Q50,Q51,R156,R168,R606,R608
CEC_POWER
+3V
R153 CEC@0_4
R156 CEC@4.7K_4
R168 CEC@4.7K_4
R147 CEC@4.7K_4
R146 CEC@4.7K_4
Q50 CEC@2SK3541
Q10 CEC@2SK3541
Q51 CEC@2SK3541
Q11 CEC@2SK3541
HDMI_DDCDATA_C
HDMI_DDCDATA
HDMI_DDCCLK_C
HDMI_DDCCLK
R606 CEC@*0_4
R459 CEC@*0_4
R608 CEC@*0_4
R460 CEC@*0_4
To HDMI CONN
RP55 IV@0X2
RP31 EV@0X2
IV_HDMI_DDCDATA (20)
IV_HDMI_DDCCLK (20)
EV_HDMI_DDCDATA (19)
EV_HDMI_DDCCLK (19)
+5VPCU +5VPCU
2.2K_4
R152
R151
CN23
HDMI-C12816-119A5-L
D2+
D2 Shield
D2-
D1+
D1 Shield
D1- SHELL1
D0+ SHELL2
D0 Shield
D0- SHELL3
CK+ SHELL4
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
10/19 REV_A1 Change net
01/09 REV_3B Change footprint
10/19 REV_A1 Change footprint
12/07 REV_3A Change footprint
C205 CEC@*0.1u/10V_4
U4 CEC@*TC7SET14FU
R161 CEC@10K_4
D11 CEC@CH500H-40
R166 CEC@27K_4
Q42 CEC@2SK3541
Q41 CEC@2SK3541
R159 CEC@27K_4
R160 CEC@100K_4
CEC_IN
CEC_OUT
CEC
To HDMI CONN Pin 13
To SB
To EC
C529 CEC@0.1u/10V_4
U28 CEC@NL17SZ17
HPDET
C528 CEC@0.1u/10V_4
U27 CEC@NL17SZ17
R472 CEC@1.2K/F_4
R471 CEC@470K/F_4
HDMI_HP
To EC
(29) CEC_EC_HP
From HDMI conn Pin 19
(Hot Plug Det)
To IV/EV VGA
Hot Plug Detect
C531 CEC@0.1u/10V_4
(19) DVI_HPD
(20) HTPLG
R475 EV@1K_4
R477 IV@1K_4
U30 CEC@TC7SH08FU
PLTRST#
PLTRST# (15,16,20,22,24,25,28,29)
+3V_S5 +3VPCU
CEC@*0_4 R184
CEC@0_4 R181
CEC_P
Q13 CEC@2N7002
CEC_SCLK
Q12 CEC@2N7002
CEC_SDATA
RP51 CEC@*0_4P2R_S
RP52 CEC@0_4P2R_S
SCLK (2,16,25,28)
SDATA (2,16,25,28)
3ND_MBCLK (19,28,29)
3ND_MBDATA (19,28,29)
+5VPCU R476 CEC@*0_6 CEC_POWER
+3VPCU R474 CEC@0_6
C527 CEC@*22p_6
C526 CEC@*22p_6
Y5
CEC@*8 MHz
XIN_CEC
XOUT_CEC
C502 CEC@1u/10V_6
C202 CEC@0.1u/10V_4
R164 CEC@2.2K_4
R458 CEC@2.2K_4
U26 CEC@R5F211A4SP
VCC
XOUT
XIN
RESET
MODE
VSS
NC
SCL
SDA
DDCSDA
DDCSCL
TEST1
TEST0
CEC OUT
CEC IN
HPDET
C530 CEC@*0.1u/10V_4
CEC@*G691L308T73UF
U29
CEC-RESET#
R163 CEC@47K_4
R162 CEC@47K_4
XOUT_CEC
XIN_CEC
CEC-RESET#
CEC-MODE
RP54 CEC@4.7KX2
RP50 CEC@4.7KX2
CEC_SCLK
CEC_SDATA
HDMI_DDCDATA
HDMI_DDCCLK
CEC_OUT
CEC_IN
HPDET
T76 CEC-RESET#
T78 CEC-MODE
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
Size
Document Number
HDMI+CEC
Rev
1A
Date: Tuesday, January 22, 2008
Sheet 21 of 37

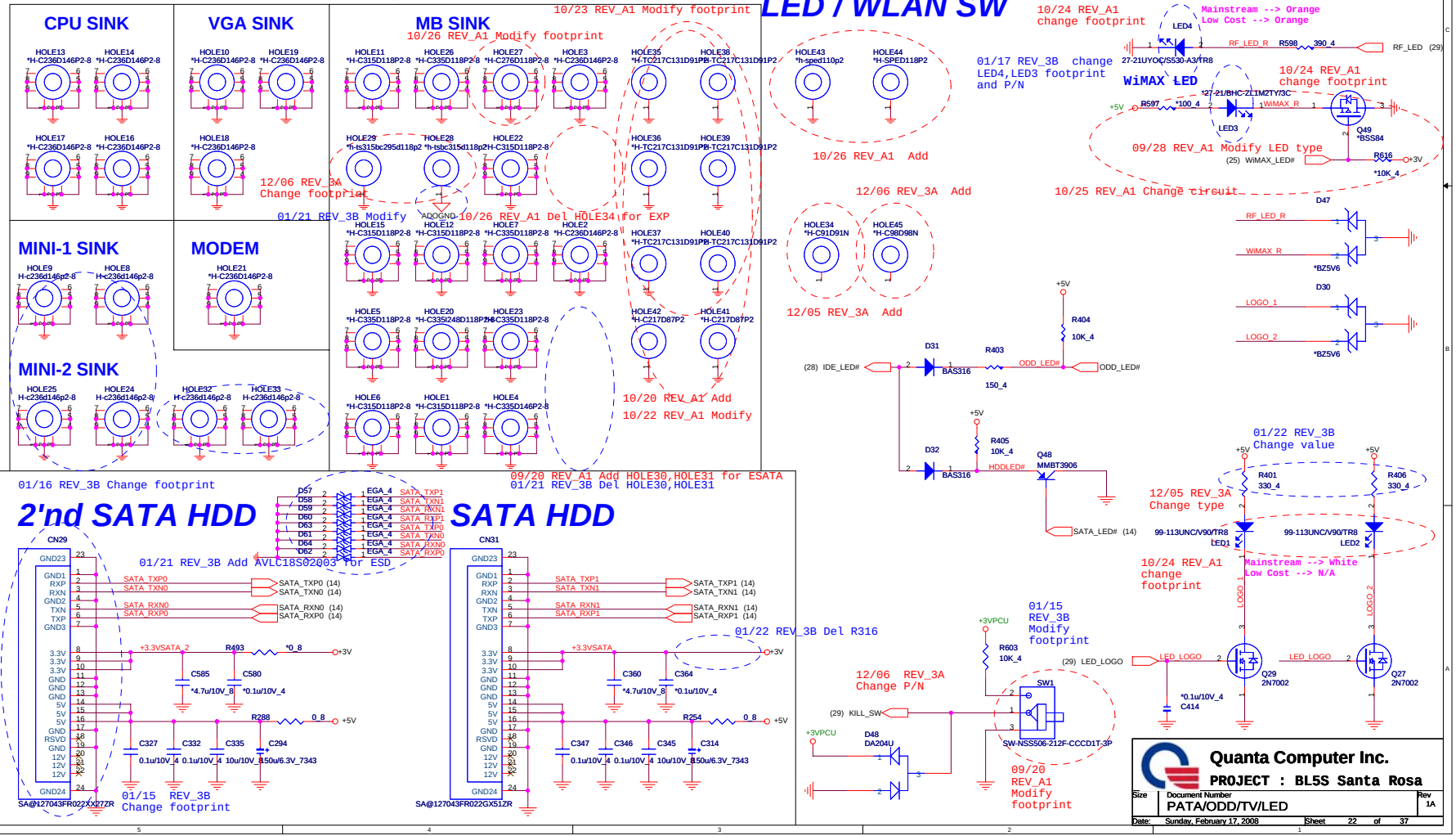
ODD



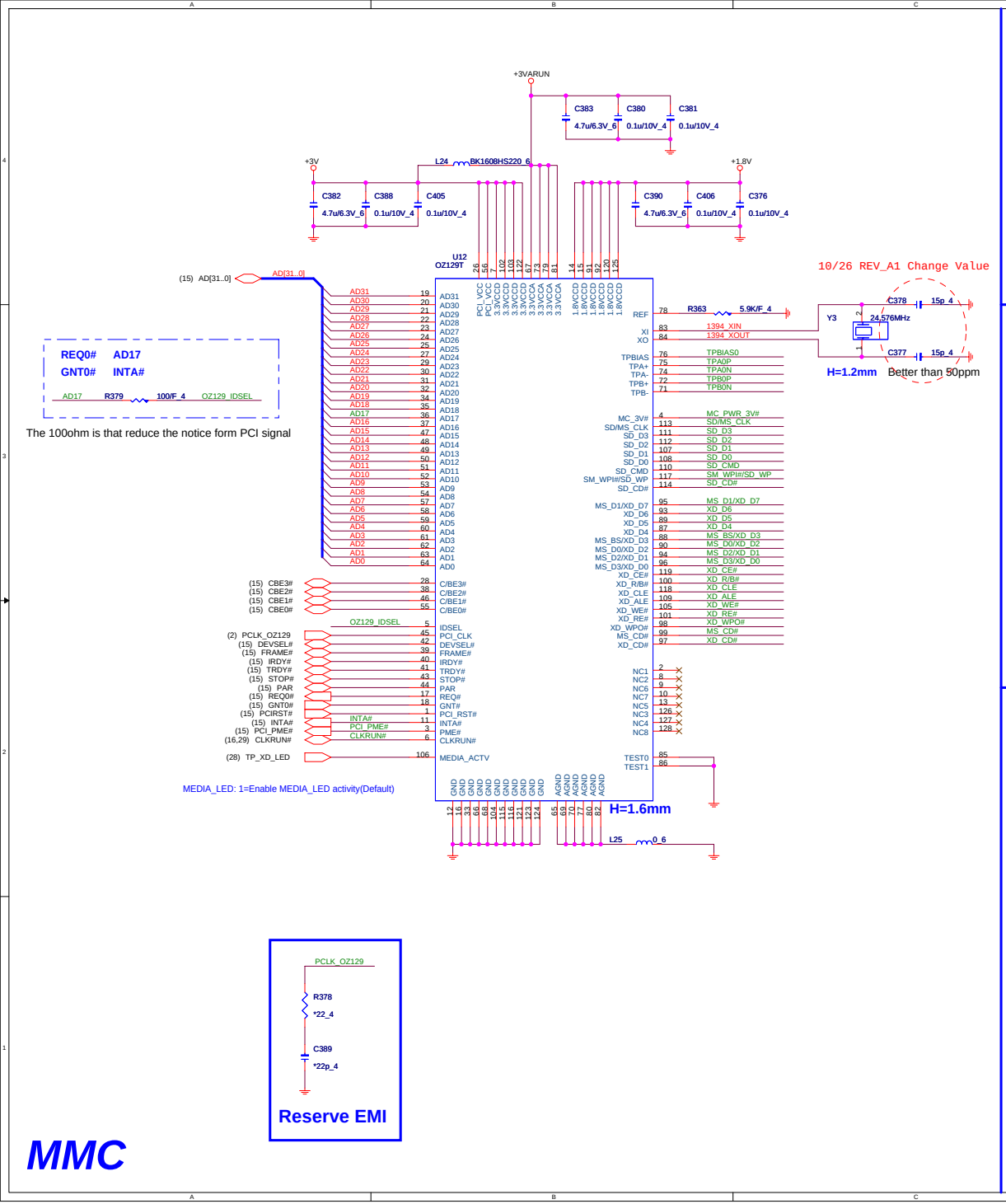
TVOUT



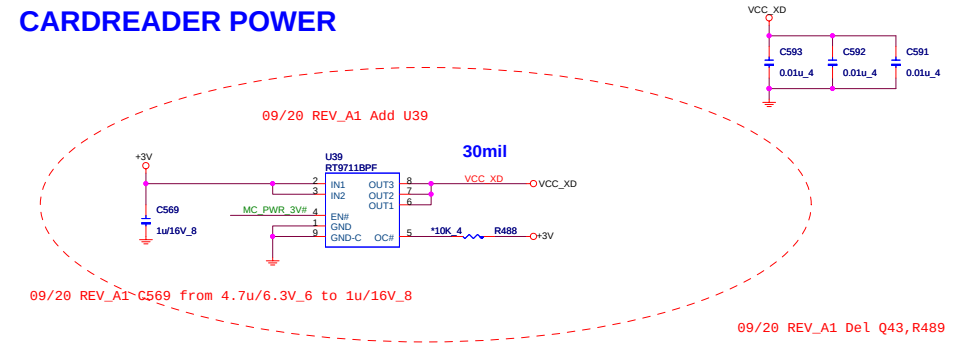
LED / WLAN SW



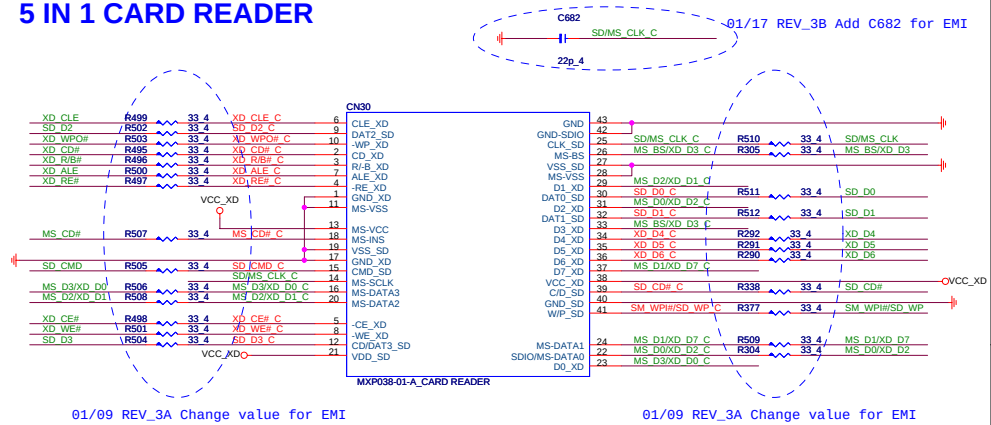
Quanta Computer Inc.			
PROJECT : BL5S Santa Rosa			
Size	Document Number		Rev
	PATA/ODD/TV/LED		1A
Date: Sunday, February 17, 2008	Sheet 22 of 37		



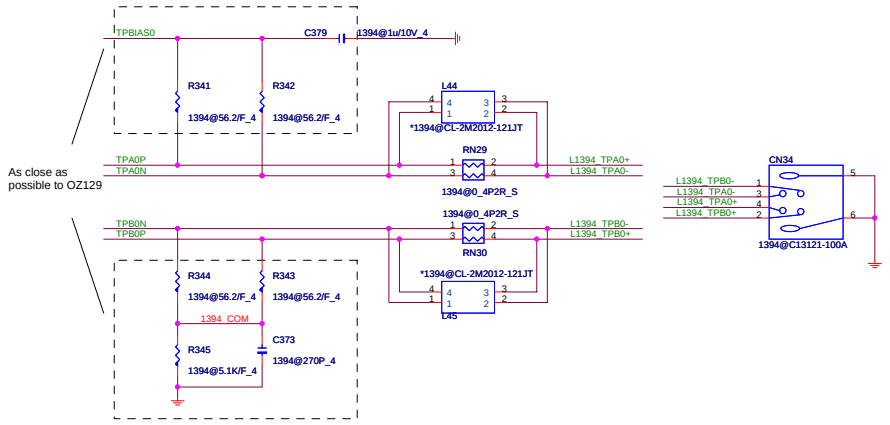
CARDREADER POWER



5 IN 1 CARD READER



1394



Quanta Computer Inc.		
PROJECT : BL5S Santa Rosa		
Size	Document Number: OZ129T (Card Reader/1394)	Rev 1A
Date: Tuesday, January 22, 2008	Sheet 23 of 37	

LAN_MARVELL_88E8040/88E8055/88E8072

10/100 : 88E8040 P/N : AL008040001
GIGA : 88E8055 P/N : AJ080550000
GIGA : 88E8072 P/N : AL008072000

U32

88E805X

88E8040T

LAN_RSET
2K Ohm for 8040
4.87K Ohm for 8055/8072

12/05 REV_3A Add D6

10/24 REV_A1 Add

10/24 REV_A1 Modify

H = 0.8mm

25 mil Trace width

25 mil Trace width

12/10 REV_3A DNI R485,R484,U7
Mount R481

EEPROM No Use
VPD_DATA Pull Down

01/16 REV_3B change footprint

TERMINATION PLANE

DELTA ~~10/100 : LFE8696-R P/N : DB0MA8LAN00~~
H = 4mm ~~GIGA : LFE9249-R P/N : DB0ZR1LAN11~~

HWS ~~10/100 : HPL-4001B P/N : DB0SA1LAN01~~
H = 4mm GIGA : HPL-68 P/N : DB0ZB1LAN12

BOTHHAND 10/100 : TST1284 LF P/N : DB0KN7LAN24
H = 4mm ~~GIGA : GST5009-LF P/N : DBKN1NLAN03~~

Quanta Computer Inc.			
PROJECT : BL5S Santa Rosa			
Size	Document Number		Rev
	LAN_Marvell_8040/8055		1A
Date: Tuesday, January 22, 2008		Sheet 24 of 37	

Mini PCI-E Card
WLAN

MINI-Card I

09/28 REV_A1 Modify

02/15 REV_3C Modify

10/26 REV_A1 Modify

09/28 REV_A1 Modify

(16,29) SERIRQ
(14) LDRQ#1
(15,16,20,21,22,24,28,29) PLTRST#
(2) PCLK_DEBUG

SERIRQ R375 *0 4
LDRQ#1 R221 *0 4
PLTRST# R553 *0 4
PCLK_DEBUG R339 *0 4

SERIRQ_WLAN
CL_RST#1_MIN
CL_DATA1_MIN
CL_CLK1_MIN

(16) CL_RST#1
(16) CL_DATA1
(16) CL_CLK1

T72
R331 *0 4
R348 *0 4
R349 *0 4

T69
T68
R426 0 4

(15) PCIE_TXP1
(15) PCIE_TXN1
PCIE_TXP1
PCIE_TXN1

(15) PCIE_RXP1
(15) PCIE_RXN1
PCIE_RXP1
PCIE_RXN1

T67
T66

(2) CLK_PCIE_MINI
(2) CLK_PCIE_MINI#
CLK_PCIE_MINI
CLK_PCIE_MINI#

(28) WCS_CLK
(28) WCS_DAT
WCS_CLK R425 BT@0 4 WCS_CLKR
WCS_DAT R424 BT@0 4 WCS_DATR
WLAN_WAKE#

To BT

2N7002E-LF
Q1
(16,24,28) PCIE_WAKE#
WLAN_WAKE#
+3V_S5
R8 10K_4

CN19
minipal-c15706-52p-ldv

NC
C-Link_RST
C-Link_DAT
C-Link_CLK
GND
NC
NC
GND
GND
PETp0
PETn0
GND
GND
PERp0
PERn0
GND
NC
NC
GND
REFCLK+
REFCLK-
GND
CLKREQ#
BT_CHCLK
BT_DATA
WAKE#
+3.3V
GND
+1.5V
LED_WPAN#
LED_WLAN#
NC
NC
USB_D+
USB_D-
GND
SMB_DATA
SMB_CLK
+1.5V
GND
+3.3Vaux
PERST#
W_DISABLE#
GND
NC
NC
NC
NC
NC
+1.5V
GND
+3.3V

WL_SMDATA
WL_SMCLK

WiMAX_LED# B
R14 *0 4
R13 WiMAX_LED#
WiMAX_LED# (22)

USBP3+ B
USBP3- B
0 4 R11 USBP3+
0 4 R9 USBP3-
USBP3+ (15)
USBP3- (15)

T2
T3

PLTRST#
RF_EN_WLAN R7 0 4
PLTRST# (15,16,20,21,22,24,28,29)
RF_EN (29)

LFRAME# PCIE *0 4 R199 LFRAME#
LAD3_PCIE *0 4 R198 LAD3
LAD2_PCIE *0 4 R200 LAD2
LAD1_PCIE *0 4 R201 LAD1
LAD0_PCIE *0 4 R202 LAD0
LFRAME# (14,29)
LAD3 (14,29)
LAD2 (14,29)
LAD1 (14,29)
LAD0 (14,29)

C22 0.1u/10V_4
C16 10u/10V_8
C20 0.001u_4
C21 0.1u/10V_4
C19 10u/10V_8

Q5 2N7002E
Q3 2N7002E
Q4 2N7002E
Q2 2N7002E
RP4 4.7KX2
RP3 4.7KX2
(2,16,21,28) SDATA
(2,16,21,28) SCLK
WL_SMDATA
WL_SMCLK
MINI2_SMDATA
MINI2_SMCLK

MINI-Card II

09/20 REV_A1 Modify

CN39
3G@minipal-c15706-52p-ldv

Reserved
+3.3V
GND
+1.5V
LED_WPAN#
LED_WLAN#
LED_WWAN#
+3.3Vaux
USB_D+
USB_D-
PETp0
PETn0
SMB_DATA
SMB_CLK
PERp0
PERn0
PERST#
W_DISABLE#
UIM_VPP
UIM_RESET
UIM_CLK
UIM_DATA
UIM_PWR
REFCLK+
REFCLK-
CLKREQ#
WAKE#

0 4 R10
(15) PCIE_TXP3
(15) PCIE_TXN3
PCIE_TXP3
PCIE_TXN3

(15) PCIE_RXP3
(15) PCIE_RXN3
PCIE_RXP3
PCIE_RXN3

(2) CLK_PCIE_MINI2
(2) CLK_PCIE_MINI2#
CLK_PCIE_MINI2
CLK_PCIE_MINI2#

*0 4 R12
T1
T71
T70

MINI2_SMDATA
MINI2_SMCLK

PLTRST#
0 4 R15
PLTRST# (15,16,20,21,22,24,28,29)
RF_EN (29)

C469 0.1u/10V_4
C641 10u/10V_8
C385 0.001u_4
C361 0.1u/10V_4
C384 10u/10V_8

MINI-Card III

CN33
minipal-c15706-52p-ldv

R314 0 4
(15) PCIE_TXP5
(15) PCIE_TXN5
PCIE_TXP5
PCIE_TXN5

(15) PCIE_RXP5
(15) PCIE_RXN5
PCIE_RXP5
PCIE_RXN5

(2) CLK_PCIE_MINI3
(2) CLK_PCIE_MINI3#
CLK_PCIE_MINI3
CLK_PCIE_MINI3#

T91
T92
T93

R329 *0 4
T57
T58

MINI3_SMDATA
MINI3_SMCLK

PLTRST#
RF_EN_WLAN
PLTRST# (15,16,20,21,22,24,28,29)

Q46 2N7002E
Q45 2N7002E
RP57 4.7KX2
(2,16,21,28) SDATA
(2,16,21,28) SCLK
MINI3_SMDATA
MINI3_SMCLK

H= 8mm

EMI

01/18 REV_3B Add PAD

PAD1
EMIPAD

12/07 REV_3A Add

VIN
C675 C676 C677 C678 C679 C680 C681
0.1u/50V_6

+1.5V
C30 C262 C251 C372 C23
0.1u/10V_4

+3VPCU
C41 C162 C11 C15 C231 C72 C615
0.1u/10V_4

+5V
+3AVDD
C14 C441 C12 C2 C673
0.1u/10V_4

12/07 REV_3A Add

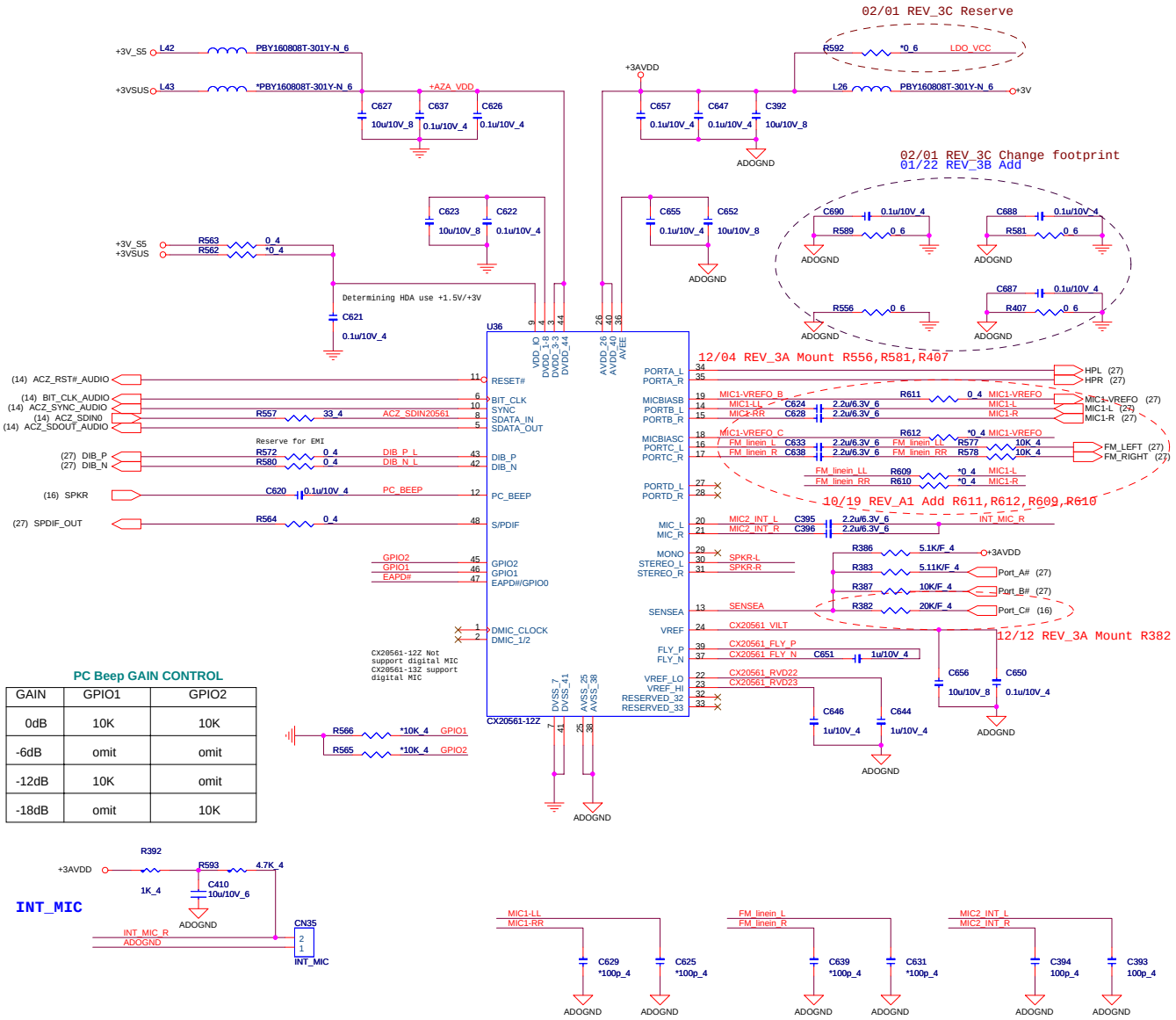
+5VPCU
C407 C252 C195 C18
0.1u/10V_4

Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	MINI PCIE/HOLE	1A

Date: Sunday, February 17, 2008 Sheet 25 of 37

Codec(CX20561)

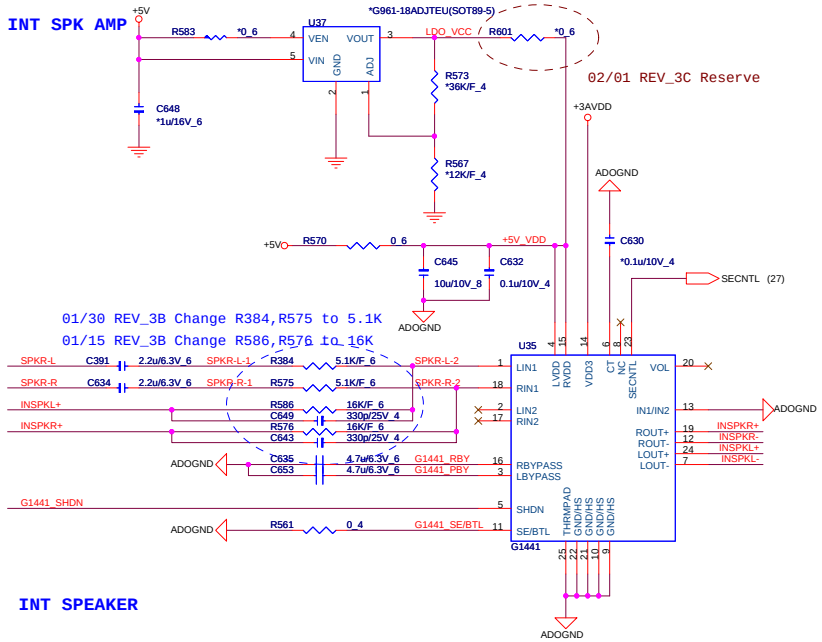


PC Beep GAIN CONTROL

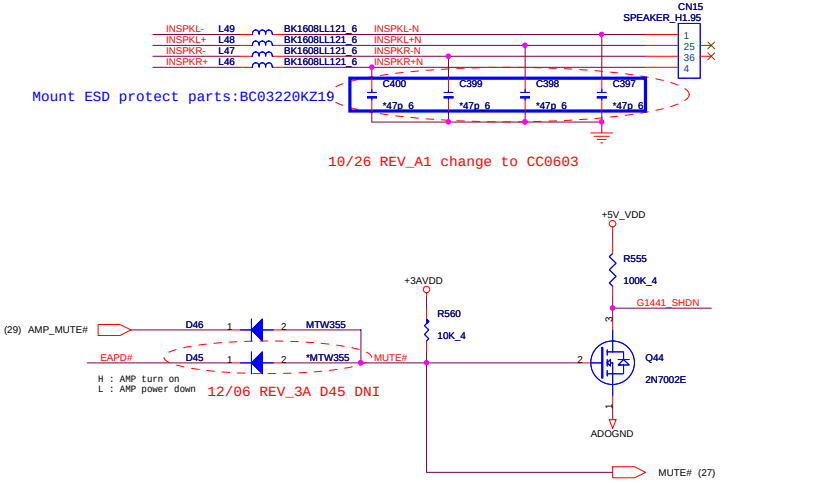
GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

INT_MIC

INT SPK AMP



INT SPEAKER



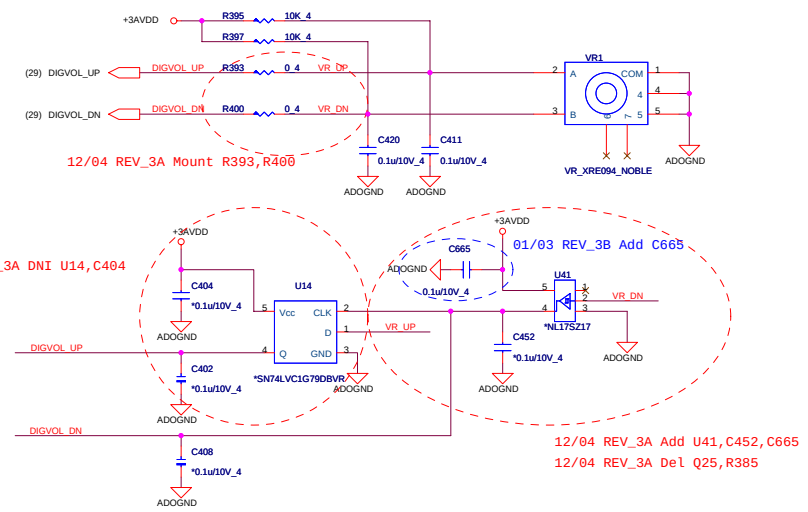
Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

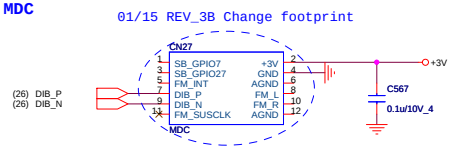
Size	Document Number	Rev
	Conexant CX205601	1A

Date: Sunday, February 17, 2008 Sheet 26 of 37

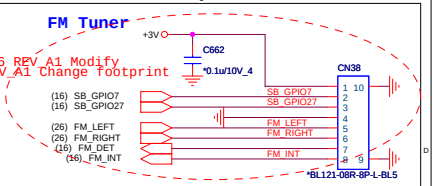
VR



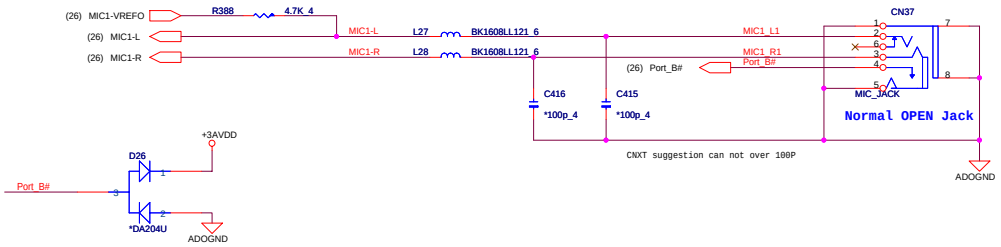
MDC



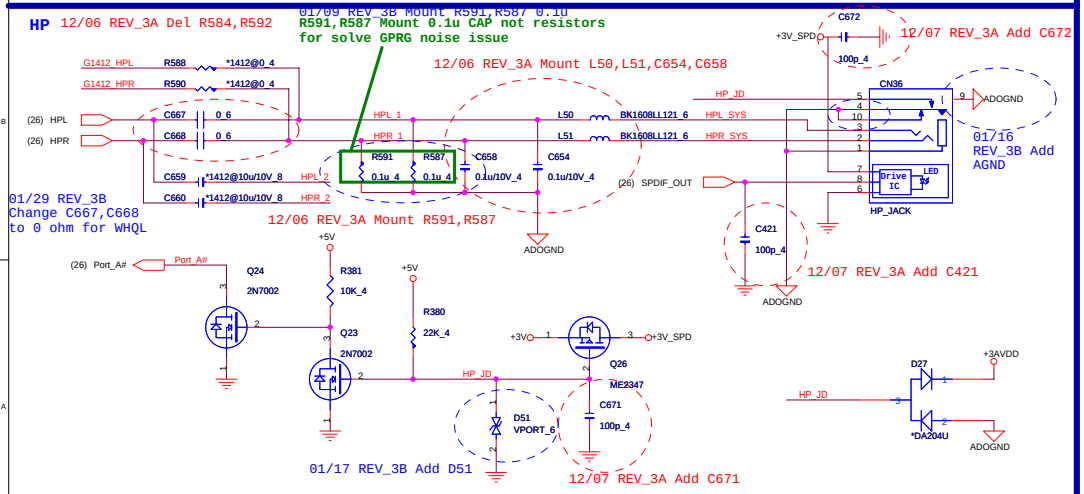
FM Tuner



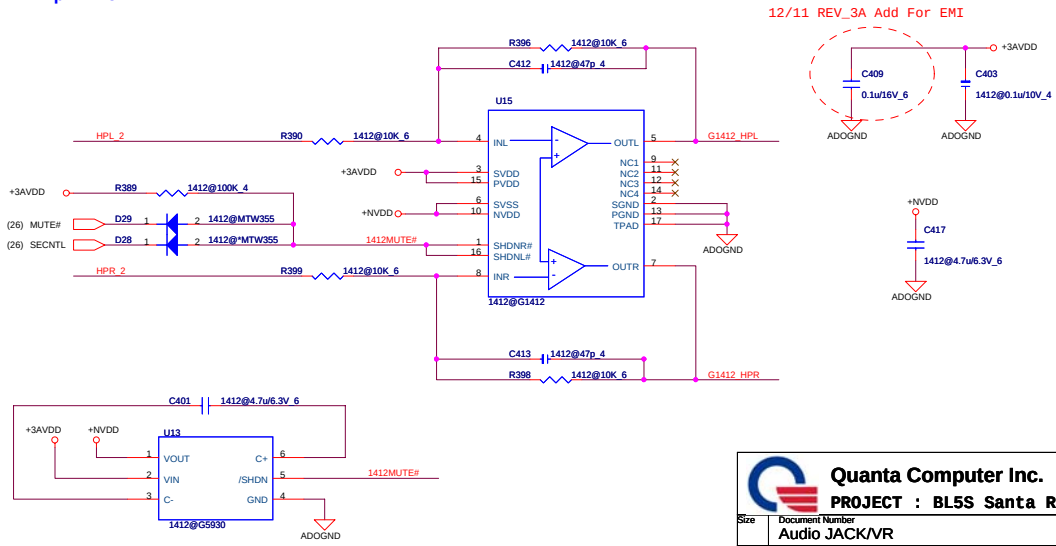
SYSTEM MIC



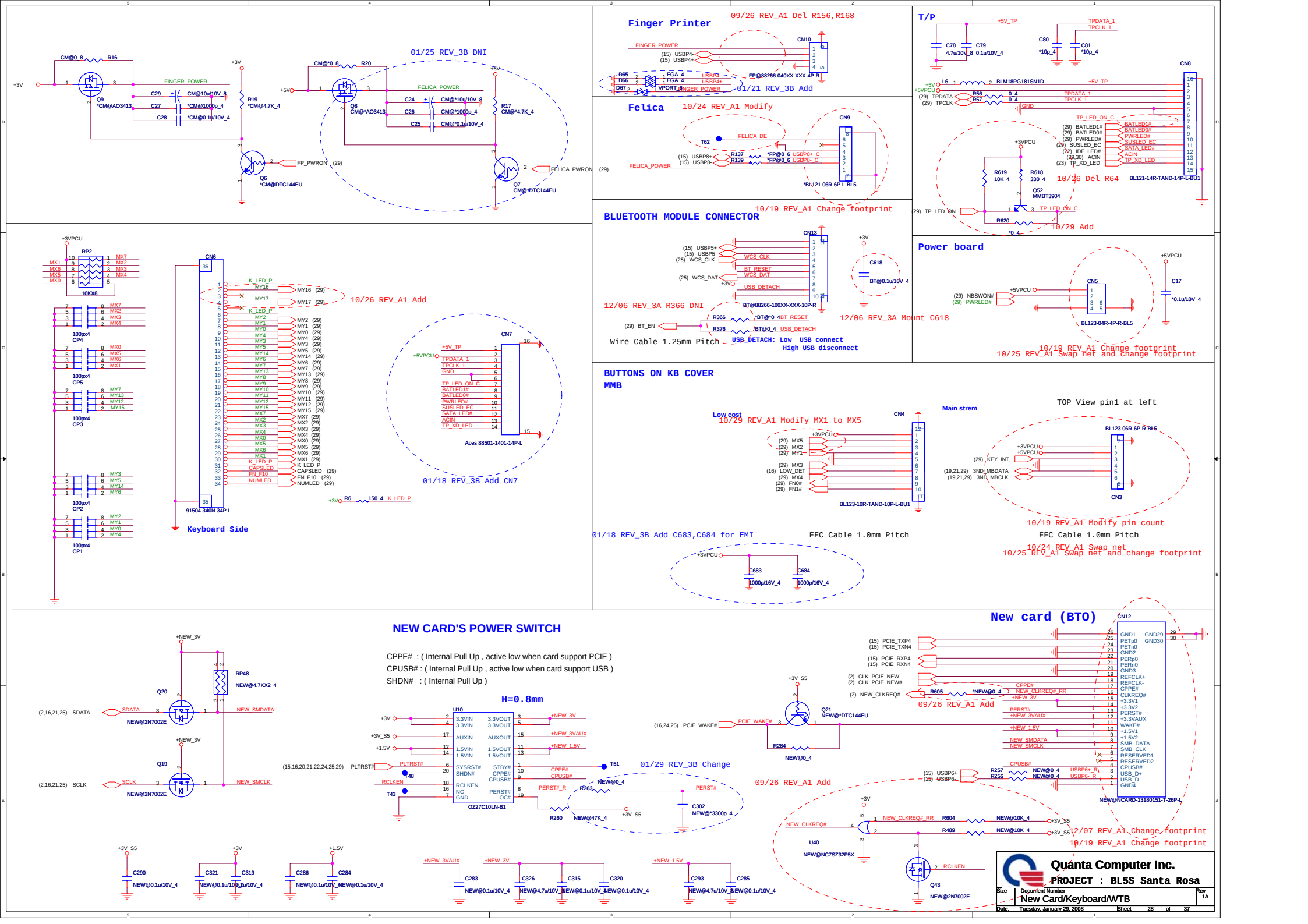
HP



HP Amplifier



Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
Size | Document Number: Audio JACK/VR | Rev: 1A
Date: Sunday, February 17, 2008 | Sheet 27 of 37


Finger Printer
09/26 REV_A1 Del R156,R168
01/21 REV_3B Add
T/P
Felica
10/24 REV_A1 Modify
10/19 REV_A1 Change footprint
BLUETOOTH MODULE CONNECTOR
12/06 REV_3A R366 DNI
12/06 REV_3A Mount C618
Wire Cable 1.25mm Pitch
USB_DETACH: Low USB connect
High USB disconnect
Power board
10/19 REV_A1 Change footprint
10/25 REV_A1 Swap net and change footprint
01/25 REV_3B DNI
10/26 REV_A1 Add
01/18 REV_3B Add CN7
Keyboard Side
BUTTONS ON KB COVER
MMB
Low cost
10/29 REV_A1 Modify MX1 to MX5
Main strem
TOP View pin1 at left
10/19 REV_A1 Modify pin count
FFC Cable 1.0mm Pitch
10/24 REV_A1 Swap net
10/25 REV_A1 Swap net and change footprint
01/18 REV_3B Add C683,C684 for EMI
FFC Cable 1.0mm Pitch
NEW CARD'S POWER SWITCH
CPPE# : (Internal Pull Up , active low when card support PCIE)
CPUSB# : (Internal Pull Up , active low when card support USB)
SHDN# : (Internal Pull Up)
H=0.8mm
01/29 REV_3B Change
New card (BTO)
09/26 REV_A1 Add
12/07 REV_A1 Change footprint
10/19 REV_A1 Change footprint
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
New Card/Keyboard/WTB
Tuesday, January 29, 2008
Sheet 28 of 37

10/26 REV_A1 Add R64,R73,R176

SMBUS Table

SMBUS	Devices
1	Battery
2	CPU Thermal Sensor 3D Sensor EC EEPROM
3	VGA Board Thermal Sensor Touch Sensor

10/26 REV_A1 Modify

10/22 REV_A1 Modify

09/29 REV_A1 Modify

09/20 REV_A1 Modify

10/24 REV_A1 Add

01/08 REV_3B Add to control MMB LED

10/22 REV_A1 Modify

10/22 REV_A1 Modify

09/20 REV_A1 Modify

SM BUS PU

I/O Base Address

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

12/05 REV_3A R38 DNI,R47 mount

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID

H=1.75mm

ADDRESS: A0H

SPI FLASH

H=2.16mm

INTERNAL KEYBOARD STRIP SET

CIR (Copy from PB2A)

Only for 8769/775C

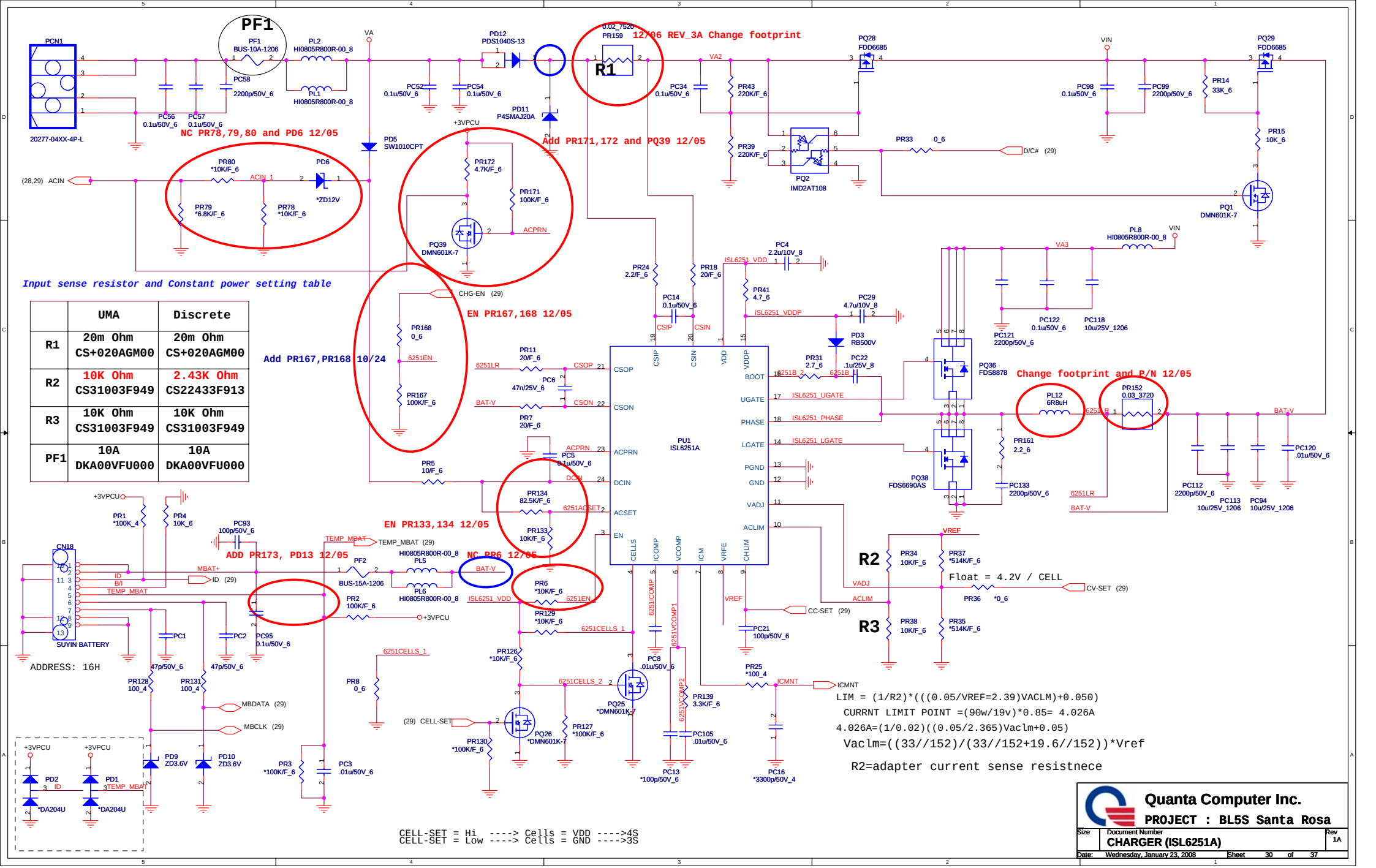
10/19 REV_A1 Change footprint
10/21 REV_A1 Change pin define
12/07 REV_3A Change P/N

WPC8763LDG:	AL008763B00
WPC8769LDG:	AJ087690F08
WPCE775L:	AJ007750F00
WPCE775C:	AJ007750F01

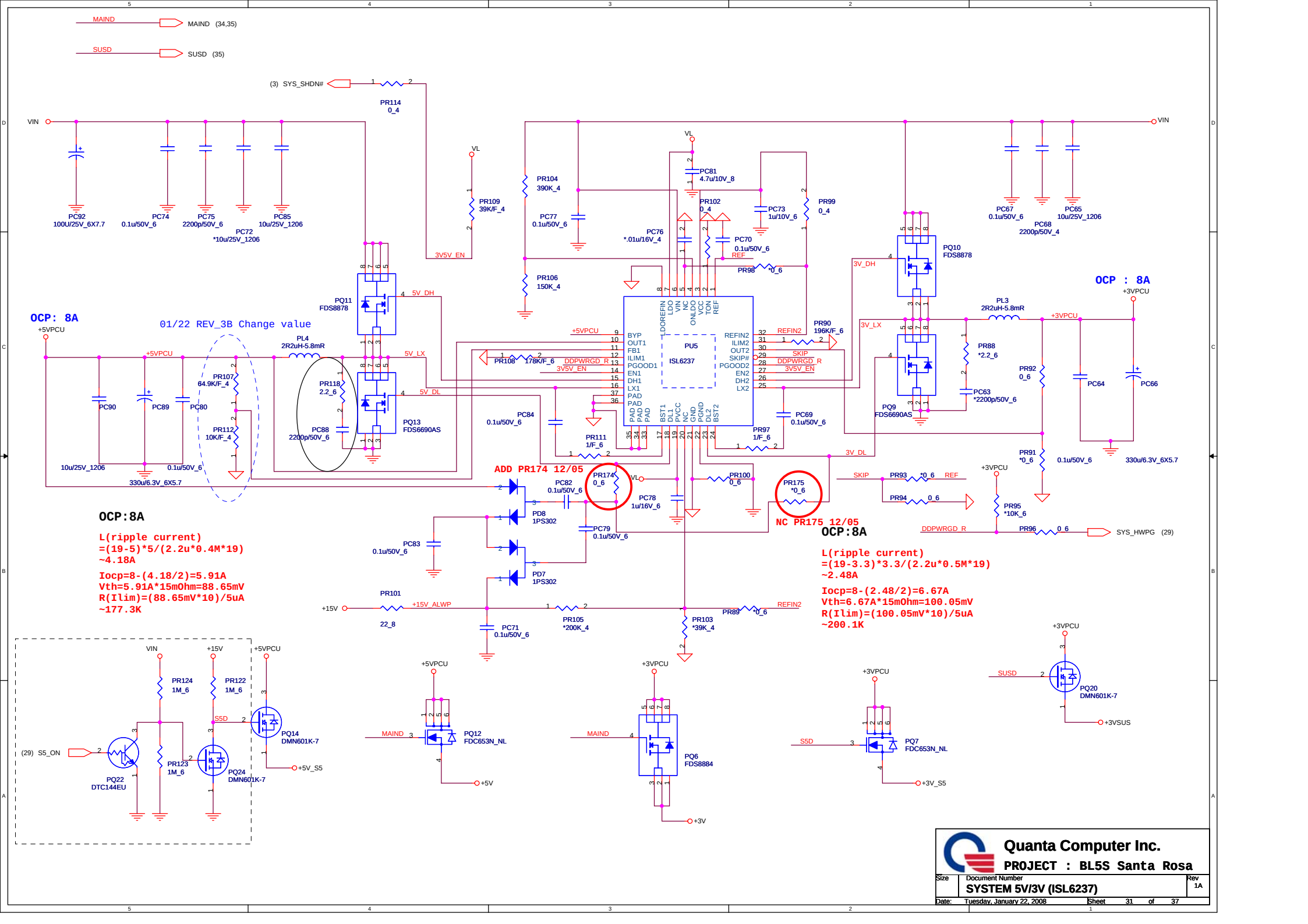
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

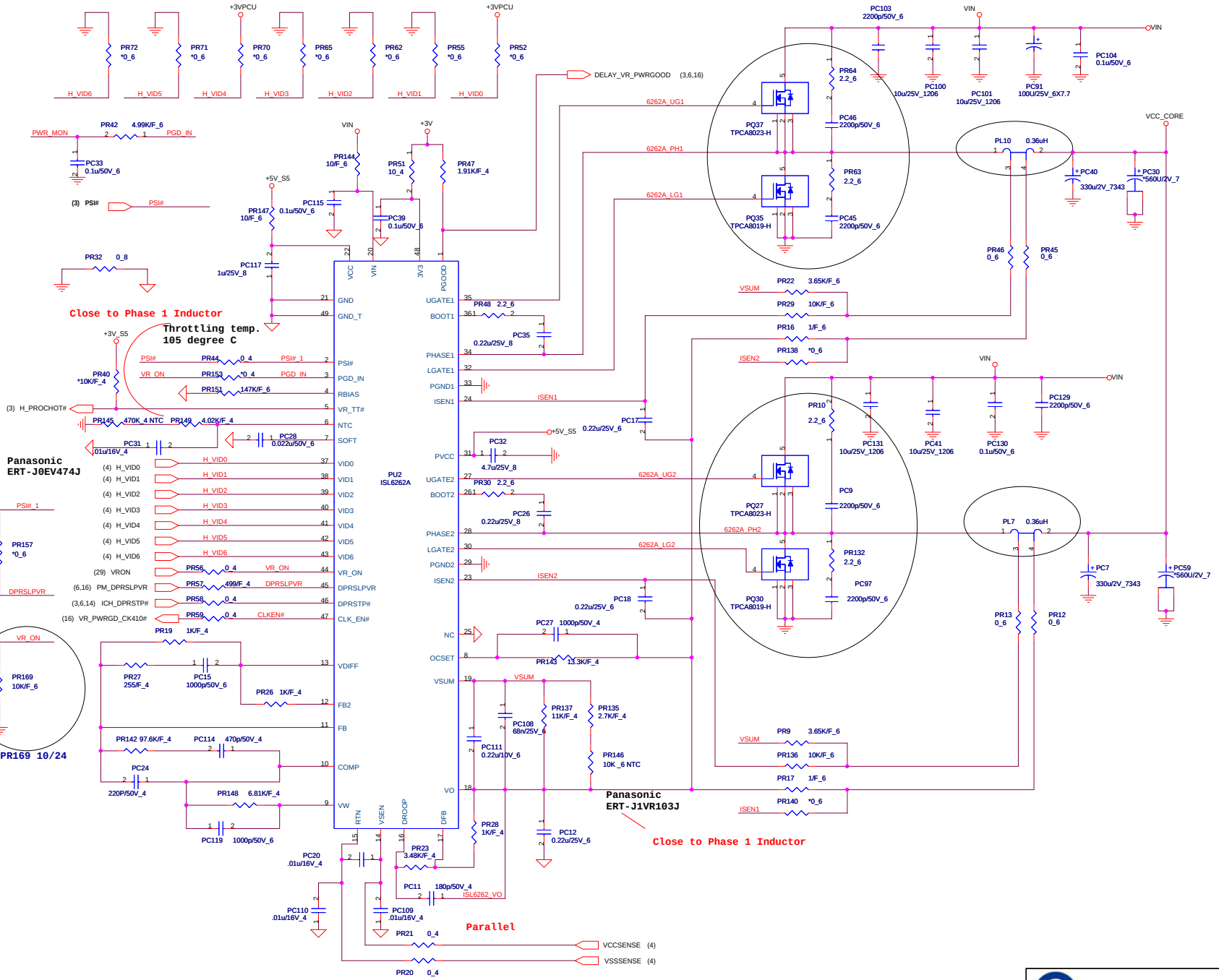
Size	Document Number	Rev
	EC-WPCE775C	1A

Date: Tuesday, January 22, 2008 Sheet 29 of 37

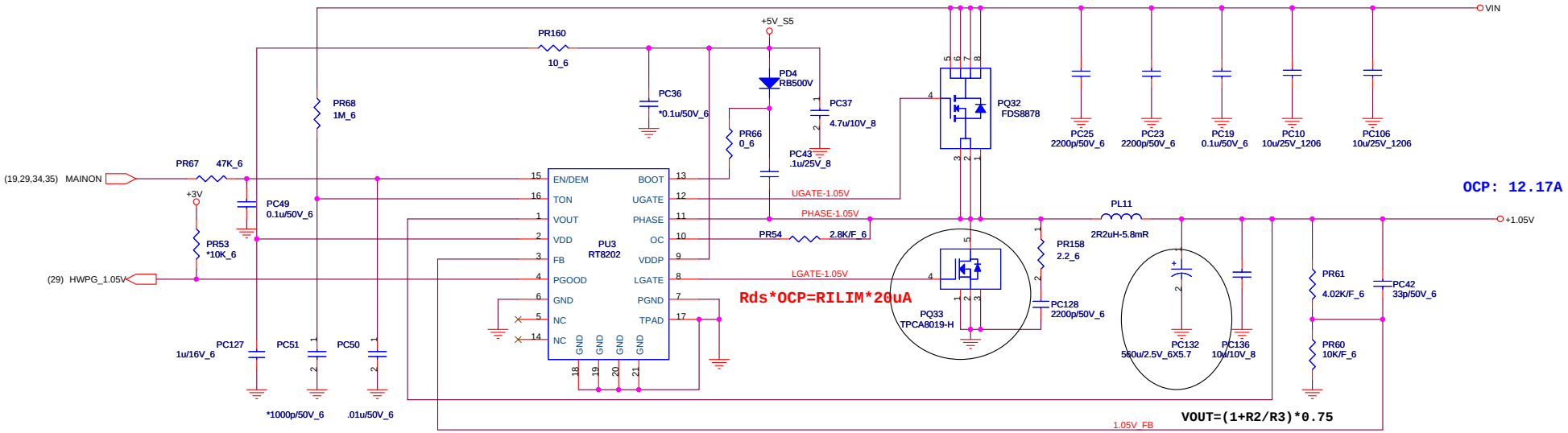


	UMA	Discrete
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	10K Ohm CS31003F949	2.43K Ohm CS22433F913
R3	10K Ohm CS31003F949	10K Ohm CS31003F949
PF1	10A DKA00VFU000	10A DKA00VFU000


MAIND
MAIND (34,35)
SUSD
SUSD (35)
(3) SYS_SHDN#
PR114 0_4
VIN
VL
3V5V_EN
PC92 100U/25V_6X7.7
PC74 0.1u/50V_6
PC75 2200p/50V_6
PC72 *10u/25V_1206
PC85 10u/25V_1206
PR109 39K/F_4
PR104 390K_4
PC77 0.1u/50V_6
PR106 150K_4
PC76 *.01u/16V_4
PC81 4.7u/10V_8
PR102 0_4
PC73 1u/10V_6
PR99 0_4
PC70 0.1u/50V_6
REF
PR98 *0_6
PC67 0.1u/50V_6
PC68 2200p/50V_4
PC65 10u/25V_1206
PQ10 FDS8878
3V_DH
OCP : 8A
+3VPCU
PL3 2R2uH-5.8mR
3V_LX
PR88 *2.2_6
PC63 *2200p/50V_6
PR92 0_6
PC64
PC66
PQ9 FDS6690AS
PR91 *0_6
0.1u/50V_6
330u/6.3V_6X5.7
OCP: 8A
+5VPCU
01/22 REV_3B Change value
PL4 2R2uH-5.8mR
5V_LX
5V_DH
PQ11 FDS8878
PR107 64.9K/F_4
PR112 10K/F_4
PR118 2.2_6
PC88 2200p/50V_6
5V_DL
PQ13 FDS6690AS
PC90
PC89
PC80
10u/25V_1206
0.1u/50V_6
330u/6.3V_6X5.7
PU5
ISL6237
LDOREFIN LDO VIN NC ONLOCC VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC PGND DL2 BST2
PR108 178K/F_6
DDPWRGD_R
PR90 196K/F_6
REFIN2
SKIP
PC84 0.1u/50V_6
PR111 1/F_6
PC69 0.1u/50V_6
PR97 1/F_6
3V_DL
ADD PR174 12/05
PR174 0_6
PR175 *0_6
NC PR175 12/05
PR100 0_6
PC82 0.1u/50V_6
PC78 1u/16V_6
PD8 1PS302
PC79 0.1u/50V_6
PC83 0.1u/50V_6
PD7 1PS302
PR101 22_8
+15V
+15V_ALWP
PR105 *200K_4
PC71 0.1u/50V_6
PR103 *39K_4
PR89 *0_6
SKIP
PR93 *0_6
REF
PR94 0_6
PR95 *10K_6
PR96 0_6
SYS_HWPG (29)
OCP:8A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=8-(4.18/2)=5.91A
Vth=5.91A*15mOhm=88.65mV
R(Ilim)=(88.65mV*10)/5uA
~177.3K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=100.05mV
R(Ilim)=(100.05mV*10)/5uA
~200.1K
PR124 1M_6
PR122 1M_6
S5D
(29) S5_ON
PR123 1M_6
PQ22 DTC144EU
PQ24 DMN601K-7
PQ14 DMN601K-7
+5V_S5
PQ12 FDC653N_NL
+5V
PQ6 FDS8884
+3V
PQ7 FDC653N_NL
+3V_S5
PQ20 DMN601K-7
+3VSUS
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa
Size
Document Number
SYSTEM 5V/3V (ISL6237)
Rev 1A
Date: Tuesday, January 22, 2008
Sheet 31 of 37



Quanta Computer Inc.			
PROJECT : BL5S Santa Rosa			
Size	Document Number		Rev
	CPU CORE(ISL6262A)		1A
Date: Tuesday, January 22, 2008		Sheet 32 of 37	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

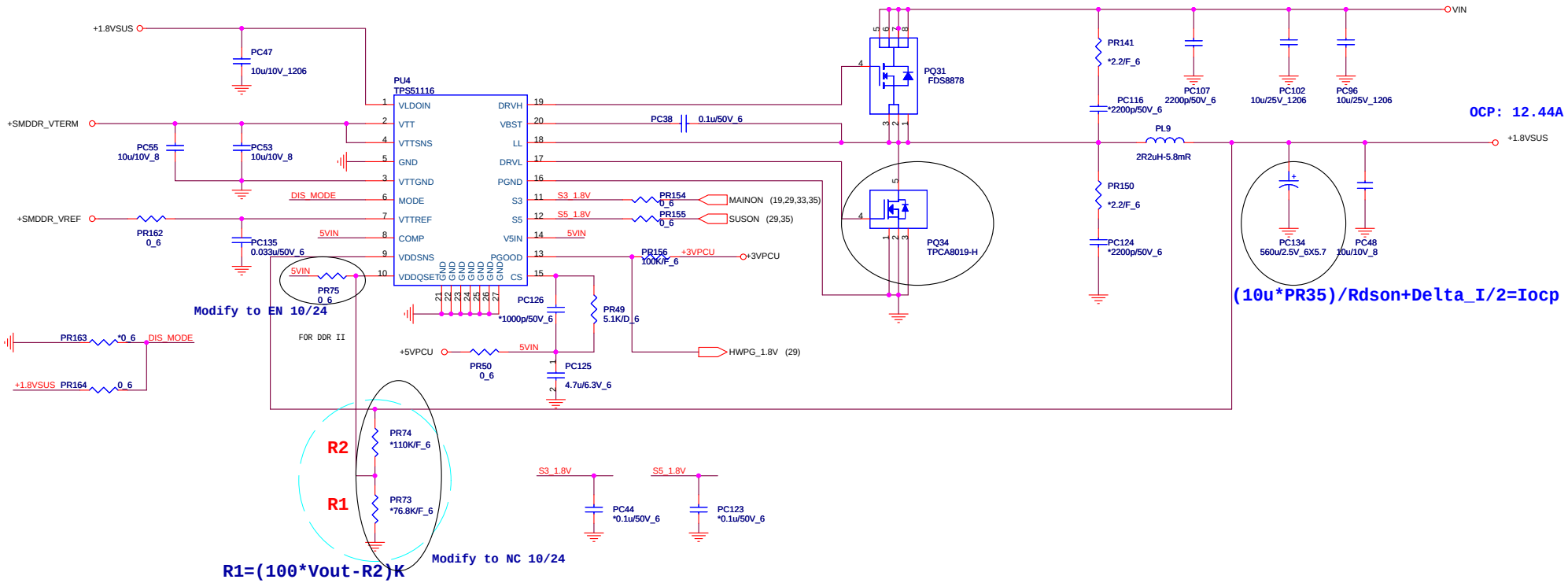
AOL1412 Rds=4.6mOhm
12.17A OCP --- OC=2.8K

SI7636 Rds=4.8mOhm
11.67A OCP --- OC=2.8K

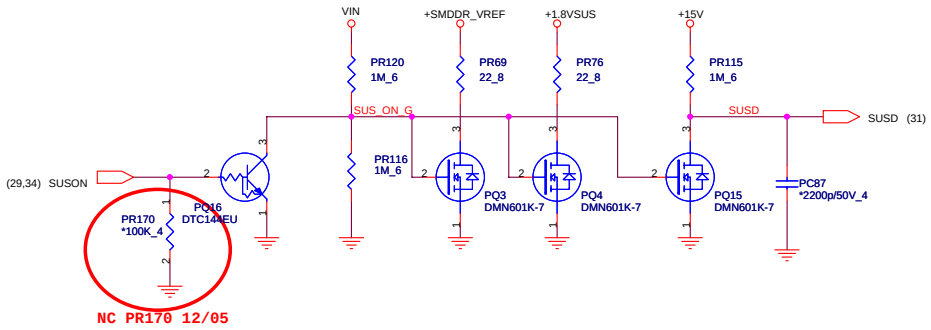
Quanta Computer Inc.
PROJECT : BL5S Santa Rosa

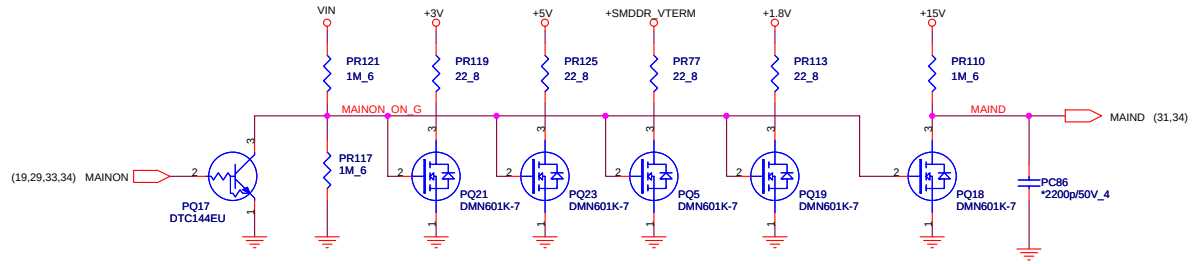
Size	Document Number	Rev
	VTT 1.05V (RT8202)	1A

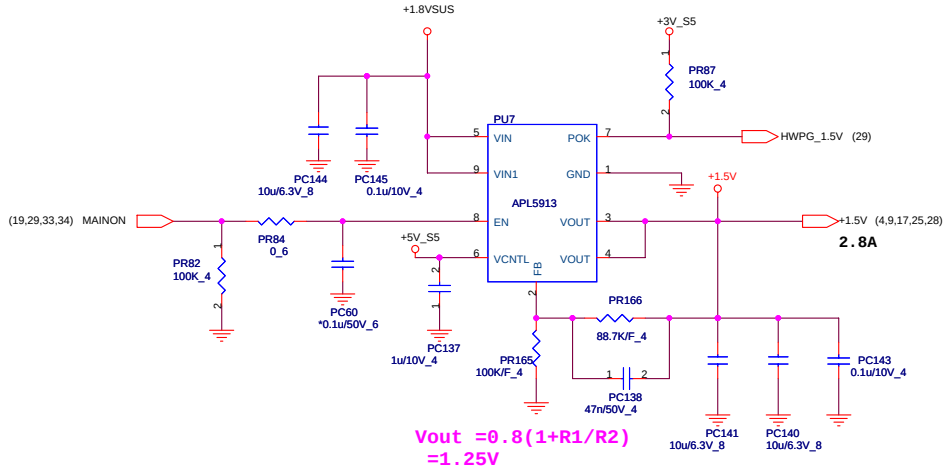
Date: Tuesday, January 22, 2008 Sheet 33 of 37

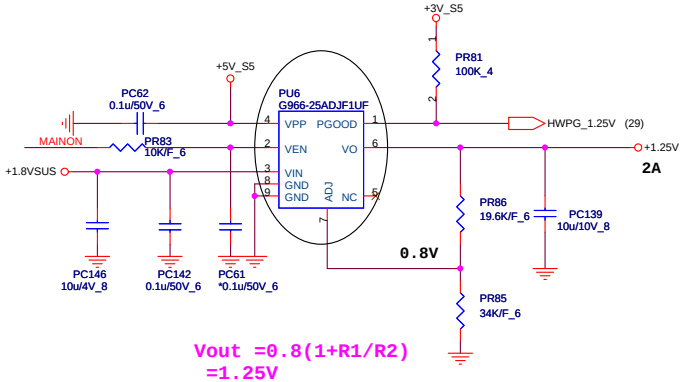


Quanta Computer Inc.		
PROJECT : BL5S Santa Rosa		
Size	Document Number: DDR 1.8V(TPS51116)	Rev: 1A
Date: Tuesday, January 22, 2008	Sheet 34 of 37	









Quanta Computer Inc.		
PROJECT : BL5S Santa Rosa		
Size	Document Number: Discharge (1.25V/1.5V)	Rev: 1A
Date: Tuesday, January 22, 2008	Sheet 35 of 37	

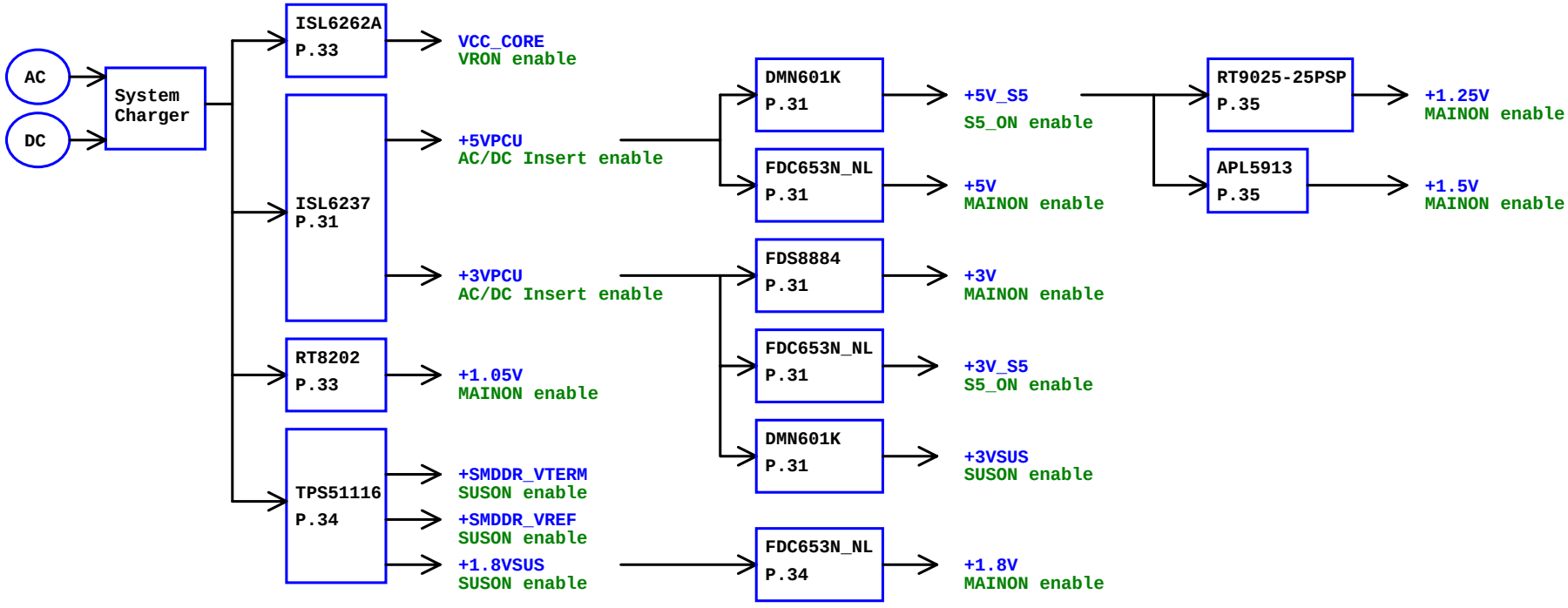
Model	REV	DATE	CHANGE LIST	NOTE
BL5S	00	20070824	FIRST RELEASED : 20070824	
	1A	20070914	FIRST RELEASED : E200709-2519	

Quanta Computer Inc.

PROJECT : BL5S Santa Rosa

Size	Document Number	Rev
	Change List	1A

Date: Tuesday, January 22, 2008 Sheet 36 of 37



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	HDMI, Cardreader (OZ129T)
+1.25V	CLK, GMCH, ICH8M