4.4.2 Pulse-Current Limiting

The internal architecture of the TL494 does not accommodate direct pulse-current limiting. The problem arises from two factors:

- The internal amplifiers do not function as a latch; they are intended for analog applications.
- The pulse-steering flip-flop sees any positive transition of the PWM comparator as a trigger and switches its outputs prematurely, i.e., prior to the completion of the oscillator period.

As a result, a pulsed control voltage occurring during a normal on-time not only causes the output transistors to turn off, but also switches the pulse-steering flip-flop. With the outputs off, the excessive current condition decays and the control voltage returns to the quiescent-error-signal level. When the pulse ends, the outputs again are enabled and the residual on-time pulse appears on the opposite output. The resulting waveforms are shown in Figure 26. The major problem here is the lack of dead-time control. A sufficiently narrow pulse may result in both outputs being on concurrently, depending on the delays of the external circuitry. A condition where insufficient dead time exists is a destructive condition. Therefore, pulse-current limiting is best implemented externally (see Figure 27).

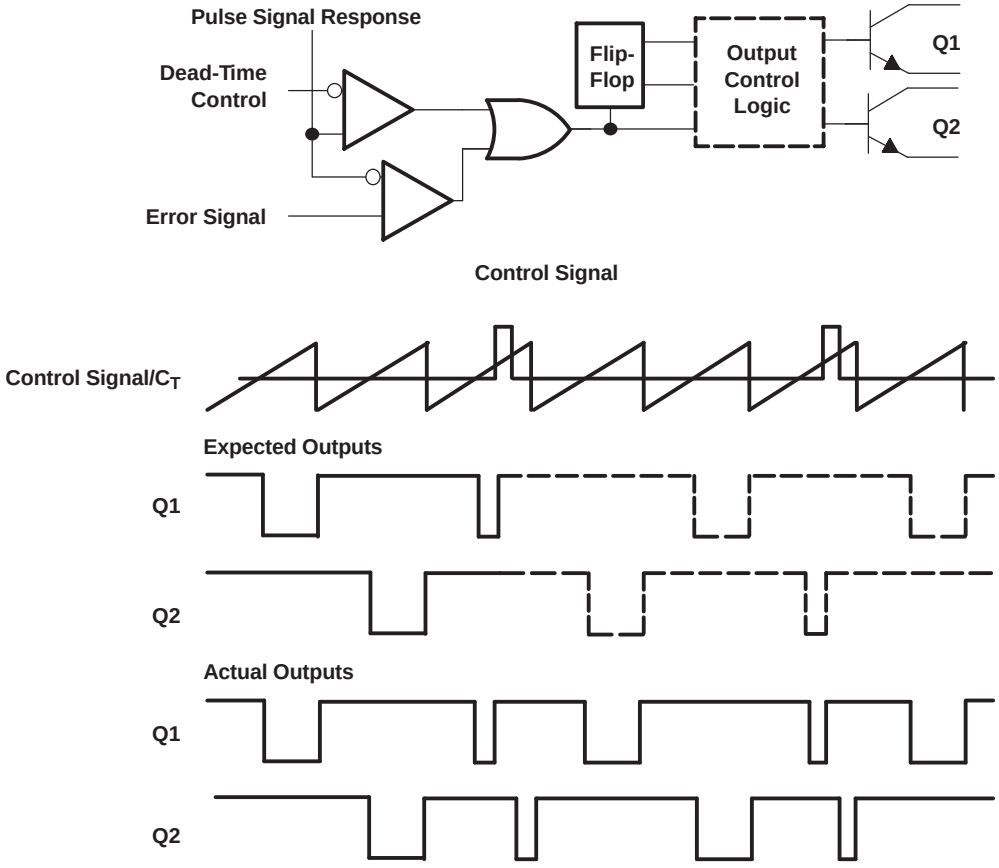

Figure 26. Error-Signal Considerations

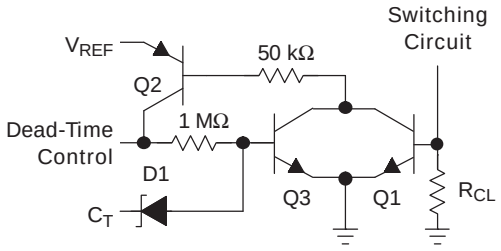

Figure 27. Peak-Current Protection

In Figure 27, the current in the switching transistors is sensed by R_{CL}. When there is sufficient current, the sensing transistor Q1 is forward biased, the base of Q2 is pulled low through Q1, and the dead-time control input is pulled to the 5-V reference. Drive for the base of Q3 is provided through the collector of Q2. Q3 acts as a latch to maintain Q2 in a saturated state when Q1 turns off, as the current decays through R_{CL}. The latch remains in this state, inhibiting the output transistors, until the oscillator completes its period and discharges C_T to 0 V. When this occurs, the Schottky diode (D1) forward biases and turns off Q3 and Q2, allowing the dead-time control to return to its programmed voltage.

4.5 Applications of the Dead-Time Control

The primary function of the dead-time control is to control the minimum off time of the output of the TL494. The dead-time control input provides control from 5% to 100% dead time (see Figure 28).

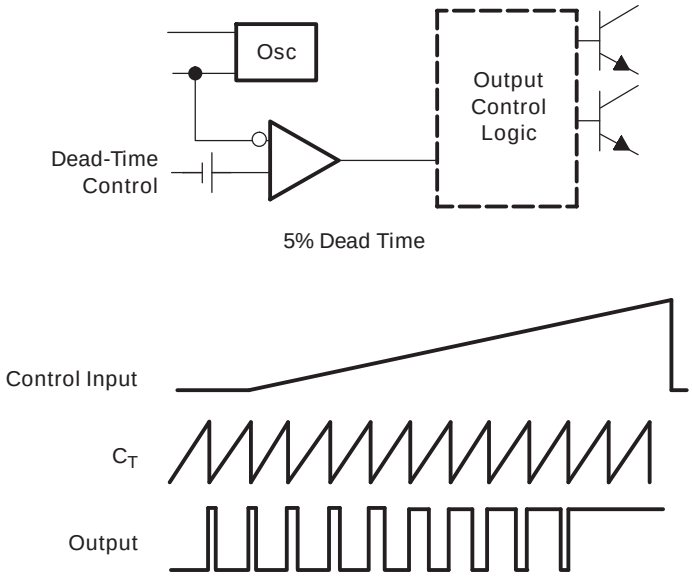

Figure 28. Dead-Time Control Characteristics

Therefore, the TL494 can be tailored to the specific power transistor switches that are used to ensure that the output transistors never experience a common on time. The bias circuit for the basic function is shown in Figure 29. The dead-time control can be used for many other control signals.

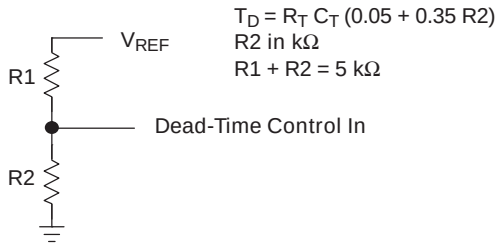

Figure 29. Tailored Dead Time