Timing Characteristics

The timing characteristics of TCS3490 are given below.

Figure 12:
AC Electrical Characteristics, V_{DD} = 3V, T_A = 25°C (unless otherwise noted)

Parameter(1)	Conditions	Min	Max	Unit
f_{SCL}	Clock frequency (I^2C only)	0	400	kHz
t_{BUF}	Bus free time between start and stop condition	1.3		µs
$t_{HD;STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6		µs
$t_{SU;STA}$	Repeated start condition setup time	0.6		µs
$t_{SU;STO}$	Stop condition setup time	0.6		µs
$t_{HD;DAT}$	Data hold time	60		ns
$t_{SU;DAT}$	Data setup time	100		ns
t_{LOW}	SCL clock low period	1.3		µs
t_{HIGH}	SCL clock high period	0.6		µs
t_F	Clock/data fall time		300	ns
t_R	Clock/data rise time		300	ns
C_i	Input pin capacitance		10	pF

Note(s) and/or Footnote(s):

1. Specified by design and characterization; not production tested.

Timing Diagram

Figure 13:
Parameter Measurement Information