

Termination techniques for high-speed buses

KARTHIK ETHIRAJAN AND JOHN NEMEC, PHD, CALIFORNIA MICRO DEVICES

As bus speeds continue to increase, system designers must seriously consider the issues of signal propagation and quality. Concerns previously relegated to the analog world, such as transmission-line effects, now determine whether a digital design will work at such high signal-transmission and edge rates. High-speed pc-board traces behave like transmission lines, and reflections occur at all points on the pc-board trace where impedance mismatches exist.

In a typical digital system, the output impedance of the driver is less than the characteristic impedance of the pc-board trace, which is in turn less than the input impedance of the receiver. Reflections translate into observable effects, such as ringing and stair-stepping. These distortions can produce or contribute to a number of problems: false triggering in clock lines; erroneous bits on data, address, and

Choosing the proper bus-termination technique—parallel, series, Thevenin, ac, or diode-based—is critical to digital-system performance. Improper termination can lead to ringing and stair-stepping, which in turn can cause false triggering and data errors.

control lines; an increase in clock and signal jitter; and an increase in total emissions from the pc board. An effective way to reduce the above transmission-line effects is to properly terminate these lines.

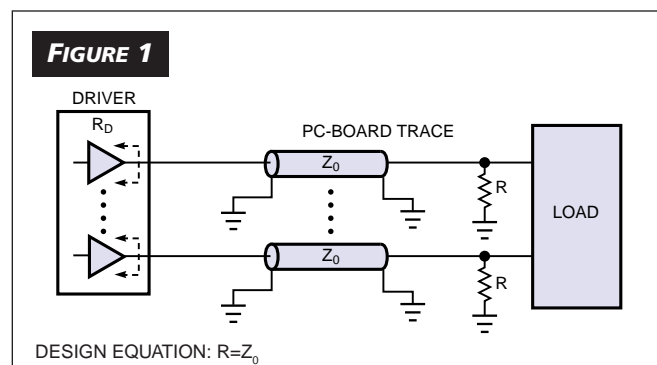
Common passive-termination techniques include parallel, Thevenin, series, and ac terminations. Schottky-diode termination, which

is an unconventional passive-termination technique, also provides some advantages. Familiarity with each technique's relative merits and demerits helps you choose the best technique or techniques for your board or system. Selection guides list recommended termination techniques for various common digital-system scenarios and for standards and specifications (Tables 1 and 2).

Parallel termination

Parallel termination is the simplest termination technique: A resistor, R , connects the open, or load, end of the transmission line to ground or V_{CC} (Figure 1). The value of R must match the characteristic impedance, Z_0 , of the line to eliminate reflections. If R matches Z_0 , the termination resistor absorbs the energy that causes the reflection, regardless of the value of the termination voltage (see box "Theory of terminations"). In digital logic, the sinking current is typically greater than the sourcing current. Terminating to V_{CC} helps the driver's sourcing capability, and terminating to ground helps its sinking capability. Hence, terminating to V_{CC} is better than terminating to ground, assuming a 50% duty cycle.

The advantages of parallel termination are that it offers simplicity of design and application and that it requires only one additional component, although you may ultimately use two resistors to terminate both ends of the line. The dis-



Parallel termination, which is the simplest type, comprises a single resistor connected from the end of the line to ground or V_{CC} .

TERMINATION TECHNIQUES

advantages of this technique are that dc power dissipates in the termination resistor, which is typically 50 to 150Ω, and that constant dc current from the driver at high or low logic levels adds to the dc load of the driver. Also, parallel termination degrades the high-output level of the signal. Terminating TTL outputs to ground lowers the V_{OH} level, which reduces the noise immunity at the receiver input.

Parallel termination also results in a lower signal slew rate with a capacitive load than does an unterminated line. The load capacitance and the resistance (parallel combination of termination resistance and Z_0) add to the RC time constant of the signal, which rises to the driver's output voltage. Note that the voltage at the end of an unterminated line doubles and hence produces a faster slew rate. The effect of different termination techniques on the slew rate of the signal at the end of the line is the outcome of complex interactions between the transmission line and the RC delay involved.

When you use parallel termination, you should be aware that a line impedance of less than 100Ω terminated with this scheme requires a dc output of 24 mA for TTL levels ($V_{OH(MIN)}=2.4V$). For this reason, parallel termination is not recommended for a battery-driven system. Also, note that the termination resistor dissipates as much as 0.25W (50 mA through a 100Ω resistor) of power, which a CMOS system that consumes only a few milliwatts of power can't accommodate. Also, remember that the power dissipation depends on the duty cycle: Connecting the resistor to ground results in the lowest power dissipation for low duty cycles, and terminating to V_{CC} results in the lowest power dissipation for high duty cycles (**Reference 1**). In addition, a strong pull-down resistor might cause the falling edge to be faster than the rising edge, resulting in the distortion of the duty cycle of the signal (**Reference 2**).

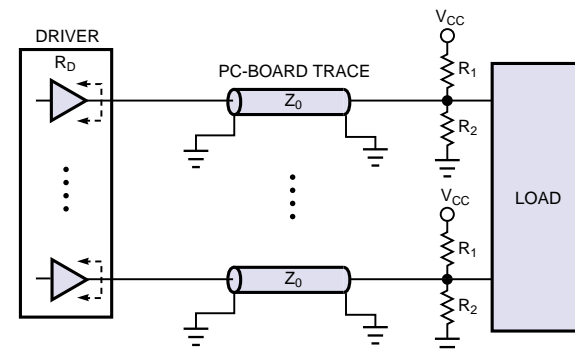
Thevenin termination

Thevenin, or dual, termination uses two resistors, R_1 and R_2 (**Figure 2**), whose parallel combination matches the Z_0 of the line. The Thevenin voltage, $V_{TH}=V_{R2}$, must be such that the driver's I_{OH} and I_{OL} currents are within the driver's specifications (see **box** "Design rules for Thevenin termination"). R_1 helps the driver to easily pull up to a logic-high state by sourcing some current to the load. Similarly, R_2 helps the driver to pull down to a logic-low state by sinking some current to ground. Properly chosen values for R_1 and R_2 enhance the driver's fan-out and smooth the power-dissipation variations because of the change in duty cycles.

The advantages of Thevenin termination are that, in this scheme, the termination resistors also serve as pullup and pulldown resistors and thereby improve the noise margin of the system. Thevenin termination also reduces the burden on the driver by supplying additional current to the load. This additional current helps the driver especially in a large voltage-swing system, such as 5 and 3.3V CMOS- or Bi-CMOS-based systems. Also, this type of termination provides good overshoot suppression.

One disadvantage of Thevenin termination is that a constant flow of dc from V_{CC} to ground, regardless of the logic state, results in static power dissipation in the termination

FIGURE 2



DESIGN EQUATIONS:

(FROM THE BOX "DESIGN RULES FOR THEVENIN TERMINATION")

$$V_{TH}=V_{OH(MIN)}-I_{OH(MAX)}(R_D+Z_0);$$

$$R_1=\frac{Z_0 V_{CC}}{V_{TH}}; \text{ AND}$$

$$R_2=\frac{Z_0 V_{CC}}{V_{CC}-V_{TH}},$$

WHERE $I_{OH(MAX)}$ =MAXIMUM OUTPUT CURRENT FROM THE DRIVER WHEN ITS OUTPUT VOLTAGE IS MINIMUM FOR HIGH-LEVEL LOGIC, $V_{OH(MIN)}$; R_D =THE OUTPUT IMPEDANCE OF THE DRIVER; AND V_{CC} =THE SUPPLY VOLTAGE.

Thevenin, or dual, termination requires two resistors, R_1 and R_2 , whose parallel combination matches the Z_0 of the line.

resistors. This method also requires ratio resistors and additional power and ground connections. Also, a line voltage, which equals the Thevenin voltage on a tristated bus, close to the switching threshold voltage causes greater levels of power dissipation within CMOS logic devices. At a voltage close to the threshold, both NMOS and PMOS transistors are conducting, which results in a current path between V_{CC} and ground. Thevenin termination also results in a lower signal slew rate with a capacitive load than does an unterminated line. The load capacitance and the resistance (parallel combination of Z_0 , R_1 , and R_2) add to the RC time constant of the signal, which rises to the driver's output voltage.

Note that CMOS devices switch at 50% threshold. Hence, when using Thevenin termination for CMOS devices, equal values for R_1 and R_2 result in a line voltage of one-half the V_{CC} . This situation occurs when a logic device does not drive the line. The result is greater levels of power dissipation within the receiver. The sum of this dissipation and the power dissipation in the termination resistors may be unacceptably high for CMOS logic devices (**Reference 1**).

The best applications for Thevenin termination are TTL circuits, especially advanced Schottky families, such as FAST (**Reference 3**). You can also use Thevenin termination to provide proper ECL termination from the -5.2V supply and for TTL from a 5V supply.

Series termination

Series termination, or back-matching, is a source-end termination unlike other types. A series termination comprises

THEORY OF TERMINATIONS

Lemma: No reflection will exist on a transmission line provided that the termination resistor, connected at the end of the line to *any* arbitrary termination voltage, matches the characteristic impedance of the line, Z_0 (**Figure A**). **Figures B** and **C** show the Thevenin and Norton equivalent circuits of **Figure A**'s parallel termination, respectively, where V_i , I_i =incident voltage, current; V_r , I_r =reflected voltage, current; V_T =termination voltage; R_T =termination resistor; and I_T =current through R_T .

Proof: From the Thevenin equivalent circuit,

From the Norton equivalent circuit,

and

$$V_i + V_r = V_T + I_i R_T. \quad (\text{A})$$

Adding **Equations A** and **D** produces

and

Subtracting **Equation D** from **Equation A** produces

Substituting **Equation C** into **Equation H** produces **(B)**

and

From **Equation J**, the magnitude of the reflected voltage is

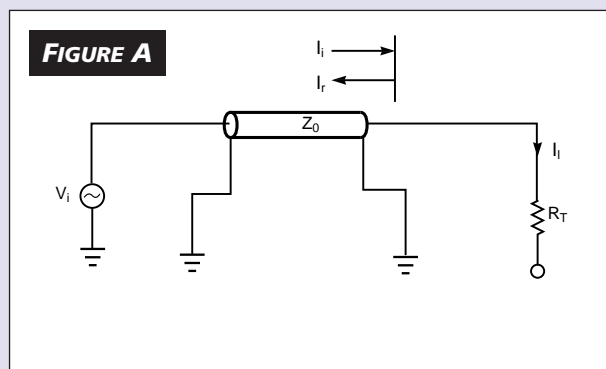
independent of the termination voltage. In addition, if $R_T = Z_0$ (perfectly matched), then $V_r = 0$; hence, the proof. **(C)**

$$V_i - V_r = \frac{Z_0}{R_T} \cdot V_T + I_i Z_0.$$

$$2V_i = \left(1 + \frac{Z_0}{R_T}\right) \cdot V_T + (R_T + Z_0) \cdot I_i,$$

$$I_i = \frac{2V_i - \left(1 + Z_0/R_T\right) \cdot V_T}{R_T + Z_0},$$

$$I_i = \frac{2V_i}{R_T - Z_0} - \frac{V_T}{R_T}.$$



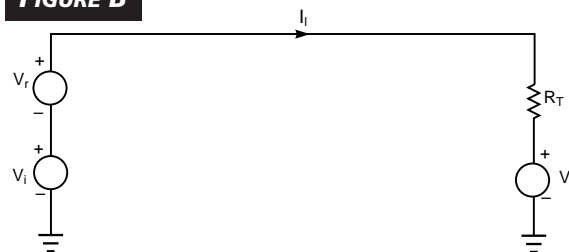
In parallel termination, no reflections occur if $R_T = Z_0$, regardless of the value of V_T .

$$2V_r = \left(1 - \frac{Z_0}{R_T}\right) \cdot V_T + (R_T - Z_0) \cdot I_i. \quad (\text{H})$$

$$2V_r = \left(1 - \frac{Z_0}{R_T}\right) \cdot V_T + (R_T - Z_0) \cdot \left(\frac{2V_i}{R_T + Z_0} - \frac{V_T}{R_T}\right), \quad (\text{I})$$

$$V_r = \left(\frac{R_T - Z_0}{R_T + Z_0}\right) \cdot V_i. \quad (\text{J})$$

FIGURE B

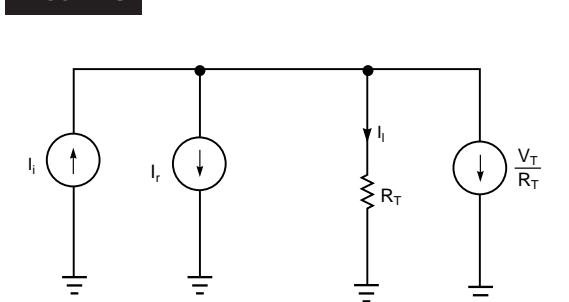


(D)

(E)

(F) The Thevenin model for parallel termination includes V_i , V_r , and V_T , the incident, reflected, and termination voltages, respectively.

FIGURE C



(G)

The Norton model for parallel termination includes I_i , I_r , and I_T , the incident, reflected, and R_T currents, respectively.

TERMINATION TECHNIQUES

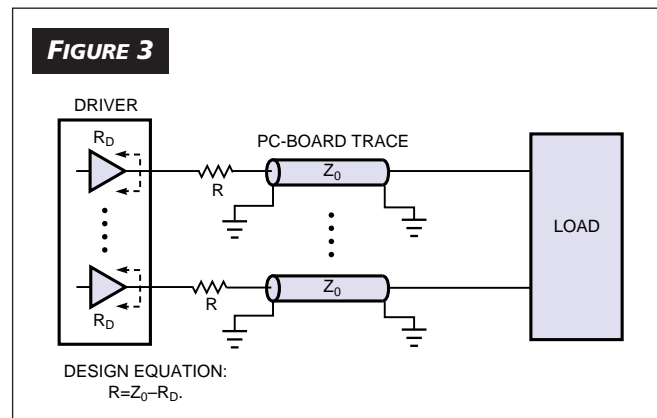
a resistor between the driver's output and the line (**Figure 3**). The sum of the output impedance of the driver, R_D , and the resistor value, R , must equal Z_0 . With this type of termination, only one-half the signal value appears on the line because of the voltage division between the line and the combination of the series resistor and the driver's impedance.

At the receiving end, however, the mismatch between the line impedance and the receiver's typically high input impedance causes a reflection of approximately the same voltage magnitude as the incident signal. The receiving device immediately sees the full voltage (the sum of the incident and reflected voltages), and the added signal propagates to the driving end. However, no further reflections occur because the series resistor terminates the reflected wave at the driving end.

The advantages of series termination are that it adds only one resistor per driver for the system and that its termination resistor consumes less power than all the other resistive types of termination. Series termination also adds no dc load to the driver and offers no extra impedance from signal line to ground.

The disadvantages of series termination are that using this method makes it difficult to tune the value of the series resistance so that the received-signal amplitude (after the first reflection) falls within the switching threshold and noise budget. Also, most drivers are nonlinear; that is, the output impedance varies with the logic state of the device, further complicating tuning. Hence, it is difficult to select a crisp value for the series resistance by applying the simple design equation.

Another disadvantage of series termination is that the driving end of the transmission line does not see the full reinforced signal amplitude for as long as twice the propagation delay of the line. The diminished signal amplitude during this time reduces some of the receiver's noise immunity in a multidrop situation. Also, with series termination, the data setup time for digital signals of the receiver (part of its timing budget) must accommodate this propagation delay. Series termination also results in a lower signal slew



A series termination comprises a resistor, R , which connects the driver's output, and the line; the sum of the output impedance of the driver, R_D , and R must equal Z_0 .

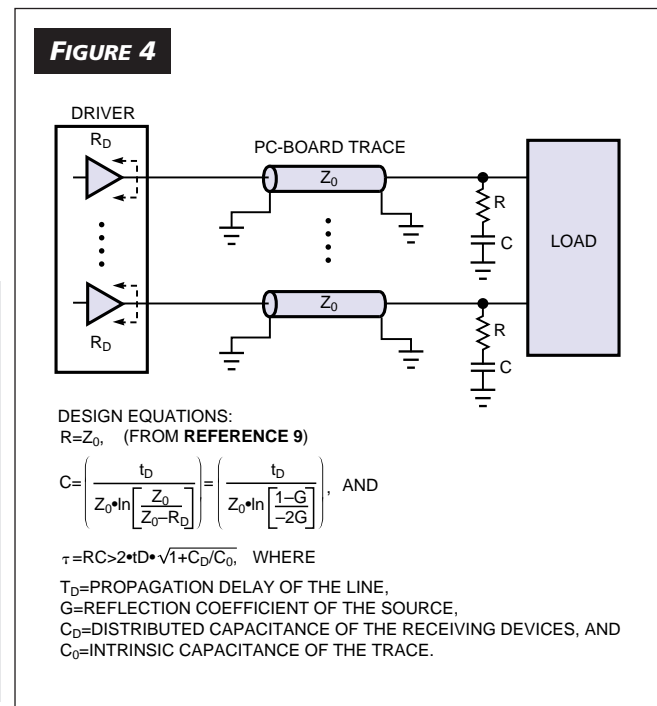
rate with a capacitive load than does parallel termination. The load capacitance and the Z_0 of the line add to the RC time constant of the signal, which rises to one-half the driver's output voltage.

The applications for series termination include CMOS-to-CMOS connections because series termination adds no impedance from signal line to ground (**Reference 1**). This termination also works well for advanced CMOS logic families, such as FACT and ECL. With FACT devices, the series-termination resistor adds to the output impedance of the driver. Thus, the driver dissipates less power than it does without the termination (**Reference 3**). Series termination also works well for systems with loads lumped at the end of the cable as opposed to a multidrop situation. In a multidrop situation, receivers on the line see the full amplitude of the signal at different times.

You can eliminate the disadvantages of higher propagation delay and usage with lumped loads only by using more transmission lines (**Reference 4**). If the driver has high fan-out, then you can connect many transmission lines— N , for example—to the driver's output. Each line then needs its own series termination according to the design equation. The net impedance at the output of the driver is $(R + Z_0)/N$. This net impedance must be much larger than the internal impedance of the driver for the driver itself to function.

AC termination

AC, or RC, termination comprises a resistor, R , and a capacitor, C , that connect to the load end of the transmission line (**Figure 4**). The value of R must match the Z_0 of the



In ac termination, a resistor, R , and capacitor, C , connect to the load end of the transmission line.

DESIGN RULES FOR THEVENIN TERMINATION

In Thevenin termination, the parallel combination of Thevenin resistors R_1 and R_2 matches the characteristic impedance, Z_0 , of the transmission line (**Figure A**). The values for R_1 and R_2 are based on the asymmetric characteristic of the driver dur-

$$Z_0 = \frac{R_1 R_2}{R_1 + R_2}.$$

ing high and low levels of the logic, given that,

$$\frac{V_{TH}}{V_{CC}} = \frac{R_2}{R_1 + R_2}.$$

$$\frac{V_{TH}}{V_{CC}} = \frac{Z_0}{R_1},$$

Applying voltage division between R_1 and R_2 from the above

$$R_1 = \frac{Z_0 \cdot V_{CC}}{V_{TH}}.$$

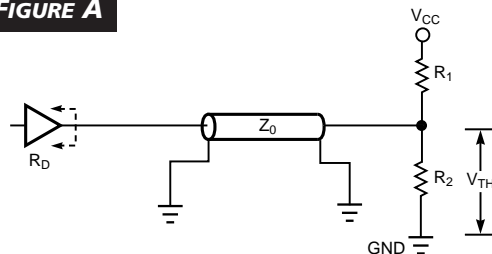
circuit results in

$$R_2 = \frac{Z_0 \cdot R_1}{R_1 - Z_0}.$$

Then, from **Equations A** and **B**,

$$R_2 = Z_0 \cdot \frac{Z_0 \cdot V_{CC} / V_{TH}}{Z_0 \cdot V_{CC} / V_{TH} - Z_0},$$

FIGURE A



For proper Thevenin termination, the parallel combination of R_1 and R_2 must match Z_0 .

$$R_2 = Z_0 \cdot \frac{V_{CC}}{V_{CC} - V_{TH}}. \quad (\text{G})$$

and

From **Equation A**,

Substituting **Equation D** into **Equation E** produces and

Equations D and **G** give the values of R_1 and R_2 , respectively. The Thevenin voltage, V_{TH} , is an unknown in these equations, and you can calculate V_{TH} from the driver specifications.

To determine the Thevenin voltage, you can draw a Thevenin-equivalent circuit (**Figure B**) to the circuit in **Figure A**, where $I_{OH(MAX)}$ is also the sourcing current. Now,

$$V_{TH} = V_{OH(MIN)} - I_{OH(MAX)}(R_D + Z_0). \quad (\text{H})$$

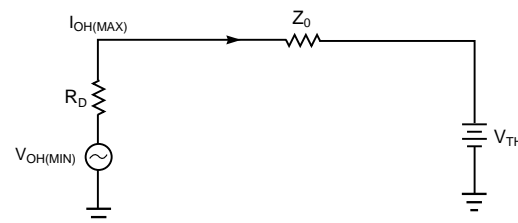
and

You can obtain $V_{OH(MIN)}$ and $I_{OH(MAX)}$ from the driver's data sheet. By careful observation, you can infer that during logic-high state, the Thevenin resistor, R_1 , performs pullup action by supplying current to the load. This current added with the driver's sourcing current is just enough to maintain the voltage at the output of the driver at the minimum threshold-logic voltage, $V_{OH(MIN)}$. Designing V_{TH} in this way minimizes power dissipation in R_1 and R_2 .

During a logic-low state, R_2 sinks any excess current (any current greater than $I_{SINK(MAX)}$ or $I_{OL(MAX)}$) from the load to the ground. Because sourcing is a bigger problem than sinking, you design V_{TH} based on a logic-high state. Hence, R_2 may not be an optimum value for sinking or pulldown action. Nevertheless, using **Equation G** to calculate R_2 helps the driver to sink current during a logic-low state.

For digital devices, design V_{TH} to be at either logic-high or -low state. Now, if a driver's output is tristated, the line is pulled either to a high or low state (depending on V_{TH}) rather

FIGURE B



The Thevenin model for single-ended parallel termination shows sourcing-current $I_{OH(MAX)}$.

TERMINATION TECHNIQUES

line to eliminate reflection. Choosing the capacitor value is intricate, because a small value results in a smaller RC time constant, and the resulting RC circuit acts as an edge generator, causing overshoot and undershoot. On the other hand, a large capacitor value increases power consumption. As a rule, the RC time constant must be greater than twice the loaded propagation delay of the line (**Figure 4** and **Reference 5**). Power dissipation in the termination components is a function of the frequency, duty cycle, and bit pattern of the previous data. These factors affect the charging and discharging of the termination capacitor and hence affect power dissipation.

The advantages of ac termination are that the termination capacitor blocks dc and hence saves considerable power and that an appropriate choice of the capacitor value results in the waveform at the load end that's nearly an ideal square wave with minimal overshoot or undershoot.

One disadvantage of ac termination is that the data on the

line may exhibit time jitter, depending on the previous data pattern. For example, a long string of like bits causes the line and capacitor to charge to the maximum level of the driver's output voltage. Then, a subsequent data bit of the opposite polarity takes longer than normal to cross the receiver threshold because the voltage at the receiver starts from a greater potential. The timing budget must include this increased time to guarantee system operation (**Reference 3**).

When using ac termination, note that the standard RS-422 interface protocol does not recommend ac termination, because the drivers' typical 100 Ω source impedance can introduce output jitter. Also, current-mode drivers do not use ac termination (**Reference 3**).

Schottky-diode termination

Schottky-diode, or diode, termination comprises two Schottky diodes and their connections (**Figure 5**). Any reflection at the end of the transmission line, which causes

TABLE 1—SELECTION GUIDE FOR TERMINATION TECHNIQUES (SCENARIO BASED)

Scenario	Recommended termination	Reason
MECL drivers driving three or more lines in the backplane	Series (100 Ω), parallel 600 Ω to $-2V$ parallel	Pulldown resistor compensates for the drive current; series termination addresses parallel fan-out (Reference 4)
Circuits containing a mixture of bipolar and advanced CMOS devices that are strong drivers	Parallel	Reduces overall system power consumption of terminated to ground for low duty cycle and to V_{CC} for high duty cycle (Reference 1)
Circuits containing a mixture of bipolar and advanced CMOS devices that are weak drivers	Thevenin	Provides drive support; Thevenin resistors provide current, which helps the driver that connects to a long line
CMOS-to-CMOS connections	Series	Adds no extra impedance from signal line to ground (Reference 1)
FACT (advanced CMOS) devices for low-power applications	Series	Adds to the output impedance of the driver; hence, the driver dissipates less power (Reference 1)
FAST (advanced Schottky-TTL) devices	Thevenin (330 Ω pair)	FAST devices have limited current-drive capability (Reference 3)
Switching-I/O cache-memory or SDRAM arrays that connect to the backplane	Schottky diode, 10 to 50 Ω series	Memory plug-ins can be perceived as adding distributed capacitance on the line, which effectively lowers Z_0 ; Schottky-diode termination requires no impedance matching (Reference 12).
Extensible bus applications, such as switching-I/O cache-memory or SDRAM arrays that connect to the backplane	Series	Tuning the value of the series resistance limits overshoot and undershoot to predetermined values—typically, 35 and 12%, respectively (Reference 18)
Driving a backplane with tristatable devices	Schottky diode	Schottky-diode termination can handle large impedance variations (Reference 4)
Battery-driven systems	Series, ac, Schottky diode	Low dc power consumption compared with parallel or Thevenin termination; enhances battery life (Reference 1)
Drivers with limited current capability driving heavily loaded data lines	Thevenin	Sourcing and sinking capabilities of Thevenin termination help the driver to sustain a crisp logic state at every receiver end
Current-source drivers with high output resistance compared with the Z_0 of the line	Parallel	Creates matched source (Reference 16)

TERMINATION TECHNIQUES

the voltage at the input of the receiver to rise above V_{CC} plus the forward-bias voltage of the diode, forward-biases the diode that connects to V_{CC} . The diode turns on and clamps the overshoot to V_{CC} plus the threshold voltage.

Similarly, the diode that connects to ground limits undershoot to its forward-bias voltage. However, the diodes absorb no energy and merely divert it to either the power or ground plane. As a result, multiple reflections occur on the line. The reflections gradually subside, principally because of the loss of energy via the diodes to V_{CC} or ground and the resistive losses of the line. These losses limit the amplitude of the reflections to maintain signal integrity.

Three characteristics of a diode have a profound effect on its performance as a termination device. Higher turn-on time, t_{ON} , results in undershoot. Higher forward-bias voltage, V_F , causes time jitter. Higher reverse-recovery time, t_{rr} , increases the rise time, t_r , of the signal. Thus, you can preserve signal integrity by using a diode that has a small t_{ON} , V_F , and t_{rr} as a termination device. A Schottky diode possesses these characteristics.

One advantage of diode termination is that, unlike a classic termination scheme, Schottky-diode termination requires no matching. Hence, you can use this technique to

terminate a line of unknown Z_0 . If the load that connects to the transmission line is capacitive, then it effectively reduces Z_0 . Variations in Z_0 do not affect the termination. Also, the power dissipated in the dynamic on-resistance of the Schottky diode is much smaller than the power dissipation of any resistive-termination technique. In fact, the reflection power partially feeds back to the source through the forward-biased diodes. Also, you can place Schottky diodes at any point along the line where reflections may originate.

The one disadvantage of diode termination is that the existence of multiple reflections can affect subsequent signal launches. Hence, you need to verify diode response at the switching frequency. To reap the benefits of this termination scheme, you must choose a Schottky diode that has small t_{ON} , V_F , and t_{rr} .

Schottky-diode termination works well in a multidrop situation in which some of the receivers on the line can also drive the line. Hence, application of transmission-line theory to arrive at a conventional termination in such situations becomes highly complicated. Simulations prove that terminating at multiple points—preferably at points of discontinuity, or stubs—yields a uniformly improved signal integrity over the length of the bus.

TABLE 2—SELECTION GUIDE FOR TERMINATION TECHNIQUES (SPECIFICATION BASED)

Standard specification	Recommended termination	Comments
Gunning transceiver logic (GTL)	Parallel (50 to V_{TT} =1.2V)	GTL (JEDEC) bus uses pullup termination on both ends of the bus, which terminates signals arriving from sources anywhere along the length of the bus (Reference 8)
GTL+ for boards with Pentium Pro processor	Parallel (45 to 65 to V_{TT} =1.2V)	Similar to GTL (Reference 14)
Backplane transceiver logic (BTL)	Parallel (33 to V_{TT} =2.1V)	BTL (IEEE) and GTL are both low-voltage, high-speed interface standards (Reference 8)
Futurebus+ backplane	Parallel (39 to V_T =2.1V)	See Reference 19
High-speed transceiver logic	Parallel (50 to V_{TT}), series (25)	Termination depends on the load type as suggested in the specifications (Reference 9)
Stub-series-terminated logic	Parallel (50 to V_{TT}), series, (25 to 50)	Represents a multidrop situation in which stubs are series-terminated and the ends of the bus are parallel-terminated
Low-voltage differential signaling for use in, for example, portable-computer applications	Parallel (100 between D+ and D-)	Requirement for functionality (Reference 10)
USB for use in, for example, desktop-computer applications	Series (27)	Adds to the driver output impedance, which is 3 to 15 (Reference 17)
Single-ended SCSI-I	Thevenin (R_1 =220 ; R_2 =330)	Common practice (Reference 15)
Differential SCSI-1	Parallel (330 to V_T , 150 between D+ and D-, 330 to ground)	Common practice if many devices are not connected (Reference 7)
IEEE 1284-compliant parallel ports in computers that connect to peripherals, such as printers	Series	IEEE 1284-compliant high-speed drivers have high output impedance of 45 to 55 (Reference 11)
IEEE-488 bus	Thevenin	Interconnects TTL-level signals through ribbon cables as long as 20m (Reference 6)

Note: V_{TT} and V_T both stand for the termination voltage.

TERMINATION TECHNIQUES

One general point applies to all of these termination schemes: The effective Z_0 of a transmission line decreases because of layout procedures and loading in a multidrop situation (**Reference 5**). The actual loaded characteristic impedance, Z_0' , is now as follows:

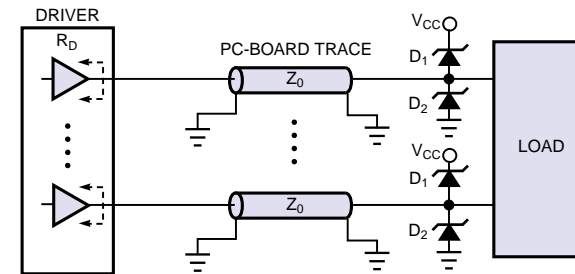
$$Z_0' = \frac{Z_0}{\sqrt{1 + C_D / C_0}},$$

where C_0 is the intrinsic capacitance of the trace, and C_D is the distributed capacitance of the receiving devices (the total load capacitance divided by the trace length). Typically, sockets add 2 pF to C_D , and vias add 0.3 to 0.8 pF to C_D . Hence, a distributed capacitive load on a line reduces the characteristic impedance. This correction factor for Z_0 applies to all termination schemes, depending on the overall system architecture.

References

1. Pace, C, "Terminate bus lines to avoid overshoot and ringing," *EDN*, Sept 17, 1987, pg 227.
2. "Advanced High-Speed CMOS (AHC) Logic Family," Texas Instruments, Document SCAA034A, June 1997.
3. Royle, D, "Correct signal faults by implementing line-analysis theory," *EDN*, June 23, 1988, pg 143.

FIGURE 5



Schottky-diode termination, for which two diodes connect to the end of the line, requires no matching and thus is useful for terminating lines of unknown Z_0 .

4. Blood, William R, "MECL system design handbook," Motorola Inc.
5. "Transmission line effects in PCB applications," Motorola Semiconductor Application Note, Document AN1051/D, 1990.
6. ANSI/IEEE Standard 488, IEEE Inc, New York, NY, 1978.

7. Goldie, J, "An introduction to the differential SCSI interface," National Semiconductor Corp, AN-904, August 1993.
8. "GTL/BTL: A low swing solution for high speed digital logic," Texas Instruments, SCEA003A, March 1997.
9. HSTL, EIA/JESD8-6 Standard, EIA, August 1995.
10. Huq, S, "An overview of LVDS technology," National Semiconductor, AN-971.
11. IEEE Standard 1284, ANSI, December 1994.
12. "Introduction to termination for high-speed bus applications," California Micro Devices Data Book, pg 9-1, Document AP-201, August 1996.
13. Nemec, J, "The dynamics of AC termination," California Micro Devices Data Book, pg 1, Document ST-103, November 1996.
14. "Pentium Pro processor GTL+ guidelines," Intel, AP-524, March 1996.
15. "SCSI Termination," Apple Inc, Technote DV 15, August 1990.
16. True, K, "Reflections: Computations and waveforms," National Semiconductor Corp, AN-807, 1996.
17. USB Specification, Revision 1.0, January 1996.
18. Vu, M, "Choose termination and topology to maximize signal integrity and timing," *EDN*, Oct 24, 1996, pg 95.
19. "What is Futurebus+?," National Semiconductor Corp, AN-1036, January 1996, pg 95.
20. Yamada, M, and Y Konishi, "Trend of high speed I/O interface," Mitsubishi Electric Co, ULSI Laboratory, Technical Report of IEICE, ICD95-31(1995-05).

Authors' biographies



Karthik Ethirajan is an application engineer at California Micro Devices (Milpitas, CA), where he has worked for one year. In his current position, Ethirajan interacts with customers and engineers to design new products and develop application notes. He has an MSEE from Western Michigan University (Kalamazoo, MI) and a BSEE from Anna University (India). In his spare time, Ethirajan enjoys swimming and jogging.



John Nemec is director of applications at California Micro Devices (Milpitas, CA), where he has worked for three years. While at the company, he has helped to develop terminations, filters, charge pumps, and drivers. Nemec has a PhD from the University of Houston and an MSEE and a BSEE from the University of Arizona (Tucson, AZ). In his spare time, Nemec enjoys swimming and travel.

VOTE

Please use the Information Retrieval Service card to rate this article (circle one):

High Interest
578

Medium Interest
579

Low Interest
580