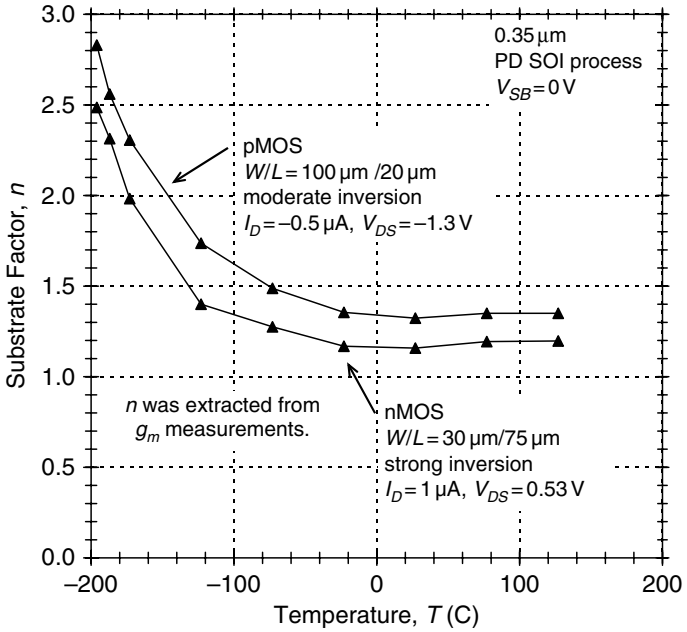

Figure 3.4 Measured substrate factor, n, from −196 to 127 °C (77 to 400 K) for nMOS and pMOS devices in a 0.35 µm PD SOI CMOS process. n is nearly independent of temperature except at very cold temperatures below −73 °C (200 K). n almost doubles at −196 °C (77 K), most likely due to increasing interface capacitance. Reproduced by permission of the Institute of Electrical and Electronic Engineers © 2004, from [20]

Table 3.9 MOS substrate factor, thermal voltage, low-field mobility, and low-field transconductance factor with resulting technology current over the −55 to 125°C military temperature range for nMOS devices in a 0.18 µm CMOS process

T (°C)	T (K)	n (n_0) (in MI)	U_T (mV)	μ_0 ($cm^2/V \cdot s$)	$k_0 = \mu_0 C'_{OX}$ ($\mu A/V^2$)	$I_0 = 2n_0 k_0 U_T^2$ (µA)
−55	218	1.272	18.784	681.3	572.9	0.514
−20	253	1.276	21.800	544.9	458.3	0.556
0	273	1.279	23.524	486.1	408.8	0.578
27	300	1.282	25.850	422.0	354.9	0.608
50	323	1.286	27.832	377.7	317.7	0.633
70	343	1.289	29.555	345.2	290.3	0.654
100	373	1.294	32.140	304.4	256.0	0.684
125	398	1.298	34.294	276.2	232.3	0.709

Values are calculated for μ_0 $(T = 300\,K) = 422\,cm^2/V \cdot s$, $C'_{OX} = 8.41\,fF/\mu m^2$, and a mobility temperature exponent of −1.5 to model nMOS devices in a 0.18 µm CMOS process. The substrate factor is from Table 3.8.

in Table 3.6 using the temperature-corrected thermal voltage, mobility, and transconductance factor expressions from Table 3.7. A room temperature ($T = 300\,K$), low-field mobility of $\mu_0 = 422\,cm^2/V \cdot s$, gate-oxide capacitance of $C'_{OX} = 8.41\,fF/\mu m^2$, and mobility temperature exponent of $BEX = -1.5$ are used to again model nMOS devices in a 0.18 µm CMOS process. Mobility and gate-oxide capacitance process parameters are from Table 3.2, and temperature process parameters are from Table 3.5.

Table 3.9 shows a large decrease in mobility and the transconductance factor as temperature increases. Mobility, μ_0, and correspondingly the transconductance factor, $k_0 = \mu_0 C'_{OX}$, are proportional

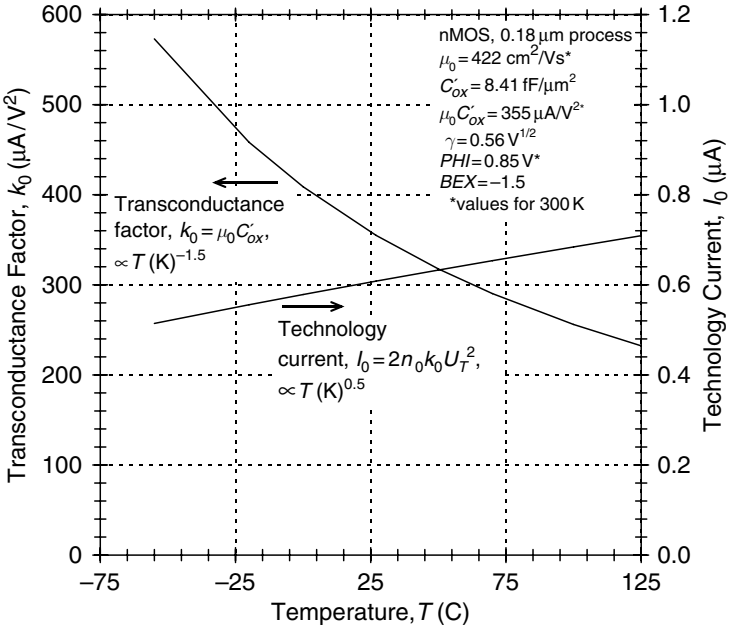

Figure 3.5 Low-field transconductance factor and technology current for the −55 to 125 °C military temperature range for nMOS devices in a 0.18 µm CMOS process. While mobility and the transconductance factor decrease significantly with temperature, the technology current used in the inversion coefficient definition increases modestly because of the increase in the thermal voltage

to T^{BEX}, the absolute temperature raised to the mobility temperature exponent, which is taken as $BEX = -1.5$ for the example process. The technology current, $I_0 = 2n_0 k_0 U_T^2 = 2n_0 \mu_0 C'_{OX} U_T^2$, is proportional to the product of T^{BEX} and T^2 resulting from temperature dependency in the mobility and squared thermal voltage, U_T^2, respectively. As a result, the technology current is proportional to $T^{(2+BEX)}$. This is an interesting result where decreasing mobility is countered by the square of increasing thermal voltage. For a high value of $BEX = -2$, the mobility and thermal voltage temperature dependencies cancel, giving a temperature-independent technology current. On the other extreme for a low value of $BEX = -1$, the technology current is directly proportional to T. For the example here with $BEX = -1.5$, the technology current is proportional to $T^{(2-1.5)}$, or $T^{0.5}$. This is a modest temperature sensitivity, well below that of the mobility or thermal voltage individually. As mentioned earlier, the moderate inversion substrate factor, $n = n_0$, given in Table 3.9, is nearly constant over the −55 to 125 °C temperature range. It contributes little to technology current temperature effects.

Figure 3.5 shows the transconductance factor and technology current over the −55 to 125 °C military temperature range from values given in Table 3.9. Over the military temperature range, the transconductance factor decreases by 60 % while the technology current increases by 38 %. However, over the 0 to 70 °C commercial temperature range, the transconductance factor decreases by 29 % while the technology current increases by only 13 %.

3.5.3 Inversion Coefficient

The increase in technology current, I_0, with temperature means that the inversion coefficient, $IC = I_D/[I_0(W/L)]$ from Table 3.6, decreases with temperature if drain current, I_D, and device shape factor, $S = W/L$, remain constant. Over the −55 to 125 °C military temperature range listed in Table 3.9, the technology current increases by 38 % resulting in an inversion coefficient decrease of 28 % if drain