

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity tb_my_clock is
5  end entity tb_my_clock;
6
7  architecture arch of tb_my_clock is
8      constant T: time := 20 ns;
9      signal t_mclk: std_logic;
10     signal t_rst: std_logic;
11     signal t_clk: std_logic;
12 begin
13     uut: entity work.my_clock(arch)
14         port map(mclk => t_mclk, rst => t_rst, clk => t_clk);
15     process
16     begin
17         t_mclk <= '0';
18         wait for T/2;
19         t_mclk <= '1';
20         wait for T/2;
21     end process;
22     t_rst <= '0';
23 end arch;
```