

Gate Drive Design Tips

In this article, we return to basics of converter design—how to turn on and off the power FET in a modern dc-dc power supply. There have been many articles and application notes on this topic in the past, and the reader is encouraged to read these for more background information [1].

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Direct Drive from the PWM Controller

Most modern control chips incorporate an output driver stage, usually consisting of a totem-pole arrangement of two transistors. This output can be used to directly drive the gate of a power FET, as shown in Fig 1.

The direct connection can be used when the control circuit shares the same ground reference as the power circuit, and power levels are relatively low.

Data sheets show that several amps can be provided from the PWM controller output, more than enough to drive low-power devices. However, a FET input is a large capacitance, and it's usually not a good idea to try and use the full available current. It can lead to increased EMI due to rapid turn-on and turn-off, excessive reverse recovery loss in rectifiers, and noise issues inside the PWM controller itself. Clock jitter, and sporadic interruptions in the normal operations can occur. [2].

It's a good idea to limit the current from the PWM controller with the network shown in Fig. 2. Two resistors are used—one to control the turn-on time, and one to control the turn-off time. A diode is used to separate the two functions, but can be omitted in some cases if the timing is less critical.

We usually turn on the FET slowly when running a low-power converter. Don't be afraid to experiment with the value of the resistor R_{on} . I've used values as low as 1 ohm, and as high as 1 kohm in designs. My rule of design is to increase the resistor while monitoring the switching waveforms and power dissipation in the FET. If the temperature starts to rise significantly, cut the value



of the resistor in half. For a DCM fly-back, it is surprising how slowly you can turn on the device without significant switching loss.

Turn off needs to be faster to provide rapid shut down during overcurrent conditions. Experiment with different values, rather than simply using the values shown in the application notes. For more information on how fast you have to control the FET, refer to [3].

Dedicated Gate Drivers

As power levels rise, you will find the values of the gate resistors need to decrease to minimize switching loss. For higher power circuits, it is common industry practice to use a high-current driver chip. This prevents interference with the PWM controller, and also allows better layout of the PCB. There are many good drivers on the market, or you can even build your own high-current totem-pole driver if you want to raise performance while reducing costs.

Isolated Gate Drives

At higher power levels, we start to use topologies such as the two-switch forward converter, half-bridge converter, or full-bridge converter. All of these topologies require a floating switch to be driven.

There are silicon solutions to this problem. I would use these for low voltage applications, but not for off-line circuits. High-side integrated drivers remove too much control from the

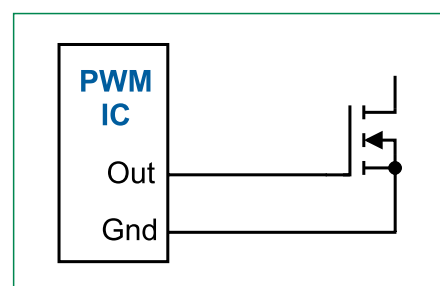


Figure 1: The power FET is driven directly from the output of the PWM controller.

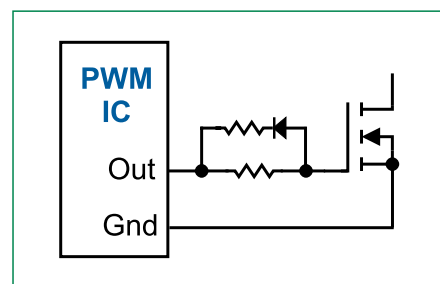


Figure 2: Slow-down resistors are used to control the turn-on and turn-off time of the power FET. We usually turn the device off faster than it is turned on in order to achieve fast current protection.

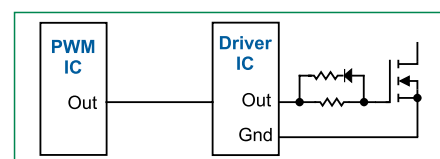


Figure 3: For larger power devices, and higher power switching, it's a good idea to use separate gate drive circuits to switch the devices rapidly. Gate resistors are still used, but are not shown here.

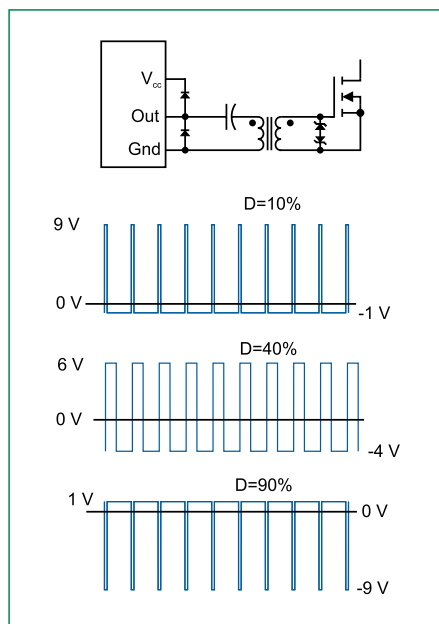


Figure 4: The most rugged scheme for isolated drives uses a gate drive transformer as shown. Catch diodes are needed for reactive current drives, and a dc blocking capacitor prevent saturation of the transformer. The capacitor causes a level shift in the output drive voltage, and this varies with duty cycle.

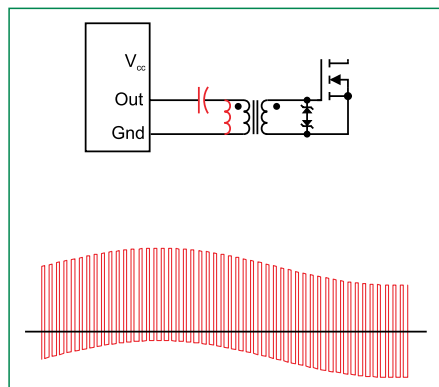


Figure 5: The dc coupling capacitor can ring with the magnetizing inductance of the gate drive transformer, usually during start-up and transients. This ringing should be properly damped to ensure safe operation.

designer, and do not provide the same level of protection, isolation, immunity from transients, or common-mode noise rejection as a well-designed and implemented gate drive transformer.

Fig. 4 shows the most rugged way to achieve a floating drive. The output of the drive chip couples through a dc-blocking capacitor to a small trans-

former (usually a toroid for high performance.) The secondary is connected directly to the gate of the FET, and any slow-down resistors should be placed in the primary of the transformer. Note the use of zeners on the gate for transient protection. Catch diodes are needed at the output of the driver, and should not be omitted even if initial tests show that there is no problem with the reactive current in the transformer.

The circuit of Fig. 4 provides a secondary gate waveform with a negative value when the FET is off. This greatly enhances common-mode noise immunity, crucial for a bridge circuit. However, the negative waveform also has the disadvantage of reducing the voltage applied when the switch is on. At short duty cycles, the positive pulse is largest. At a 50% duty cycle, half the available gate voltage is lost. At large duty cycles, there may not be enough voltage to properly turn the FET on. The transformer-coupled circuit is most effectively used with duty cycles from 0-50%. Fortunately, this is exactly what is needed for the forward, full- and half-bridge converters.

Notice in Fig. 5 that the dc coupling capacitor can give rise to a low-frequency ringing superimposed on the gate drive waveform. The usual solution to this is to use a large value of capacitor which lowers the Q of the ringing waveform. Make sure you test all transient conditions, especially start up when the capacitor is initially discharged.

DC-Restorer Circuit – Watch Out!

Occasionally, you may run into a high-voltage circuit that needs an isolated gate drive close to 100%. In the past, the circuit of Fig. 6 has been recommended for this application.

A diode and capacitor on the secondary restore the dc value of the gate drive, and allow the gate to be driven to duty cycles of up to 90% or more. However, there is a serious flaw in this circuit, and it is not recommended for use without very careful analysis.

The circuit works well during steady-state operation (a gate load resistor is recommended), but when the PWM controller shuts off, the dc blocking capaci-

tor is connected across the gate drive transformer for an indefinite period. This can lead to saturation of the transformer, as shown in Fig. 6b. When the transformer saturates, the secondary is a short circuit, and the secondary capacitor can turn on the FET. The saturation can be avoided with a gapped core, and smaller value of capacitor, but this will increase the reactive current needed from the gate driver, and may produce other problems.

Isolated Gate Drives for the Bridge Converters

The half- and full-bridge converters are isolated applications that need a very rugged drive scheme. During the switch off time, the opposite side of the bridge will turn on, impressing a high common-mode voltage to the off device.

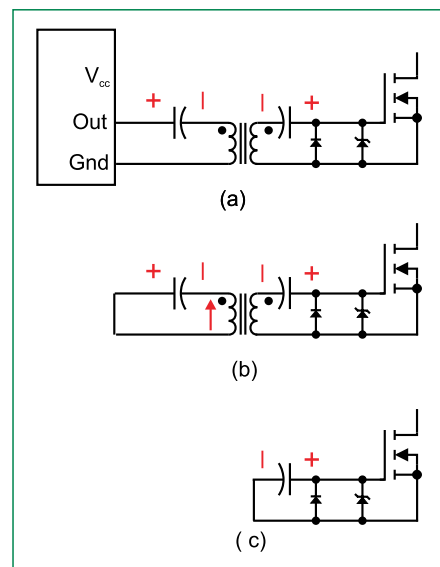


Figure 6: This dc-restorer circuit has been suggested for many years for circuits that require an isolated drive in excess of 50% duty cycle. This circuit can very often lead to failure when the power supply is turned off, and is not recommended.

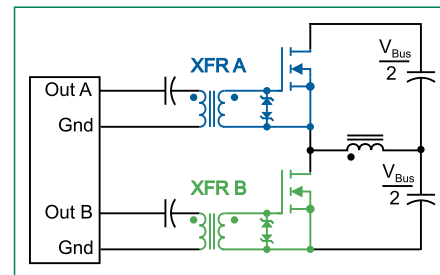


Figure 7: Two separate gate drive transformers are recommended for the half-bridge converter.

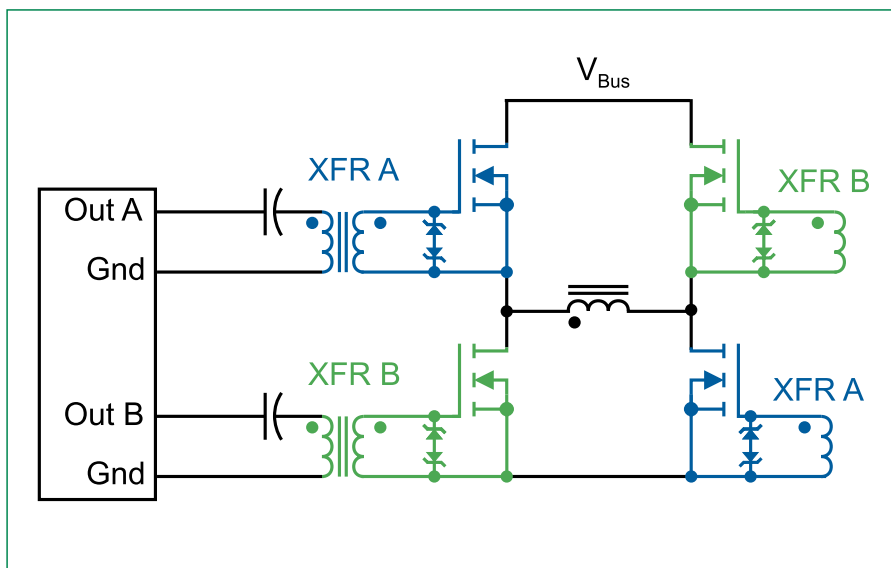


Figure 8: The full bridge converter also uses two transformers for rugged design. Two FETs are driven from two separate secondaries of each gate drive transformer.

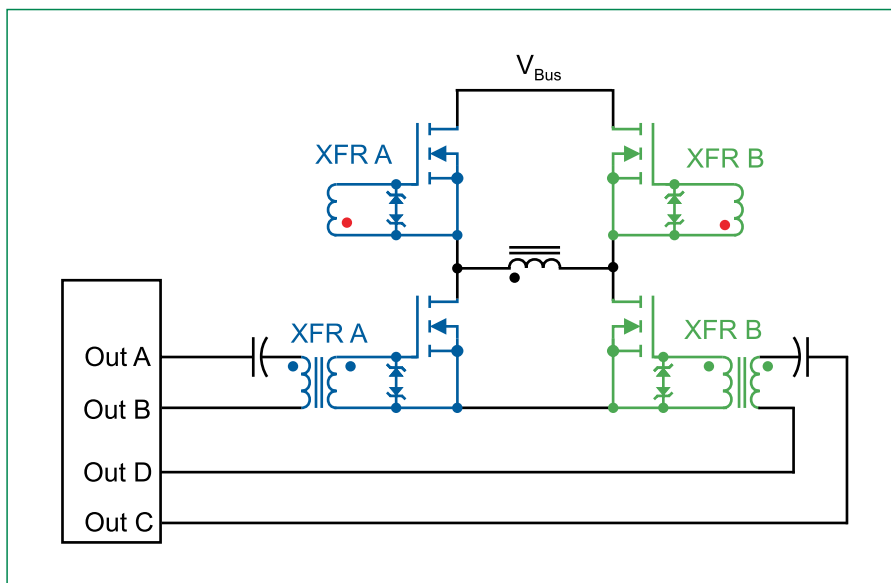


Figure 9: The phase-shifted full bridge uses a bi-directional transformer on each leg, Note the polarity of the secondaries.

Fig. 7 shows the recommended scheme for a half-bridge converter. Two gate drive transformers should be used. Do not try to use just one transformer with a tri-state operation, which may be presented as a technique in some application notes.

The full-bridge converter, shown in Fig. 8, also needs two gate-drive transformers. Dual secondaries on each transformer are used to drive the pair of FETs on the diagonally-opposite legs of the bridge. For both types of bridges,

the gate circuit should be thoroughly tested during start up transients where the highest peak currents are seen, and the negative drive of the gate is the smallest.

The phase-shifted bridge in Fig. 9 also has two gate drive transformers, but notice the different arrangement. Each side of the bridge operates at a fixed 50% duty cycle, allowing the use of single gate drive transformer with dual secondaries of opposite polarities. This is one of the few circuits where the

bipolar drive gate circuit can be used reliably. The only caveat is to be wary of the shut-down condition where ringing waveforms can turn on a device—there is no negative drive under this condition.

Summary

Gate drive circuits are a crucial part of design. Make sure you use the right scheme, and do not blindly copy an application note. Gate drive transformers add a level of ruggedness to your design that cannot be achieved with silicon solutions. If you are designing at high power levels, they are an essential element. While you need to think through all the components in a gate drive, be careful not to overcomplicate the design. Additional active elements to supposedly speed up the device switching do not usually offer improvements in overall performance, but they do introduce new potential failure mechanisms. Keep your gate circuits as simple as possible.

Additional Reading

[1] "Design and Application Guide for High Speed MOSFET Gate Drive Circuits", Laszlo Balogh, Texas Instruments Application Note.

[2] "Six Reasons for Power Supply Instability", Ray Ridley, www.switching-powermagazine.com

[3] "Power Supply Stress Testing", Ray Ridley, www.switchingpowermagazine.com

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Workshop Agenda

Day 1

Morning Theory

- Converter Topologies
- Inductor Design
- Transformer Design
- Leakage Inductance
- Design with Power 4-5-6

Afternoon Lab

- Design and Build Flyback Transformer
- Design and Build Forward Transformer
- Design and Build Forward Inductor
- Magnetics Characterization
- Snubber Design
- Flyback and Forward Circuit Testing

Day 2

Morning Theory

- Small Signal Analysis of Power Stages
- CCM and DCM Operation
- Converter Characteristics
- Voltage-Mode Control
- Closed-Loop Design with Power 4-5-6

Afternoon Lab

- Measuring Power Stage Transfer Functions
- Compensation Design
- Loop Gain Measurement
- Closed Loop Performance

Day 3

Morning Theory

- Current-Mode Control
- Circuit Implementation
- Modeling of Current Mode
- Problems with Current Mode
- Closed-Loop Design for Current Mode w/Power 4-5-6

Afternoon Lab

- Closing the Current Loop
- New Power Stage Transfer Functions
- Closing the Voltage Compensation Loop
- Loop Gain Design and Measurement

Day 4

Morning Theory

- Multiple Output Converters
- Magnetics Proximity Loss
- Magnetics Winding Layout
- Second Stage Filter Design

Afternoon Lab

- Design and Build Multiple Output Flyback Transformers
- Testing of Cross Regulation for Different Transformers
- Second Stage Filter Design and Measurement
- Loop Gain with Multiple Outputs and Second Stage Filters

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