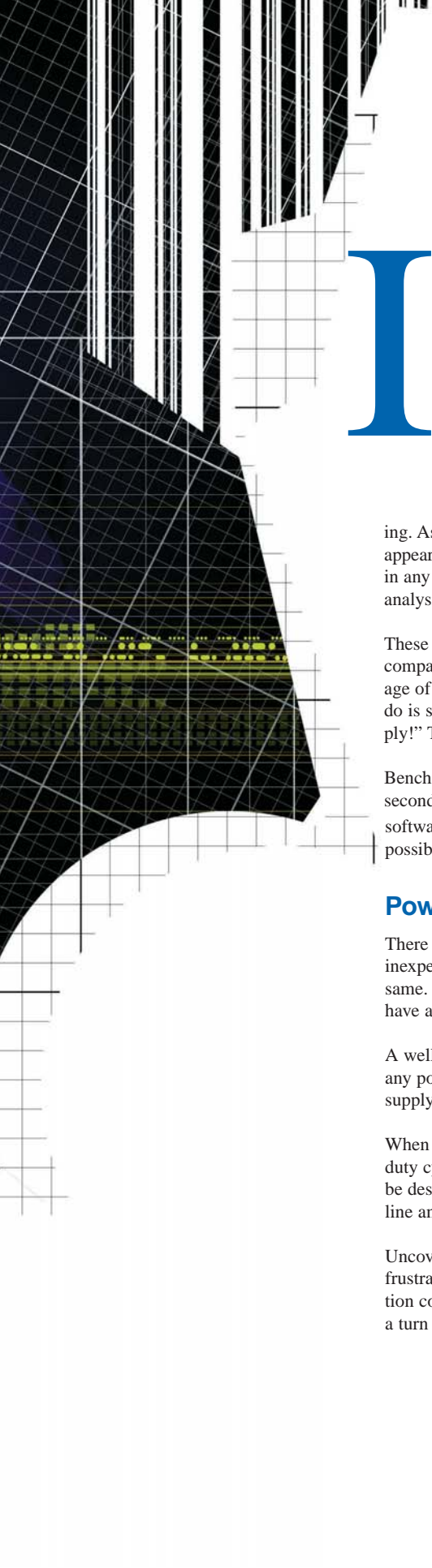




Designers' Series - Part IX

Six Common Reasons for Power Supply Instability

by Dr. Ray Ridley



In past issues of *Switching Power Magazine*, we've talked a lot about control loop design issues, compensation, measurement, and modeling. However, most of this has focused on well-behaved power supplies that are predictable, and which track closely with the theoretical results of small-signal modeling. When you study the theory of power supply modeling, this is the main focus, and still a worthy topic for graduate research. Yet so many power converter topologies and modes of operation have never been modeled.

We are often asked to help companies characterize their control-loop modeling. As we analyze each power supply on the bench, several development problems appear—consistently. What's alarming is that you won't find these problems covered in any university textbook. It is assumed that these issues are already solved before the analysis and loop measurement begin.

These development problems are often overlooked by IC controller semiconductor companies. In fact, a recent advertisement from one well-known vendor states, "the age of testing power supplies in the lab with an oscilloscope is over. All you need to do is simulate on line with a simple software model, then build the final power supply!" This couldn't be further from the truth.

Bench testing is still an integral part of power supply development, and some of the second-order issues will never show up on a simulator. Our philosophy is to use design software by all means, but only to the point of achieving a lab prototype as fast as possible. Don't plan on skipping this vital step, or your project could be in trouble.

Power Supply Instability

There are many mechanisms in a power supply that can cause instability. And to the inexperienced designer, they can all look the same on the oscilloscope and sound the same. (Yes, you can usually hear an unstable power supply.) In fact, even when you have a lot of experience, identifying *which* problem you have can be difficult.

A well-behaved power supply should be silent, both electrically and acoustically. Yet any power supply designer is painfully familiar with the hashy sound of an unstable supply. It sounds a lot like a modem connection.

When working properly, a power supply should smoothly move through its range of duty cycles without jitter, oscillation, or any pulse-skipping. Many power supplies will be designed and shipped with regions of noisy operation for certain combinations of line and load.

Uncovering the underlying cause of noisy operation can be very time-consuming and frustrating, especially if you don't know the list of possibilities. Changing compensation components can help in some regions, but not in others. Problems can go away in a turn of the PC board, only to re-emerge later.

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Day 1

Morning Theory

- Converter Topologies
- Inductor Design
- Transformer Design
- Leakage Inductance
- Design with Power 4-5-6

Afternoon Lab

- Design and Build Flyback Transformer
- Design and Build Forward Transformer
- Design and Build Forward Inductor
- Magnetics Characterization
- Snubber Design
- Flyback and Forward Circuit Testing

Day 2

Morning Theory

- Small Signal Analysis of Power Stages
- CCM and DCM Operation
- Converter Characteristics
- Voltage-Mode Control
- Closed-Loop Design with Power 4-5-6

Afternoon Lab

- Measuring Power Stage Transfer Functions
- Compensation Design
- Loop Gain Measurement
- Closed Loop Performance

Day 3

Morning Theory

- Current-Mode Control
- Circuit Implementation
- Modeling of Current Mode
- Problems with Current Mode
- Closed-Loop Design for Current Mode w/Power 4-5-6

Afternoon Lab

- Closing the Current Loop
- New Power Stage Transfer Functions
- Closing the Voltage Compensation Loop
- Loop Gain Design and Measurement

Day 4

Morning Theory

- Multiple Output Converters
- Magnetics Proximity Loss
- Magnetics Winding Layout
- Second Stage Filter Design

Afternoon Lab

- Design and Build Multiple Output Flyback Transformers
- Testing of Cross Regulation for Different Transformers
- Second Stage Filter Design and Measurement
- Loop Gain with Multiple Outputs and Second Stage Filters

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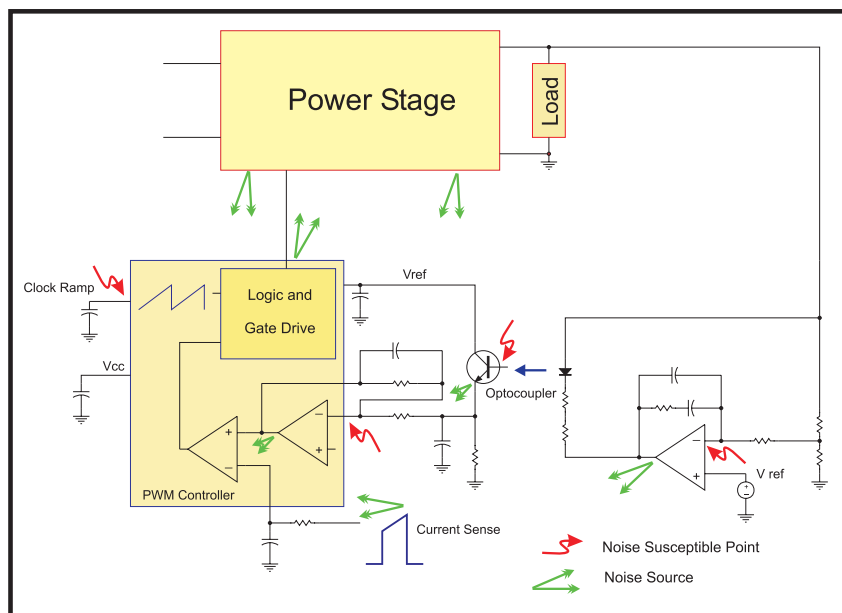


Figure 1: Feedback System

We have identified at least 6 different categories of mechanisms for apparent “unstable” operation. Only two of these are classic control loop instability theories discussed in textbooks.

The problems discussed in this article are:

- Amplifier noise pickup through any active devices, including operational amplifiers and optocouplers
- Control chip component placement
- Operation too close to maximum duty cycle
- Light load operation
- Current waveform filtering.
- Classic current-loop oscillation
- Voltage-loop compensation

Typical Control Circuit

Figure 1 shows a typical feedback system for a power supply with an isolated output. A voltage amplifier and reference on the secondary are used for the main compensation, referred to in most articles about power supply control design. The output of the amplifier feeds an optocoupler diode, and the transistor output of the optocoupler is configured as an emitter follower on the primary of the power supply.

The internal error amplifier of the PWM controller is set up with a gain of 2 to 4 times. This reduces the need for a high gain secondary amplifier, and reduces the voltage range needed from the optocoupler.

Amplifier Noise Pickup

As switching frequencies rise, and demands on transient response become more stringent, companies are pushing for higher gains in their feedback loops. That often necessitates high gain-bandwidth error amplifiers. The problem with these amplifiers is that they will pick up stray RF signals, and amplify them through to their output.

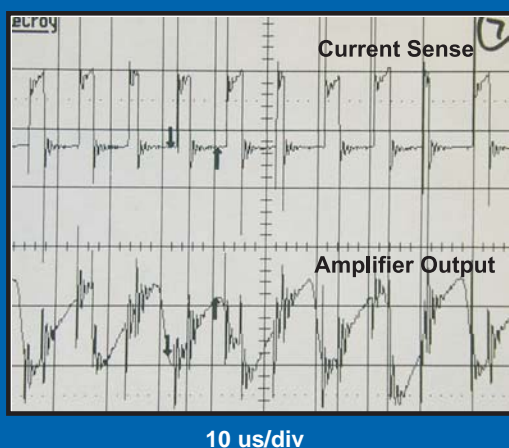


Figure 2a: Operational Amplifier Noise

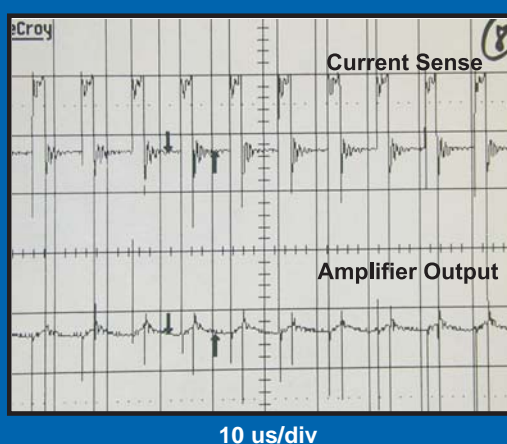


Figure 2b: Operational Amplifier Noise after Filtering

Even though you may have configured the amplifier with a feedback capacitor to have very low gain at high frequencies, RF noise can pass through due to input off-sets and other mechanisms.

This is shown clearly in Figure 2a. The secondary-side amplifier output is shown with a large amount of ripple (400 mV) at the switching frequency. The ripple gets through to the PWM modulator output, and can cause pulse-skipping and subharmonic oscillation. The subharmonic oscillation amplifies the effect of the error amplifier ripple.

A small RC filter at the output of the error amp can fix this problem. The time constant is placed at about half the switching frequency to minimize the effect on the loop phase margin. Filtered waveforms are shown in Figure 2b.

It's not only the operational amplifiers that can cause this problem. Any amplifying device can do this. A common problem in power supplies is the base lead of the optocoupler, which can also pick up EMI and cause improper operation. The solution to this can be as simple as cutting off the base lead connection on the optocoupler package before placing on the PC board. Some vendors even supply their parts this way, without the base lead brought out of the package.

Control Chip Layout

Layout of components around the power supply control chip is crucial, as shown in Figure 3. The clock signal of the control chip is the most sensitive area. The timing capacitor must be placed as close to the pins as is physically possible.

Operation Close to Maximum Duty

The clock has been cleaned up with proper placement of capacitors on the clock pin. But at low line, the jitter problem returns, as shown in Figure 4.

You can never get rid of all the noise in the system. When the power supply operates close to maximum duty cycle, the residual clock noise is enough to trip the clock comparator, and prematurely end the clock timing signal. In this waveform, alternate waveforms show the turn-off noise tripping the clock signal early.

Light Load Operation

Another problem arises at the opposite end of the operation—light load and high line. Under this condition, the duty cycle is at a minimum, and only the beginning portion of the control ramp is used. With voltage-mode control this is not usually a problem, but with current-mode control, pulse skipping operation can be unavoidable at very light loads.

Figure 5 shows an example of this. The clock ramp is clean, the output of the PWM error amplifier is close to its minimum value. On every third cycle shown, it drops below the minimum value required for the power switch to be turned on, and the complete pulse is skipped.

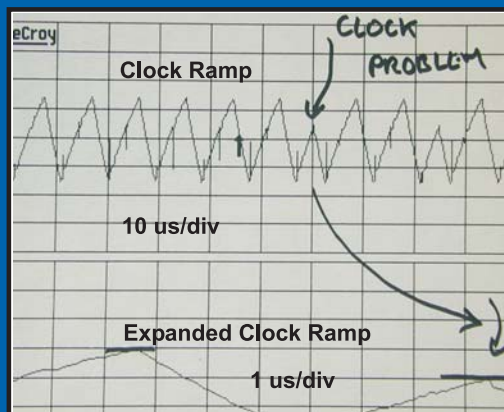


Figure 3: Early Clock Ramp Reset Due to Improper Layout

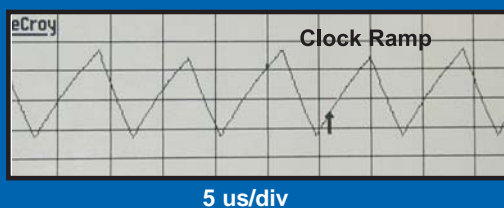


Figure 4a: Early Clock Ramp Reset due to Operation Close to Maximum Duty Cycle

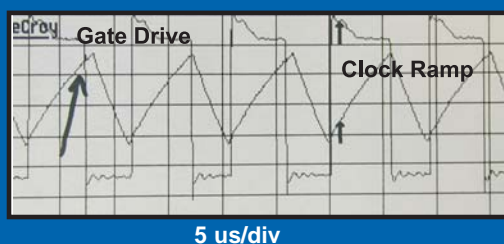


Figure 4b: Same Event as 4a, with Gate Drive Waveforms

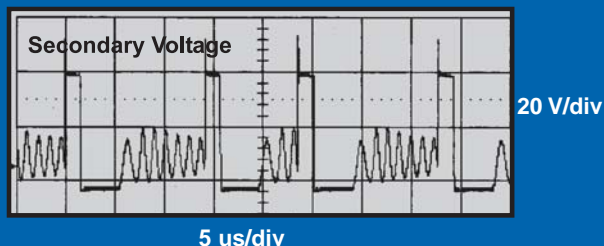


Figure 5: Pulse-Skipping Operation at Light Load and High Line

Frequency Response Measurement



USB port compatibility.

Designed specifically for switching power supplies, the AP200 makes swept frequency response measurements that give magnitude and phase data plotted versus frequency.

Features

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Magnetics

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| PC Data Transfer | Automatic |

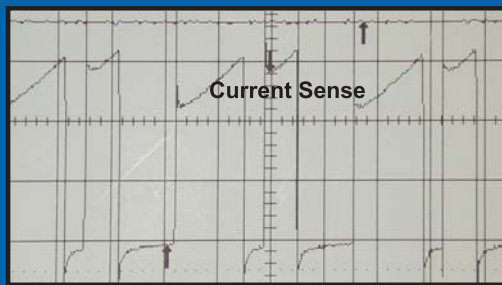
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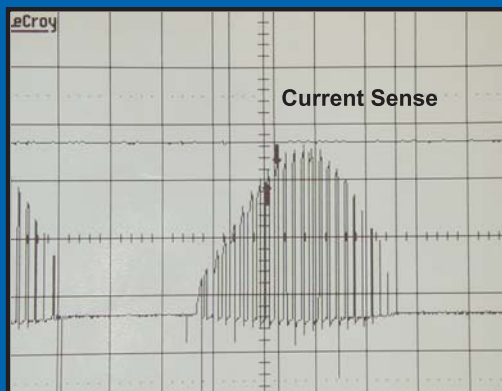
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5 us/div

0.2 V/div

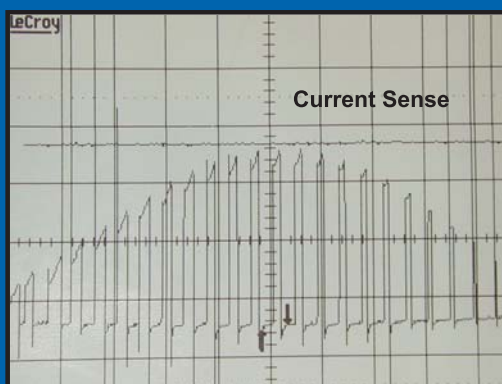
Figure 6: Classic Current-Mode Oscillation Around 50% Duty Cycle



50 us/div

0.2 V/div

Figure 7a: Sinusoidal Oscillation Due to Insufficient Phase Margin in Feedback Loop



20 us/div

0.2 V/div

Figure 7b: Expanded Waveform

The waveform shown in Figure 5 is the secondary of the power transformer of a forward converter. The converter is operating in discontinuous conduction mode. Notice the ringing in the waveform, the frequency of which is determined by the output filter inductor of the converter, and parasitic capacitances. This ringing can also impact the noise level of the system, and can cause some strange effects on the control loop characteristics.

Current Waveform Filtering

This is the first of the problems explicitly dealt with by control chip notes. The turn-on spike of the sensed current can be large enough and wide enough to prematurely turn off the PWM comparator. We've talked about this in earlier issues of SPM, and the phenomenon is well known. There are two common solutions—filtering the sensed current waveform, and (these are often combined) “leading-edge blanking” where the current-sense signal is ignored for a short period of time by the PWM function.

Both of these solutions have problems if the power supply needs to operate at very short duty cycle. With excessive filtering, the current sense waveform information is inaccurate at the start of the waveform. This can lead to a system that has characteristics more like voltage-mode control, and the compensation may not give enough phase margin.

If the desired duty cycle becomes less than the leading edge blanking period, the power supply will enter into a pulse-skipping mode. This will cause audible noise and operation similar to the problems observed above.

Current Loop Instability

Finally, we get to the first of the classic power supply instability problems that are talked about in the analysis papers and articles. You've got to fix all of the above issues before this can be clearly seen.

When using current-mode control, the system will enter a subharmonic oscillation as you approach 50% duty cycle. This results in a long pulse, followed by a short pulse, as shown in Figure 6.

Note: when this happens, be sure to check the clock signal. Despite the apparently chaotic operation of the supply here, the clock pulse should be stable once the above problems are fixed. If it's not, you still need to clean up the layout and signals.

The solution to the current loop instability is well known—add a compensating ramp. However, as shown above, it is crucial that you don't try to use the clock ramp signal to generate this. Alternate solutions have been shown in earlier editions of Switching Power Magazine, and you can find these at our web site. (www.switchingpowermagazine.com)

Only Need One Topology?

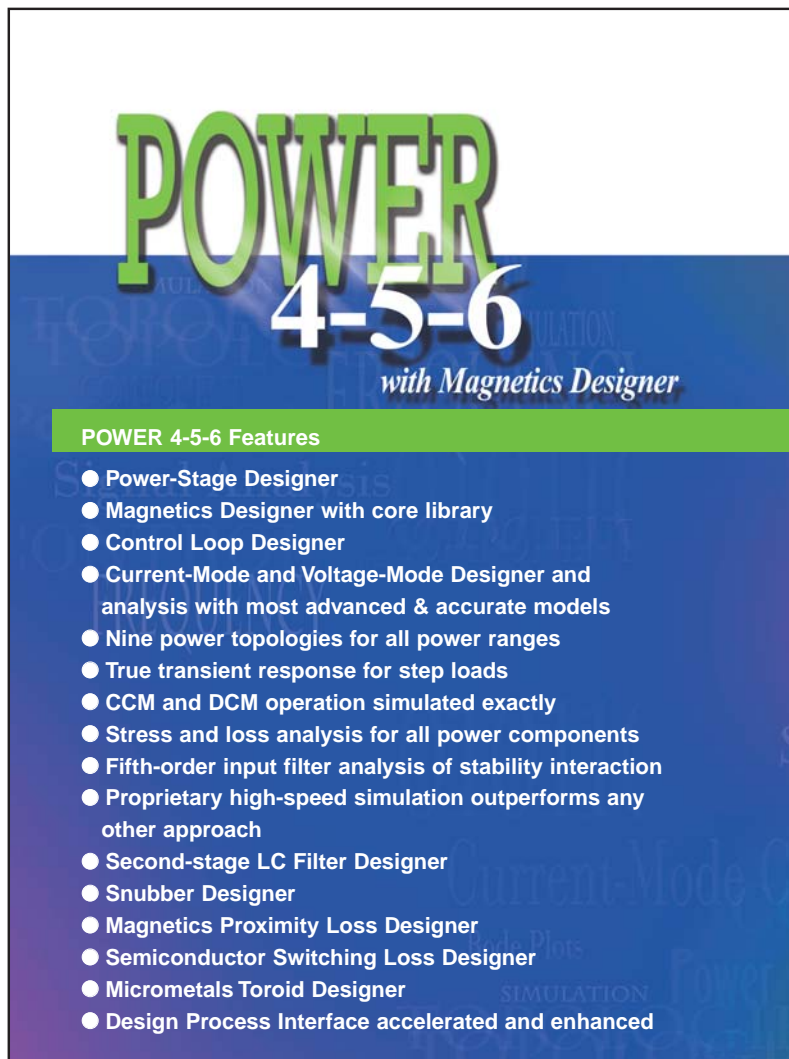
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Voltage Loop Instability

Finally, after fixing the five problems above, you can concentrate on the issue of loop compensation. While many designers view this as the most complex part of power supply design, once you have the proper tools and understanding, it takes relatively little time to compensate a loop properly. All you need to change are component values on the board. The other issues frequently require a new board layout.

The waveforms are different than the other observed behaviors discussed in this article. You can usually hear the oscillation as a fairly high-pitched tone (1-10 kHz), but without the white-noise characteristics. The circuit waveform envelopes are typically sinusoidal, limited by the minimum and maximum duty cycle available, as shown in figures 7a and 7b. There is usually a smooth transition of duty cycle widths from one pulse to the next, rather than the subharmonic characteristics of the other forms of instability.

Although these seem like minor issues, they can be monumental in achieving success in power supply design. Until all of these instability issues are solved, the control compensation design should not take place. The symptoms will only multiply throughout the next generation of processes in your design.