A Switched Opamp-based 10-b Integrated ADC for Ultra Low-power Applications

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Abstract

This paper describes an ultra low-power switched opamp-based integrated ADC designed using a cyclic algorithm approach, for cardiac pacemaker applications. The A/D converter shows a typical operating power consumption of 8.18 μW for the analog part and of 9.71 μW for the digital one, whereas the stand-by dissipation is about 1 nW and 5 nW, respectively, (measured on 10 chip samples and averaged), considering a typical supply of 2.8 V. The ADC has a resolution of 10-b, its typical operating clock frequency is 32 kHz (2.9 kS/s sampling rate) and it is able to reach the same resolution at 2 V, with 0.7 kS/s sampling rate, showing a dissipation of 1 μW for the analog part and 1.3 μW for the digital part. It is also characterized by low offset and no missing codes.

1. Introduction

The Switched Capacitor (SC) technique needs a particular attention in switch design when used at low supply voltages. In fact, the signal swing applied in these cases is dramatically reduced when a very low supply voltage is used [1]: complementary switches and op-amps do not efficiently work because of the insufficient switch overdrive. These problems can be solved by the use of a switched-opamp (SOA) technique, instead of SC, to overcome the typical impairments of low-voltage low-power systems [2-7].

This paper describes a switched-opamp implementation of a cyclic algorithmic ADC that leads to very low power consumption. The architecture complies with the constraints of a biomedical implantable application: ultra low-current consumption lower than 4 μA, typical supply voltage of 2.8 V (but the circuit maintain its performance at 3.5 V and 2 V supply). Moreover, the ADC can be put in power-off mode, wakening it only when needed. The technology used is a BiCMOS 0.8 μm, with 2-M and 2-P layers.

2. The ADC architecture

The aim of this paper is the design of an integrated ultra low-power consumption A/D converter which operates with a standard battery supply for cardiac pacemaker applications (operating from 3.5 V down to 2 V), with a resolution of 10-b, conversion rate higher than 2 kS/s, input dynamic range of 800 mV and small silicon area.

This performance has been obtained using a cyclic conversion algorithm with the SOA technique. The choice of this approach instead of others is motivated by the following considerations. Both pipeline and sigma-delta approaches could have been used in applications (biomedical also) where either conversion rate or resolution are requirements more important than consumption and silicon area. In fact, the pipeline architecture is able to achieve a high conversion rate (also in low voltage applications [9]), but it consists of a series of identical stages that consume additional power, whereas the sigma-delta approach can be used in high-resolution applications (> 16-b), in which hardware simplicity and conversion rate are not the main issues.

Moreover, a successive approximation architecture (SAR) using a very low supply voltage allows one to achieve medium-speed/medium-resolution converters with a low-power consumption and using standard threshold CMOS devices. The results shown in the literature [11] indicate that SAR approach is well suited for operation even below 1 V (around the threshold voltages of the device used), but the very low current dissipation (~30 μA) is achieved with a supply voltage of 1 V. In cardiac pacemaker application, the standard battery used establishes the supply voltage value to the typical value of 2.8 V, and thus the same value of dissipation has to be reached at a voltage value larger than 1 V. On the other hand, SOA technique can be used in our application because the main goals of this technique are not only the capability of reducing the supply voltage and overcoming the limits due to the switches overdrive. In fact, the possibility of completely turning "on" opamps only in one of the two phases of the main clock, being the opamp switched-off in the other phase, allows one to halve the power consumption of the entire system. This is a great advantage, especially for systems employed in biomedical applications and particularly in pacemakers, where low-voltage and low-power requirements are mandatory.

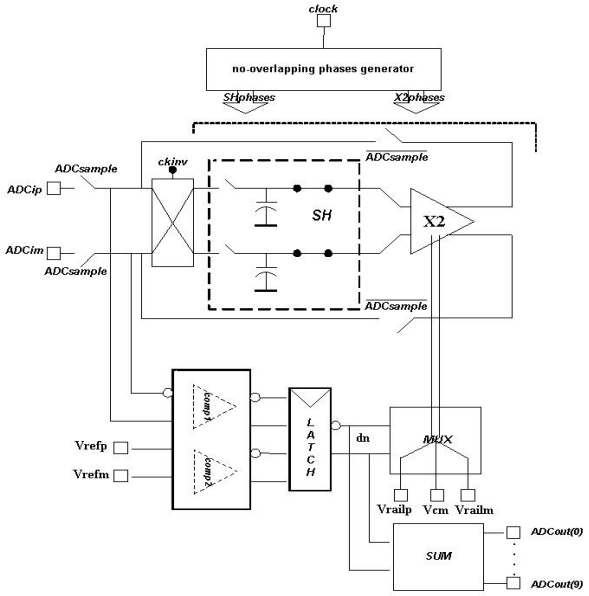

Fig. 1. ADC schematic diagram

Fig. 1 shows the schematic diagram of the ADC described in this paper. The architecture is a classical Cyclic/Algorithmic topology with 1.5 b per cycle, consisting of three main blocks: a Sample and Hold (indicated with SH in Fig. 1), some comparators and a Multiplying DAC (indicated with X2). The ADC works as follows:

- when *ADCsample* is asserted (see Fig. 1), any analog signal present between *ADCip* and *ADCim*, that is sampled through the input switches of SH during the first phase (*phase1* in Fig. 2), is converted by the two comparators (that act as a flash sub-ADC) in a 2-b digital number;
- then *ADCsample* is removed, the SH block holds the sampled signal while X2 samples the SH output. At this time the input switches are opened and a loop is created between X2 and SH.

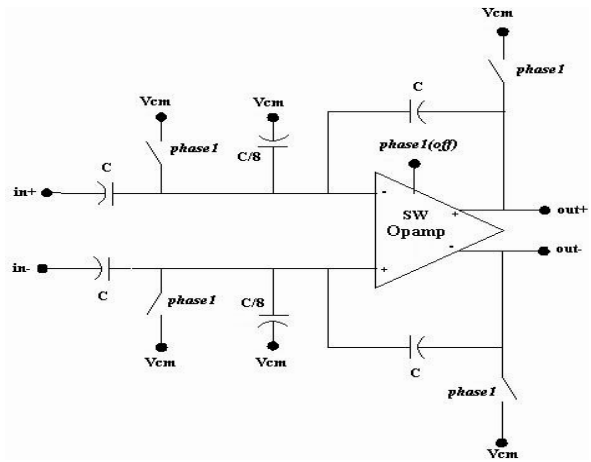

Fig. 2. SH architecture

During the following clock cycles (*phase1-phase2*), the operation continues: the SH block samples the X2 output feedback, this signal is compared by the two comparators and the X2 block multiplies by two the SH output. If necessary, a reference voltage is added or subtracted to it, according to the result of the comparison.

The ADC needs 11 clock cycles (32 kHz) to produce a 10-b output code. A new conversion begins (and a new input analog signal is processed) when *ADCsample* becomes active again. If V_{in} is the voltage difference between the SH inputs, V_{ref} is the voltage reference ($V_{ref} = V_{railp} - V_{railm} = \frac{input\ dynamic\ range\ ADC}{2}$), V_{resn} is the voltage residue at X2 output of *n*-th conversion cycle and d_n the respective binary code, then the algorithm works as follows for each clock cycle:

$$Vresn = \begin{cases} 2V_{in} - V_{ref} & if \quad V_{in} > \frac{V_{ref}}{4} & d_n = 10 \\ 2V_{in} & if \quad -\frac{V_{ref}}{4} \le V_{in} \ge \frac{V_{ref}}{4} & d_n = 01 \\ 2V_{in} + V_{ref} & if \quad V_{in} < -\frac{V_{ref}}{4} & d_n = 00 \end{cases}$$

The digital result d_n is the input of the block SUM that encodes the output.

The SOA technique, traditionally used to reduce the operating supply voltage [9], is mainly used in this case to achieve a reduced power consumption, for a 2 V minimum supply: in fact, if SH is "on", X2 is "off" and vice versa. When a block is off, the SOA output stage is in high impedance and is pulled to *Vcm* (common-mode voltage of the ADC) by the related switches.

Fig. 2 shows the SH architecture employed in this design. It consists of switches (in a transmission gate configuration), a SOA, two sample capacitors *C*, two hold capacitors *C* (of the same value) and two capacitors having a value of *C*/8, that avoid large spikes on the virtual ground to be traded-off with the offset that these capacitors produce.

During $\overline{phase1}$ (sample phase), the charge is stored on the sampling capacitors *C* and SOA output stage is in high impedance. In order to minimize the delay caused by the slew-rate, that can be high in low-power applications, SOA output stage is pulled to the middle of the dynamic output range (*Vcm*) in this phase. During *phase1*, the inputs of this stage are pulled to *Vcm* (while the output of the X2 stage is pulled to *Vcm*), then SOA is turned "on" and all the switches are turned "off". As a consequence, the charge is stored on the sampling capacitors of the X2 stage.

Fig. 3 shows the X2 architecture. There are two capacitors with the same value of the hold capacitors (*C*/2), in order to obtain a 1.5-b requirement. During *phase2*, the charge is stored "on" the sampling capacitors (through the hold phase of the SH stage), *C*/2 input capacitors are pulled to *Vcm* (as in the output stage of the SOA). At the end of *phase2*, the amplifier is turned "on". During the following phase (*phase1*), the *C*/2 input capacitors are pulled to one of the *Vrail* voltages, depending on the result of the $\pm V_{ref}/4$ comparison. In this

way, the subtractions or additions described before are executed. It is worth noting that the 0.5-b redundancy is obtained using only two non-overlapping phases (*phase1-phase2*) and the complementary ones (since all the switches are implemented as transmission gates).

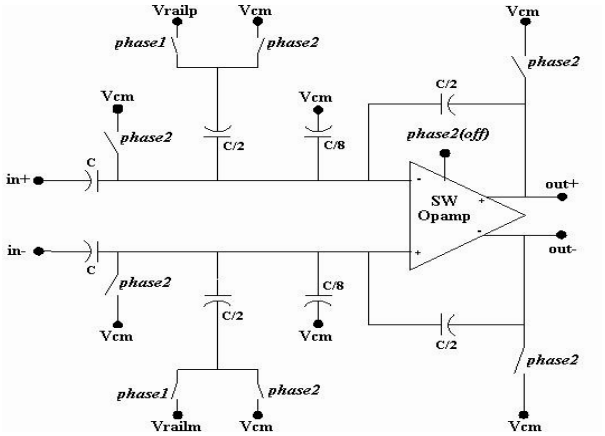

Fig. 3. X2 architecture

2.1. Switched Opamp

The amplifier employed in the ADC analog core is a simple 2-stages Miller compensated OTA (Fig. 4). The amplifier has a fully differential architecture, mainly to improve PSRR and to enhance the signal swing. It has also an active CMFB circuit.

During the opamp inactive phase, the output branches are turned "off" and the input stage is kept "alive" to guarantee a fast turn-on of the amplifier. The dissipation is 150 nA for the input stage and 1 µA for the output stage (500 nA per branch). This means that the current consumption, excluding CMFB circuit, is 1.15 µA during on-phase and 150 nA during off-phase.

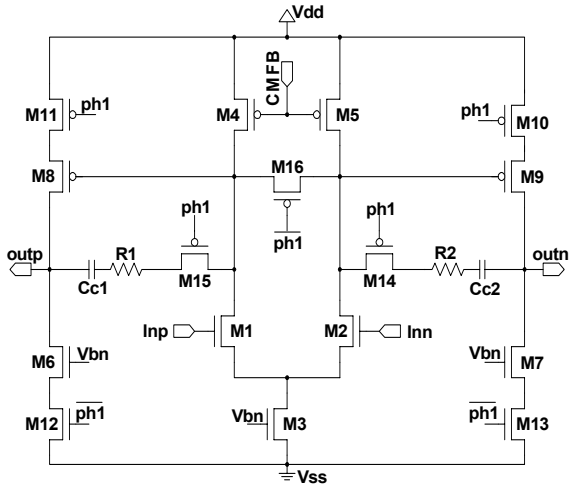

Fig. 4. Fully differential Switched Opamp

A special attention was paid in designing M4 and M5 in strong inversion (as they work as current mirrors), and the input pair M1, M2 in weak inversion, designing the OTA with suitable dimensions and layout in order to reduce the offset. Switches M14 and M15 prevent the discharge of the compensation capacitors during the off-phase of the opamp, thus allowing a fast recovery. Moreover, a switch (M16) between the drains of the input transistors shorts them during the inactive phase, so avoiding the saturation of the input stage caused by the absence of feedback.

The fully differential opamp needs a Common Mode FeedBack (Fig. 5) to work properly. A switched capacitor approach was chosen due to its simplicity and the high linearity it can give.

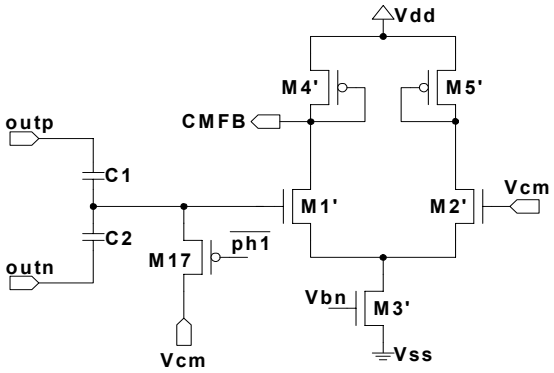

Fig. 5. Common Mode FeedBack circuit

The outputs are averaged by *C*1 and *C*2 during on-phase; this averaged voltage is the input of a simple opamp (replica of the input stage of the main amplifier) and is compared to the wanted Common Mode Voltage (*Vcm*). A feedback signal is generated (CMFB) that controls the current of the input stage of the main opamp (see Fig. 4).

During the off-phase, capacitors *C*1 and *C*2 are reset (*outp* and *outn* are put to *Vcm*) through switch M17 and the Common Mode FeedBack is kept "on", to be ready for the next phase.

Parameter	Value	Unit
Supply Voltage	2÷3.5	V
Temperature	-15÷45	°C
Ao	101	DB
GBW	387	KHz
PM	60	Deg
SR (min)	0.12	V/µs
Idc	1.305	µA
Area	0.081	mm^2

Table 1. Op-Amp simulation results

Table 1 summarises the main performance obtained during the simulation of the entire opamp with a load of 4 pF. As shown, the gain is very high (more than we need to reach the required linearity) thanks to the two stages architecture. It is worth noting that slew rate requirements are heavily reduced in this application, thanks to the fact that output stages are pulled to *Vcm* during the inactive phase.

2.2. Comparators

In order to produce a 0.5-b redundancy, two comparators have been used in this design. It is important to note that a 1 bit per cycle architecture needs only one comparator, but it is not possible to relax the offset requirement, and the technique described in the next Section does not produce those advantages in terms of integral and differential non linearity. In this design a Input Offset Storage (IOS) method is used, in which the offset cancellation is performed by closing a unity-gain loop around the preamplifier and storing the offset on the input coupling capacitors [10].

2.3. Offset reduction in the amplifiers

In both SH and X2 blocks, the autozero operation of the amplifier allowed in classical SC architectures cannot occur because in the sample phase (*phase1* for SH for instance) SOA output is "off", so, this effect results in a huge loss of codes and potential linearity problems.

However, in the second clock cycle (the first after *ADCsample* "on"), the SH inputs are inverted, through the signal clock *ckinv*. At the third clock cycle *ckinv* (Fig. 1) turns "off" and normal conditions are restored. So, the offset stored the first time, that at the end of conversion is multiplied with 2^{N-1} (N = number of bits of the ADC), is subtracted with next offsets (next clock cycles) that are multiplied with 2^{N-k}, where $k = 2..10$ is the number of the clock cycle. This also means that, after *ADCsample* is "on", the residual signal of conversion is inverted: the SUM block thus needs additional logic [8].

2.4. ADC timing diagram

The reset signal asynchronously initialises the digital section of the ADC: the output register is loaded to "0" as conversion result, but *ADCdav* is low so this is not considered a valid result. An initialisation is recommended each time a new data acquisition begins, but the reset pulse width must be as short as possible to minimise power supply consumption.

The ADC timing diagram is shown in Fig. 6: the acquisition mode is "free running" and the data stream is collected by a microcontroller which can operate in edge mode or level mode. In fact, *ADCdav* raises each time that a valid data conversion is available (edge triggered) and remains stable until the ending of a new conversion (level triggered). The "one shot" acquisition mode is a trivial sub case.

The ADC starts when it wakes up from stand-by condition. The internal state is bounded to rising edge of the clock; an initial start up time allows the analogue part to reach a steady state and then the conversion starts (the internal signal *ADCsample* is shown for clarity) on the falling edge of the clock.

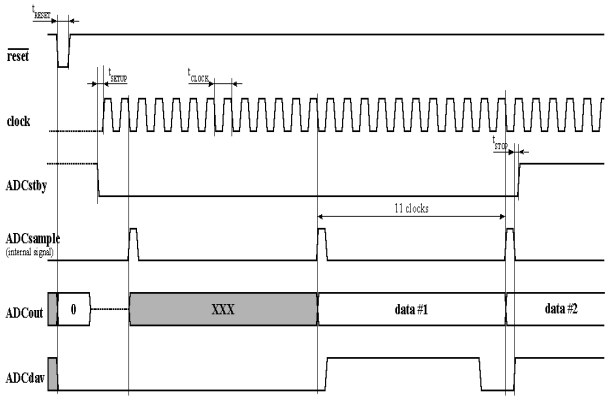

Fig. 6. ADC timing diagram

To process the input value, the ADC takes 10 clocks plus an additional clock to reinitialise the internal logic. The data output *ADCout* [9:0] is registered, so the data is stable until the register is updated.

3. Experimental Results

The A/D integrated converter was fabricated in a 0.8 μm BiCMOS technology with 2 Metal and 2 Poly layers. The ADC described in the previous Section has been designed as a part of a prototype chip developed for implantable pacemakers (the chip microphotograph is shown in Fig. 10). The front-end section consists of an input amplifier with AC coupling - externally provided - to avoid input offset amplification, a low-pass filter, and the 10-b ADC.

The prototype includes a bandgap referred to ground, five voltage buffers to provide the proper references for ADC operation and device common-mode operation.

The chip is pad-limited and the silicon area could have been reduced (see Fig. 10), if no test pad was used in our prototype. In fact, the ADC cell area is about 0.8 mm^2. Table 2 shows the operating conditions of the A/D converter. Nevertheless, all prototype have been characterised with different combinations of power supply, clock rate and bias current, showing a proper functionality in all the conditions.

Power Consumption	Supply Voltage (V)	Clock rate (kHz)	Bias Current
Maximum	3.5	32	Full
Typical	2.8	32	Full
Minimum	2	8	¼ Full

Table 2. Measurement condition

A very low power consumption has been measured for the analog core when reduced power supply, clock rate and bias current has been chosen: 0.56 µA in the minimum case. Digital core dissipation (see Table 3) is rather high for the target application (with consumption of the analog part exceed 4 µA in typical case), but no particular attention has been paid to this point, because of the following considerations:

- in implantable devices applications, an embedded processor that can implement the main part of the digital section of the ADC is commonly available.
- No low power digital library was available for the considered technology, so a standard digital library has been used.

Measurement Condition	Minimum	Typical	Maximum	Unit
Resolution		10		bit
Consumption (Analog Part)	0.56	2.92	3.9	µA
Consumption (Digital Part)	0.67	3.47	4.17	µA
INL	1.13	0.98	0.85	LSB
DNL	0.73	0.67	0.75	LSB
Input Noise	0.43	0.42	0.4	mV rms
Offset	0.72	0.73	0.7	mV
THD	56.6	56.3	57.6	dB
SFDR	60.2	59.6	61.1	dB
ENOB	8.4	8.4	8.4	bit
Offset drift	-	21.4	-	µV/°C
Gain drift	-	100	-	ppm/°C
Active Area		0.8		mm^2
Technology		AMS 0.8µm BiCMOS		

Table 3. Summary of the ADC performance

The measured DNL curve (typical case) and the measured output spectrum (2048 point FFT spaced 1.42 Hz each other) of a reconstructed 200 Hz full-scale sine wave sampled at 2.9 kS/s with a supply voltage of 2.8 V are shown in Fig. 7 and Fig. 8, respectively. The maximum value of the measured DNL is approximately of 0.7 LSB (see also Table 3). The main measurement results are summarized in Table 3.

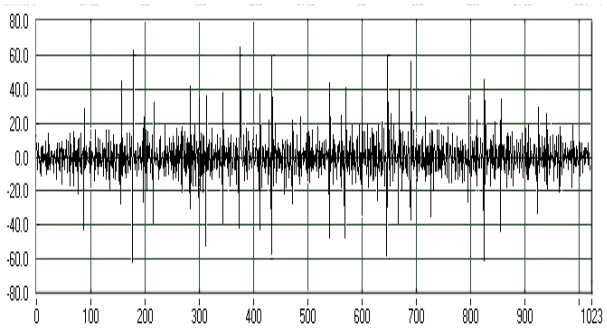

Fig. 7. Measured DNL (LSB*100) in typical condition

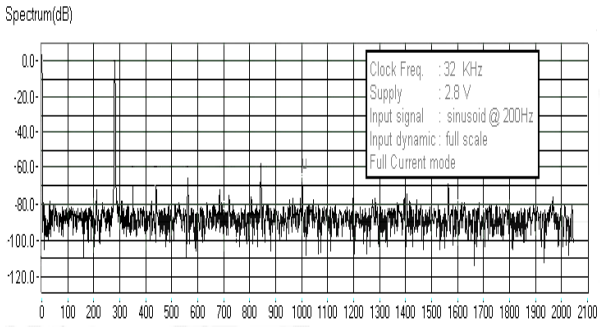

Fig. 8. Output spectrum for a 200 Hz input signal

The measured offset, INL and Gain as a function of the temperature (in the range –10/+75°C), in typical case, are shown in Fig. 9.

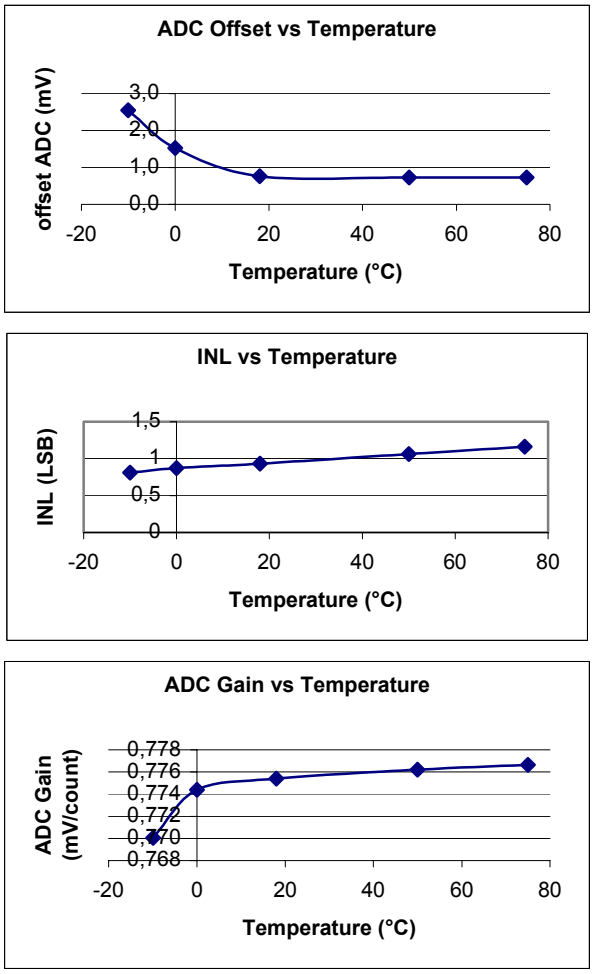

Fig.9. Offset, INL and Gain versus Temperature

It can be noticed (see Fig. 9) that the functionality of the ADC is guaranteed in a wide range of temperature.

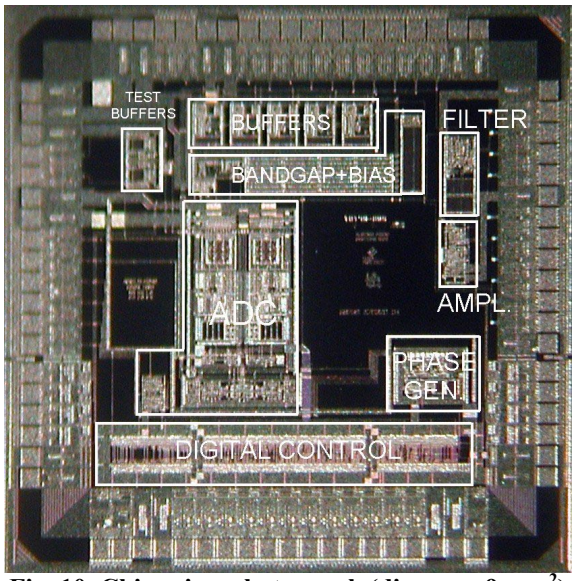

Fig. 10. Chip microphotograph (die area: 9 mm^2)

4. Conclusions

Implantable biomedical devices are asked to operate for a long time with long-life batteries (with a duration of at least 6 years) and the resolution of the sensing channel is going to increase (more than 8-b). Most of the existing ultra low-power ADCs are not capable of a resolution as high as 10-b.

In this paper we have shown how the SOA technique can be used to achieve 10-b resolution for an ADC to be used in a cardiac pacemaker characterized by an ultra low-power consumption, a low die area and the cyclic conversion algorithm approach.

Moreover, the measurements carried out on the ADC prototypes demonstrate the full functionality of it with no missing codes, with a consumption of 1.23 μA, 0.7 kS/s sampling rate and 2 V supply voltage.

References

[1] A. Baschirotto, R. Castello, F. Montecchi, "Design strategies for low-voltage SC circuits", *Electronics Letters*., vol. 30 n. 5, , 30 March 1994, pp. 378-380.

[2] J. Crols, M. Steyaert, W. Sansen, "Switched op-amp: an approach to realize full CMOS SC circuits at very low power supply voltages", *IEEE Journal of Solid-State Circuits*, vol. SC-29, n.8, August 1994, pp. 936-942.

[3] A. Baschirotto, R. Castello, "A 1V 1.8 MHz MOS switched-opamp SC filter with rail-to-rail output swing", *Proc. ISSCC Conference*, S.Francisco,1997, pp. 58-59.

[4] V. Peluso, P. Vancorenland, M. Stayaert, W. Sansen, "900 mV differential class AB OTA for switched op-amp applications", *Electronics Letters*, vol. 33 n. 17, 14 August 1997, pp. 1455-1456.

[5] G. Ferri, A. Costa, A. Baschirotto, "A 1.2V rail-to-rail switched buffer", *Proceedings ICECS*, Lisboa, Portugal, September 1998.

[6] G. Ferri, A.Baschirotto, "Low-voltage rail-to-rail switched buffer topologies", *International Journal of Circuit Theory and Applications*, vol.29, n.4, July 2001, pp.413-422.

[7] A.Gerosa, A.Novo, A.Neviani, "Low-power sensing and digitization of cardiac signals based on sigma-delta conversion", *Proc. ISPLED*, Rapallo, Sept.2000, pp.386-389.

[8] B. Ginetti, P. G. A. Jespers, A. Vandemeulebroecke, "A CMOS 13-b Cyclic RSD A/D Converter", *IEEE Journal of Solid-State Circuits,* Vol. 27, n.7, July 1992, pp. 957-964.

[9] M.Waltari, K. Halonen, "1-0Volt, 9-bit Pipelined CMOS ADC", *Proc. ESSCIRC*, Sept. 2000, pp. 360-363.

[10] B. Razavi, B. A. Wooley, "Design Technique for High-Speed, High-Resolution Comparators", *IEEE Journal of Solid-State Circuits*, vol. 27, n. 12, December 1992.

[11] J. Sauerbrey, D. Schmitt-Landsiedel, R. Thewes, "A 0.5 V, 1μW Successive Approximation ADC", *Proc. ESSCIRC*, Florence, Italy, 24th-26th September 2002.