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Subthreshold CMOS Circuits

While the implementation of the sum-product algorithm as an analog circuit may seem difficult, recall from section 4 that the marginalization steps consist entirely of multiplication and addition, hence the name of algorithm:

$$\sum_{\mathbf{x}} \left(f(\mathbf{x}) \prod_{y \in n(f) \setminus \{\mathbf{x}\}} \mu_{h \rightarrow \mathbf{x}}(y) \right)$$

This type of calculation maps naturally into analog circuitry if we are provided the correct building blocks.

Addition of currents in analog circuits is particularly elegant. Kirchhoff's current law states the sum of currents into a node is zero, and so a current adder is simply a short of one wire to another. On the other hand, building analog CMOS circuits that perform multiplication is difficult. In the normal operating regions of a MOS transistor, the saturation current increases as the square of its gate voltage, and quadratic functions do not lend themselves to multiplication.

Traditionally, multipliers are built by combining elements that respond exponentially and logarithmically to their inputs. In his multiplier circuit, Gilbert showed that bipolar transistors could be used as the exponential elements and logarithmic circuits could be formed from diode-connected transistors. This project uses MOS transistors in their subthreshold operating region to achieve the same type of exponential response.

Subthreshold MOS Transistors

In an MOS transistor, the amount of current flowing from source to drain is controlled by an electric field from an applied voltage at the transistor's gate. The electric field attracts charge carriers from either side of the channel at the source and drain, forming a thin conductive layer between them. A higher voltage and stronger electric field translates to more current flowing through the transistor.

In a semiconductor, there are two modes by which current can flow: diffusion and drift. Diffusion is the natural flow of particles from higher to lower concentration, and drift is the flow of particles subject to an applied force. In the subthreshold region of a MOS transistor, the flow of current from source to drain is due to diffusion [14]. Diffusion current in a MOS transistor is given by:

$$I = -WqD \frac{\delta N}{\delta z} \quad (5)$$

where W is the channel width, D is the diffusion constant of the carriers, N is their density, and z is the distance between source and drain. The density of the carriers decreases linearly along the channel, so $\delta N / \delta z$ can be simplified to $(N_d - N_s) / L$. N_s is the density of carriers at the source, and N_d is their density at the drain:

$$N_s = N_1 e^{\frac{-q\psi_s}{kT}} e^{\frac{qV_s}{kT}} \quad (6)$$

$$N_d = N_1 e^{\frac{-q\psi_s}{kT}} e^{\frac{qV_d}{kT}}. \quad (7)$$

We first replace N_d and N_s with their respective formulae in the following equation:

$$I = -WqD \frac{N_d - N_s}{L}$$

to get:

$$I = \frac{qW}{L} N_1 D e^{\frac{-q\psi_s}{kT}} \left(e^{\frac{qV_s}{kT}} - e^{\frac{qV_d}{kT}} \right), \quad (8)$$

where ψ_s is the surface potential at the source and along the channel. If we then assume that excursions are small around the operating point, we can replace ψ_s with κV_g . Collecting all of the pre-exponential constants into one term, I_0 , we have:

$$I = I_0 e^{\frac{-q\kappa V_g}{kT}} \left(e^{\frac{qV_s}{kT}} - e^{\frac{qV_d}{kT}} \right), \quad (9)$$

which correctly describes subthreshold PMOS transistor operation. **In an NMOS transistor, an increase in gate voltage attracts rather than repels charge carriers, so the voltages are reversed:**

$$I = I_0 e^{\frac{q\kappa V_g}{kT}} \left(e^{\frac{-qV_s}{kT}} - e^{\frac{-qV_d}{kT}} \right). \quad (10)$$

To simplify the equation, we can assume the substrate is intrinsic and so no charge from ionized donors or acceptors in the substrate reduces the effectiveness of an applied electric field at the gate. κ is the term that accounts for the differences in surface potential along the channel from V_g , so we eliminate it.

Because kT/q is a voltage that only changes with temperature, we replace it with a single variable, V_T :

$$I = I_0 e^{\frac{V_g}{V_T}} \left(e^{\frac{V_s}{V_T}} - e^{\frac{V_d}{V_T}} \right). \quad (11)$$

Another form of this equation, which is less accurate, but makes further algebraic manipulations possible, assumes that the transistor is in the saturation mode where changes in V_d do not have a strong effect on the current **flowing through the transistor. This region starts when** $|V_d - V_s| \geq 4kT/q \approx 100mV$. In this mode, the V_d term drops out and we have:

$$I = I_0 e^{\frac{V_g}{V_T}} e^{\frac{-V_s}{V_T}} = I_0 e^{\frac{V_g - V_s}{V_T}}, \quad (12)$$

which shows that we can model the transistor as having a simple exponential response when saturated and in the subthreshold region. This response is illustrated by figure 3.

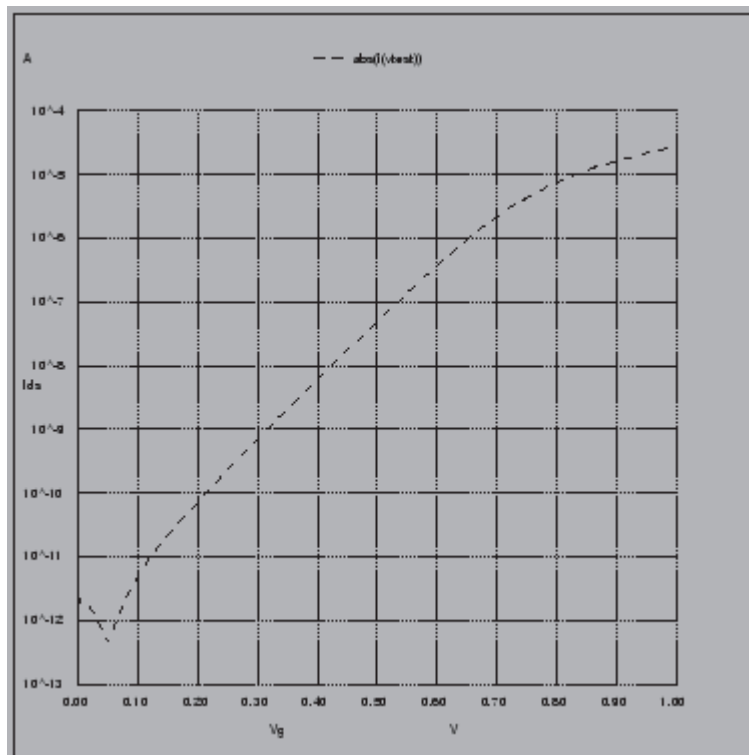


Figure 3: Drain current vs. gate voltage for a saturated subthreshold CMOS transistor.

Diode-Connected Transistors

As previously mentioned, a Gilbert multiplier is typically built of exponential and logarithmic components, and the **logarithmic component is typically a diode-connected bipolar transistor**. By solving equation [12](#) for V_g , we see that a saturated diode-connected subthreshold CMOS transistor does takes the logarithm of its input current:

$$V_g = V_T \ln \left(\frac{I}{I_0} \right) + V_s. \quad (13)$$

For typical processes, I_0 is high enough that even for very small drain currents, the voltage at the gate of the transistor will be about 0.4V [14]. This ensures that a diode-connected transistor is always saturated and the equation above will be valid for all useful subthreshold values. A plot of this logarithmic behavior is given in figure 4.

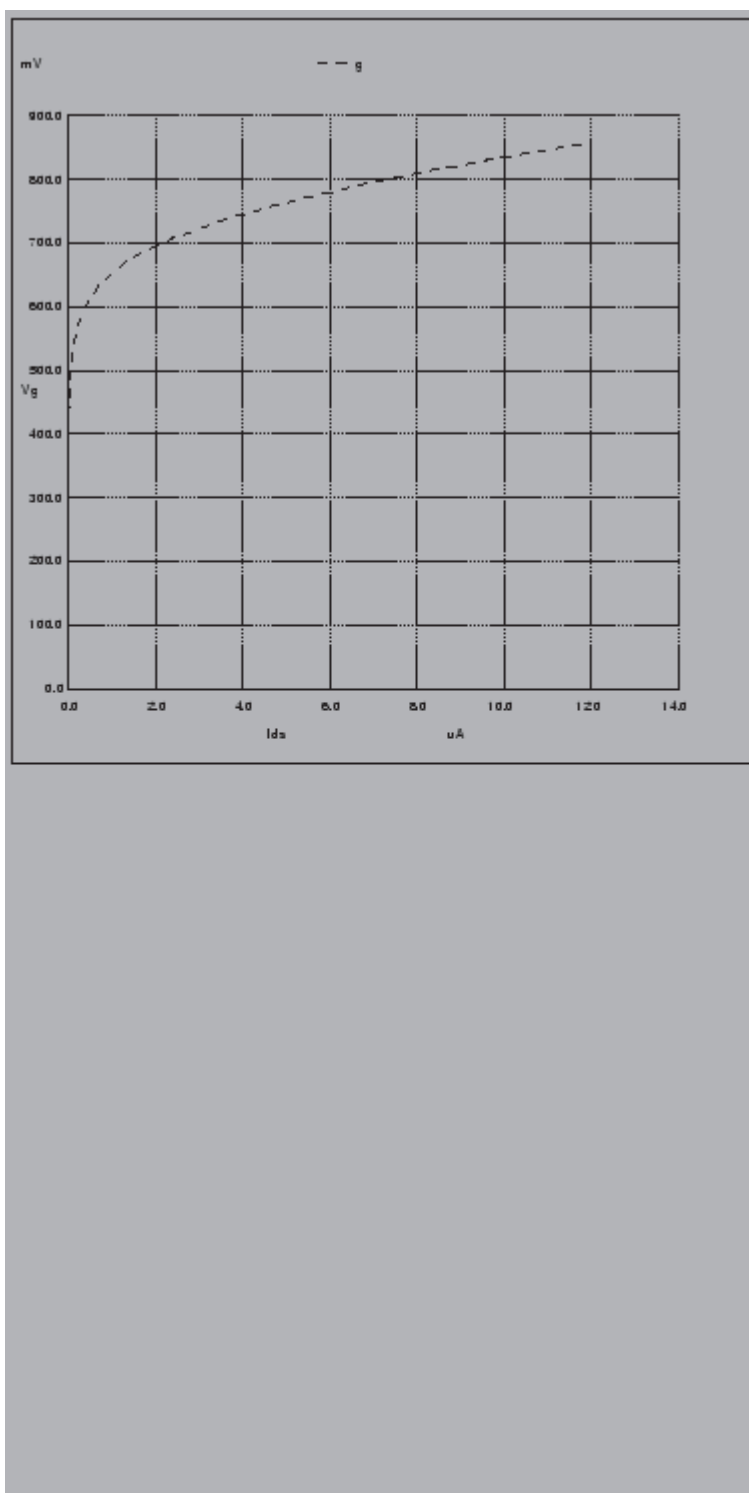


Figure 4: Gate voltage vs. drain current for a diode-connected transistor.