the table is the weak-inversion drain current where I_D is exponentially proportional to $V_{GS}-V_T$. Weak-inversion operation occurs at sufficiently low effective gate–source voltages, $V_{EFF}=V_{GS}-V_T$, where $V_{EFF}<-72\,\text{mV}$ $(-2\cdot nU_T)$. The second expression in the table is the strong-inversion drain current where I_D is proportional to the square of $V_{GS}-V_T$. Strong-inversion operation occurs at sufficiently high effective gate–source voltages where $V_{EFF}>225\,\text{mV}$ $(6.24\cdot nU_T)$. The boundaries between weak and strong inversion, discussed further in Section 3.7.2.4, assume operation at inversion coefficients of 0.1 and 10, respectively, a substrate factor $n=1.4$, and a thermal voltage $U_T=25.9\,\text{mV}$ for a typical bulk CMOS process at room temperature ($T=300\,\text{K}$). The third expression in the table is a continuous expression for drain current interpolated from weak through strong inversion. The reduction in drain current due to velocity saturation and VFMR, introduced in Section 2.4.3, is not included in the drain current expressions but will be considered later in Section 3.7.1.

The substrate factor, n, appears in the weak, strong, and continuous weak through strong-inversion expressions of drain current in Table 3.6, illustrating its importance in all regions of MOS operation. As introduced in Section 2.4.1, it represents a loss of coupling efficiency between the gate and channel caused by the substrate or body, which acts as a back gate.

In weak inversion, n is related to the capacitive voltage division between the gate voltage and silicon surface potential resulting from the gate-oxide, C'_{OX}, depletion, C'_{DEP}, and interface-state, C'_{INT}, capacitances as introduced in Equation 2.6. In weak inversion, the surface potential tracks the gate voltage with a slope of $1/n$ [15, p.75]. Normally, the interface-state capacitance is negligible such that n is governed by substrate effects. However, as described later in Section 3.5.1 and in Figure 3.4, n can increase significantly at low temperatures below 200 K (−73 °C) due, most likely, to significant increases in interface-state capacitance. In weak inversion, n is commonly recognized as the weak-inversion slope factor appearing in the weak-inversion drain current in Table 3.6 and in the subthreshold or weak-inversion swing voltage, $S=2.303\cdot nU_T$, introduced in Equation 2.7. The weak-inversion swing voltage, which is the required gate–source voltage increase for a factor-of-10 increase in drain current, is approximately 90 mV/decade for $n=1.5$ and $U_T=25.9\,\text{mV}$ at $T=300\,\text{K}$.

While most easily recognized in the expression of weak-inversion drain current, n causes a reduction in strong-inversion drain current through division by n as illustrated in the strong-inversion drain current expression of Table 3.6. As described for strong-inversion operation in the EKV MOS model, the slope of the channel, inversion-charge, pinch-off voltage, V_P, with increasing gate voltage is equal to $1/n$ [13]. An n value above unity corresponds to body or substrate effect along the channel that raises the local threshold voltage, reducing the source-referenced, inversion-charge, pinch-off voltage to $V_P=(V_{GS}-V_T)/n$ compared to $V_P=V_{GS}-V_T$ present if there were no substrate effects. As a result, the strong-inversion drain current is then divided by n.

n is approximated in Table 3.6 from the EKV MOS model for operation in strong inversion where a source-referenced, inversion-charge, pinch-off voltage of $V_P=(V_{GS}-V_T)/n$ and constant, "pinned," strong-inversion, silicon surface potential of $\phi_0=2\phi_F+4U_T$ are assumed [13, 14]. As described later in Section 3.8.3.1, the approximations for n will be used in all regions of operation because the silicon surface potential is effectively reduced for negative values of $V_{GS}-V_T$ appearing in weak and moderate inversion. Like the continuous drain current expression given in the table, n is modified using the source as the reference terminal.

As seen in Table 3.6, n is a function of the gate–source, V_{GS}, source–body, V_{SB}, and zero-V_{SB} threshold, V_{TO}, voltages, where the body-referenced $V_P=(V_{GS}-V_{TO}+V_{SB})/n$. Alternatively, as shown in the table, $V_P=(V_{GS}-V_T)/n+V_{SB}$ since the threshold voltage, $V_T\approx V_{TO}+(n-1)\cdot V_{SB}$, approximates the threshold-voltage increase from V_{TO} due to non-zero V_{SB}. n is also a function of the body-effect factor, γ, the Fermi potential, $PHI=2\phi_F$,[5] and the thermal voltage, U_T. n increases with increasing γ, corresponding to increased substrate doping concentration and increased body or substrate effect. As a result, n can be as low as 1.1 for fully depleted (PD), silicon-on-insulator (SOI)

[5] Like the MOS drain current and terminal voltages described in Footnote 4, the Fermi potential, $PHI=2\phi_F$, is also taken positively for both nMOS and pMOS devices.