From Behzad Razavi: "Design of Analog CMOS Integrated Circuits"

pp.13..14
In weak inversion, n is approximately 1.4–1.5 for typical bulk CMOS processes, but can be as low as 1.1 [4] for fully depleted (FD) silicon-on-insulator (SOI) CMOS processes where there is little substrate effect. n drops slightly with increasing inversion level (increasing VEFF = VGS − VT) and is approximately 1.35 in moderate inversion and 1.3 in strong inversion for typical bulk CMOS processes.

From David M. Binkley: "Tradeoffs and Optimization in Analog CMOS Design"

p. 14
In weak inversion, n is the weak inversion slope factor that describes the degradation of exponential MOS drain current compared to bipolar transistor collector current where the equivalent value of n, the emitter injection efficiency, is very close to unity. Often the MOS weak inversion slope factor is expressed by the weak inversion or subthreshold swing given by

$$S = \ln(10) n U_T = 2.303 \cdot n U_T \quad \text{(mV/decade)} \quad (2.7)$$

This is the required increase in gate–source voltage for a factor-of-10 increase in drain current. The weak inversion swing is approximately 90 mV/decade for bulk CMOS processes at room temperature, assuming n = 1.5 and UT = 25.9 mV.

pp. 42..43 PROCESS PARAMETERS FOR EXAMPLE PROCESSES

Parameter	Description	nMOS	pMOS
n	Substrate factor (average moderate inversion value, Vsb=0)		
	0.5µm	1.4	1.35
	0.35µm, PD SOI	1.4	1.35
	0.18µm	1.35	1.35

pp. 89, 115 & 121
... the substrate factor, n, which has typical values of 1.4, 1.35, and 1.3 in weak, moderate, and strong inversion for typical bulk CMOS processes.