

Statistical OCV with Stage Based Derating

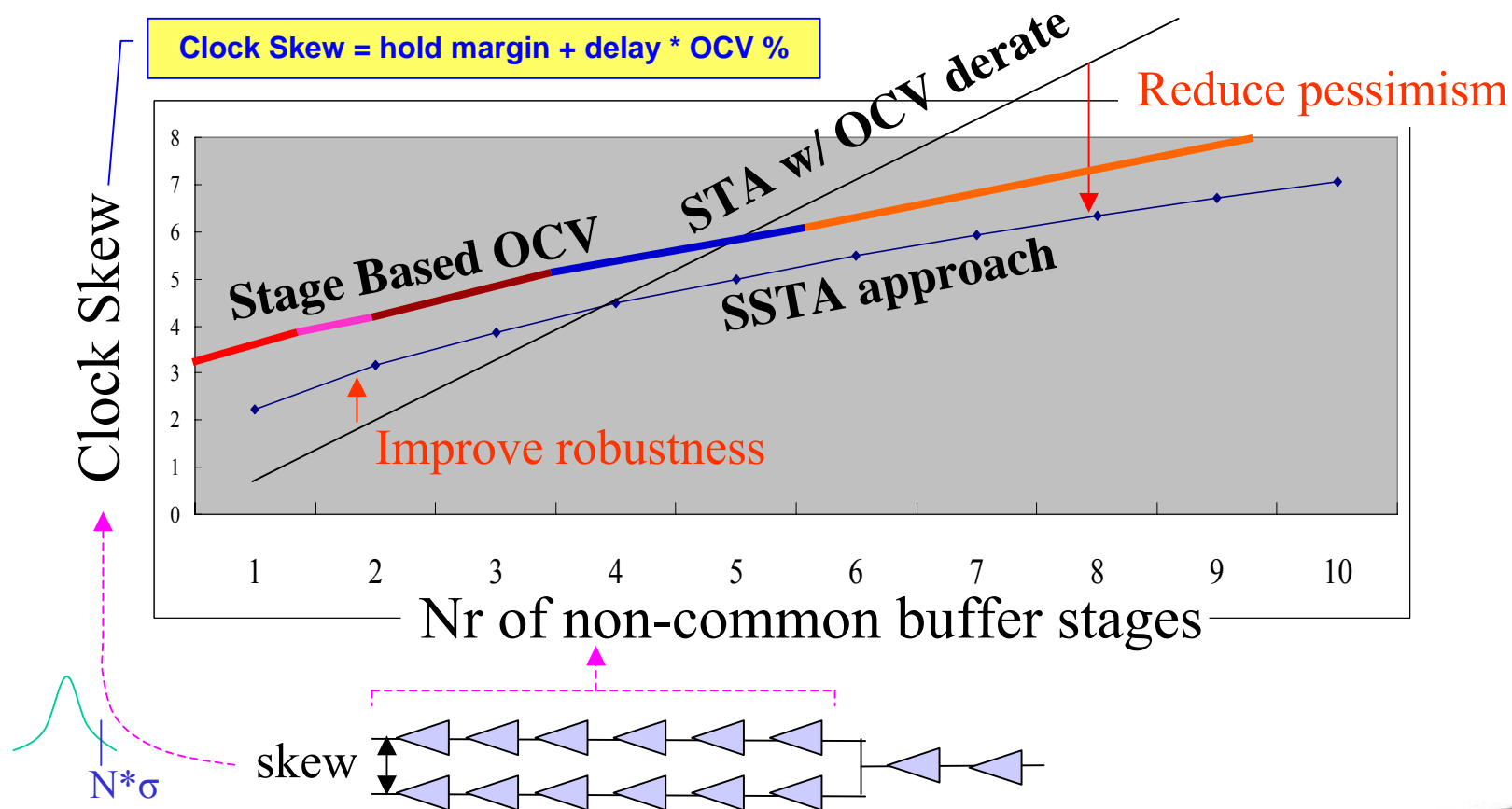
TSMC Reference Flow 9.0

Stage Based OCV Analysis Overview

- **Traditional On-Chip-Variation (OCV) timing analysis uses a constant de-rating factor and imposes unnecessary performance penalties on N45 and below nanometer designs included reduced performance, larger die sizes and longer design cycles.**
- **Stage Based OCV reduces pessimism setting and also increases robustness compared with traditional OCV.**
- **Use Stage Based OCV tuning table derived from Statistical Analysis with Monte Carlo spice to determine the stage based OCV number.**

Why Stage Based OCV ?

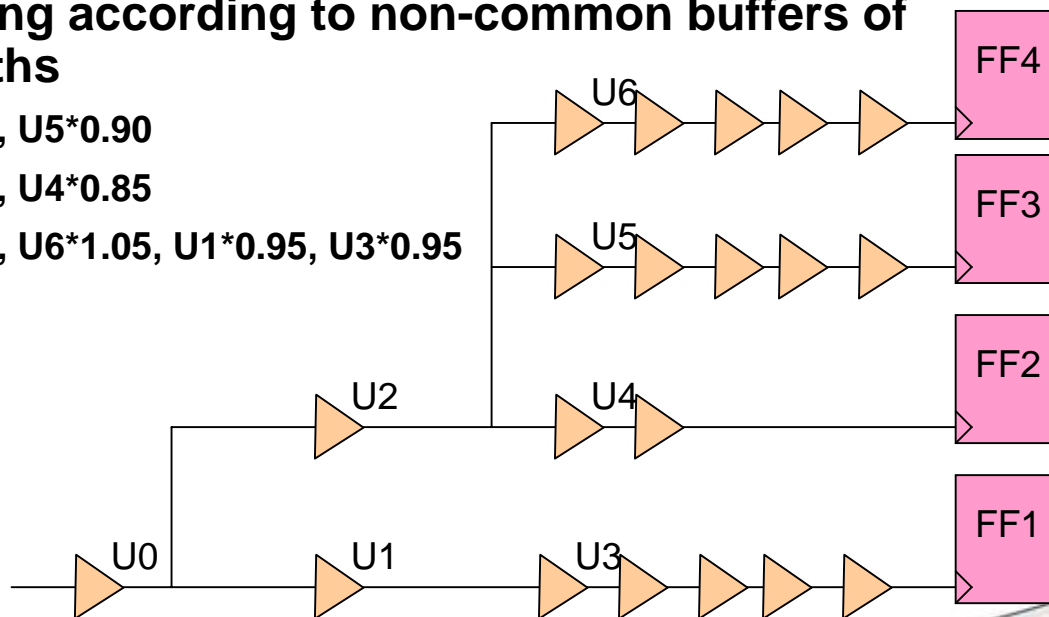
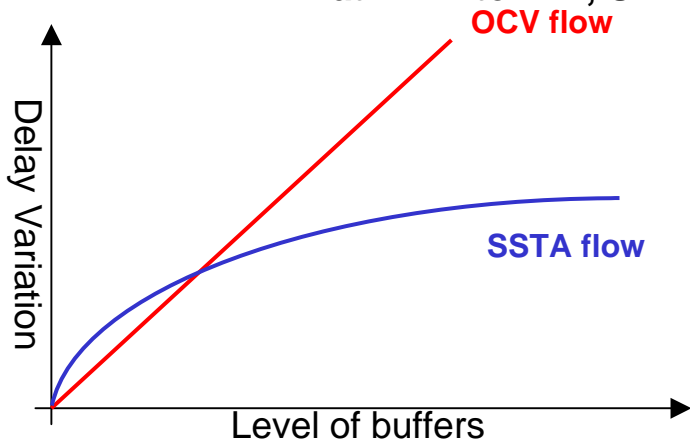
- Improve hold robustness with intra-die statistical analysis
- Reduce hold pessimism for long non-common clock paths



Stage-Base OCV Concept

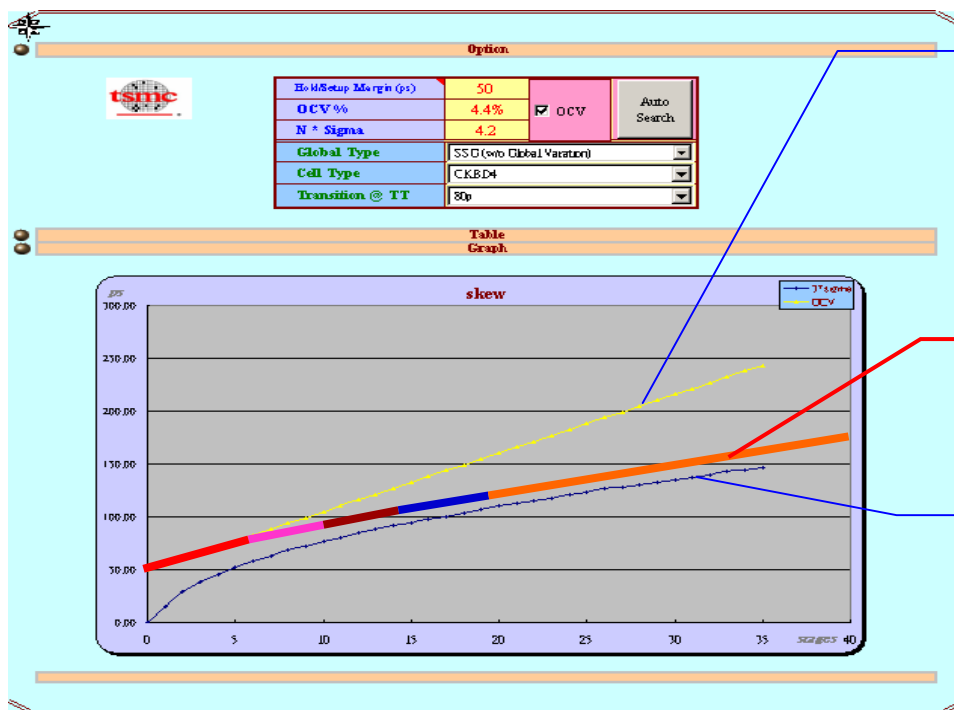
- OCV Table for different non-common buffers of clock tree
- For example :
 - Timing_derate 15% if $0 < \text{non-common buffers} \leq 2$
 - Timing_derate 10% if $2 < \text{non-common buffers} \leq 5$
 - Timing_derate 5% if $5 < \text{non-common buffers} \leq 10$
 - Timing_derate 2% if $10 < \text{non-common buffers}$
- Path based OCV derating according to non-common buffers of launch and capture paths

- Path FF4 to FF3, $U6 \cdot 1.10, U5 \cdot 0.90$
- Path FF4 to FF2, $U6 \cdot 1.10, U4 \cdot 0.85$
- Path FF4 to FF1, $U2 \cdot 1.05, U6 \cdot 1.05, U1 \cdot 0.95, U3 \cdot 0.95$



Example

- Assumptions :
 - 45GS/LP process
 - IR drop variation : 7~8% OCV on the top of stage based OCV within 3% VDD+VSS
 - 50ps hold margin (Clock jitter is not included)
 - Critical path number = 100; max. transition time (TT) = 80ps
 - Clock tree cell type : CKBD2~8

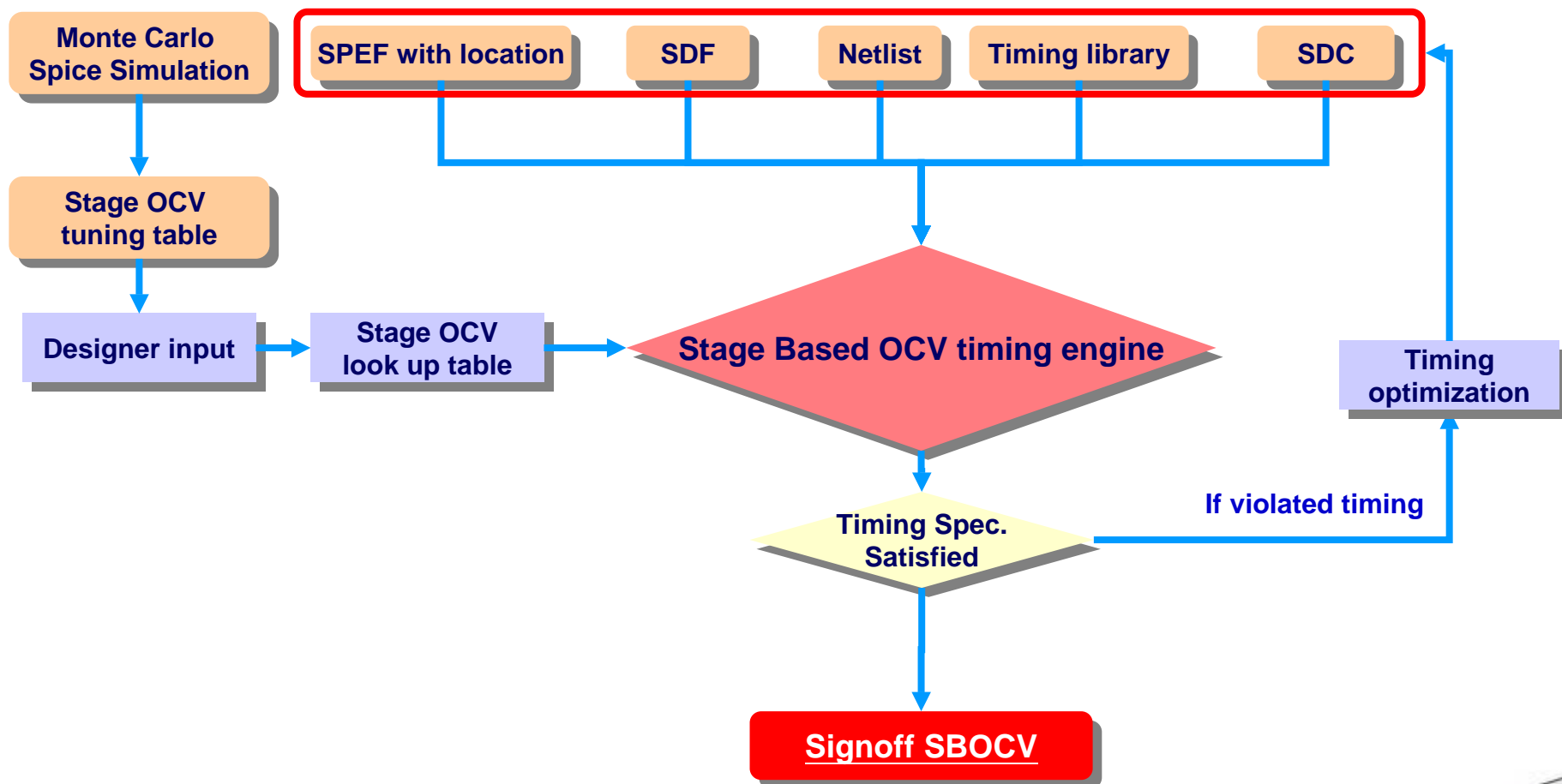


STA + OCV

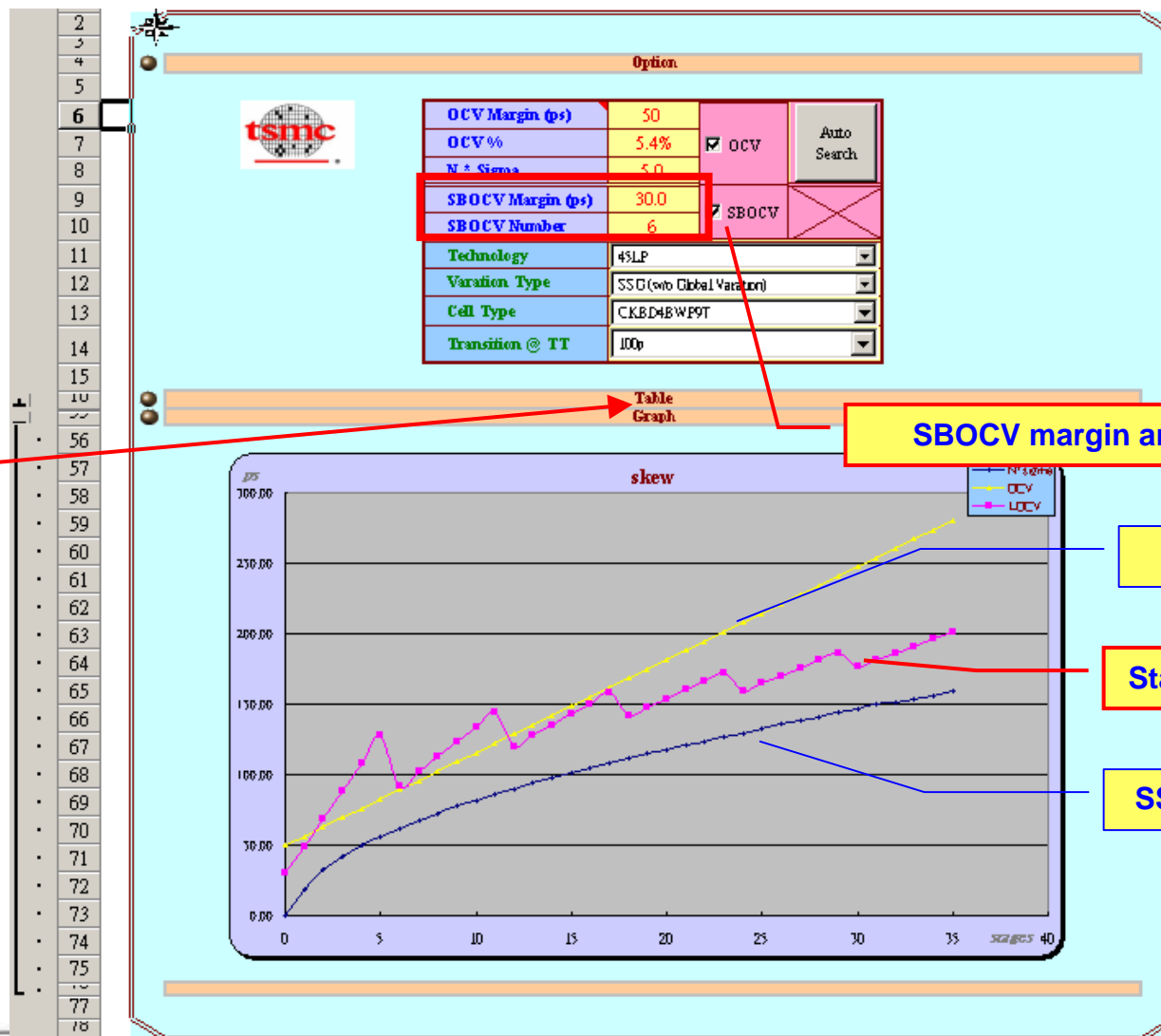
Stage-Base OCV

SSTA approach

Analysis Flow



Stage-Base OCV Tuning Table



Stage OCV
look up table

SBOCV margin and stage number

STA + OCV

Stage-Base OCV

SSTA approach

Stage-Base OCV Look Up Table

stages	mean	σ	$N \cdot \sigma$	$N \cdot \sigma / \text{Mean}$	SBOCV	User Defined SBOCV
1	112.35	3.66	18.29	16.28%	16.28%	16.28%
2	233.74	6.49	32.43	13.87%	16.28%	16.28%
3	355.23	8.43	42.16	11.87%	16.28%	16.28%
4	476.70	9.95	49.75	10.44%	16.28%	16.28%
5	598.20	11.26	56.30	9.41%	16.28%	16.28%
6	719.70	12.44	62.18	8.64%	8.64%	8.64%
7	841.22	13.54	67.71	8.05%	8.64%	8.64%
8	962.73	14.47	72.35	7.51%	8.64%	8.64%
9	1084.20	15.49	77.45	7.14%	8.64%	8.64%
10	1205.70	16.35	81.77	6.78%	8.64%	8.64%
11	1327.10	17.27	86.37	6.51%	8.64%	8.64%
12	1448.50	18.00	90.01	6.21%	6.21%	6.21%
13	1570.00	18.81	94.05	5.99%	6.21%	6.21%
14	1691.40	19.54	97.70	5.78%	6.21%	6.21%
15	1812.90	20.21	101.07	5.57%	6.21%	6.21%
16	1934.50	21.01	105.05	5.43%	6.21%	6.21%
17	2056.00	21.57	107.87	5.25%	6.21%	6.21%
18	2177.50	22.27	111.35	5.11%	5.11%	5.11%
19	2298.90	22.94	114.69	4.99%	5.11%	5.11%

Stage Based
OCV look up
table

Optional

User defined SBOCV

Based on the last page assumptions

Summary

- Statistical Analysis with Monte Carlo spice provides on-chip variation data that can be specific to each design depending on clock-buffers used and maximum input transition.
- Stage Based OCV reduces over pessimism and and increases design robustness.
- Synopsys Prime Time and Cadence ETS both support stage based OCV. Please refer to the follow Reference Flow 9.0 documents regarding detail EDA usage
 - Statistical OCV with stage based derating analysis – SOC Encounter
 - Statistical OCV with stage based derating analysis and optimization – Synopsys