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Designing a Multilayer PCB Stackup to Optimize Manufacturability, Reliability and Signal Integrity

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Abstract

As the speeds and complexity of logic and RF circuits have continued to climb, the importance of PCB stackup design in the overall design process has become more and more important. The common practice of leaving the vital PCB stackup design in the hands of PCB fabrication engineers carries with it significant hazards. It is often the case that the only criteria given to a fabricator is the overall number of layers, desired total thickness and expected impedance of the transmission lines. As will be seen in this paper, this method of arriving at a PCB stackup can result in a different PCB from every fabricator who quotes on the job as well as significant signal integrity risks.

This method of arriving at PCB stackups is akin to telling wire manufacturer the length and diameter of the suspension cables for the Golden Gate Bridge and leaving all of the strength and durability decisions in their hands. Clearly, this would not be seen as reasonable engineering.

This paper is intended to provide the attendee with all of the information necessary to arrive at a PCB stackup that makes the best trade-off between cost, materials choices, manufacturability and signal integrity requirements that results in repeatable results from multiple fabricators.

Author(s) Biography

Lee W. Ritchey is president of Speeding Edge, a leading signal integrity and PCB fabrication consulting company. He has been involved in or supervised the design and fabrication of more than 3000 high speed PCBs ranging from video game mother boards to supercomputer backplanes and daughter cards. He has taught a two day course in High Speed Design to more than 7000 engineers around the world and has authored two text books on the subject “Right The First Time, A Practical Handbook On High Speed PCB And System Design, Volumes 1 and 2”. He has also written numerous articles on PCB design and fabrication and is currently a regular columnist for Circuitree magazine. He has been instrumental in the development of the two leading PCB stackup design tools.

Mr. Ritchey has a BSEE degree from California State University at Sacramento with a specialty in microwave engineering. He has worked on programs ranging from the Apollo Mission to some of the largest supercomputers in the world.

DESIGNING A PCB STACKUP

PURPOSE

This document is intended to lead the reader through the process of designing a PCB stackup that meets the many demands it must satisfy. Information in this document is drawn from the experience gained designing more than 2000 PCB stackups for products as simple as a video game to the highest performance backplanes used in supercomputers and routers.

This document has been created because the practice which has worked in the past of allowing the fabricator to design a PCB stackup no longer works. Speeds have increased to the point where signal integrity and power delivery considerations make it necessary to employ far more discipline in the choice of materials and arrangement of the layers in the stackup- both of which are outside the skill-set of virtually all PCB fabricators. A common part of the vendor selection process has been to submit each design for a quote to several fabricators and make the choice based on price only. This is very often a fatal method of vendor selection because the lowest bidder often takes shortcuts in order to achieve the lowest price and/or may not possess the skills necessary to manufacture quality PCBs of the given complexity.

Among the demands placed on stackup design are:

- Providing enough signal layers to allow successful routing of all signals to signal integrity rules.
- Creating copper thickness in planes and signal layers that meets the conductivity demands of signals and power and, at the same time, be reasonable to manufacture.
- Providing enough power and ground layers to meet the needs of the power delivery system.
- Specifying trace widths and dielectric thicknesses that allow impedance targets to be met.
- Insuring that the spacing between signal layers and their adjacent planes is thin enough to satisfy crosstalk needs.
- Specifying dielectric materials that are economical to manufacture and readily available.
- Avoiding the use of expensive techniques such as blind and buried vias and build up processing if possible.
- Providing for prototype manufacture in one factory or country and production manufacture in another factory or country.

Information needed to design a successful PCB stackup is scattered among many documents and specifications, many of which are not in the public domain. This document is intended to bring all of the necessary information into one document to improve the design process.

HOW A TYPICAL MULTILAYER PCB IS BUILT

In order to understand the choices that must be made when designing a PCB stackup, it is useful to review how a typical multilayer PCB is fabricated. Figure 1 is a diagram showing the components that make up a six-layer PCB. The manufacturing method shown in the figure is referred to as foil lamination. This refers to the fact that the two outer layers begin as sheets of foil copper with no images etched into them. This is the most cost effective way there is to manufacture a multilayer PCB and should be the objective of the stackup design process. There are other methods available, such as ”cap” lamination that forms the outer layers as part of a two-sided piece of laminate and “build up” processing that involves blind and buried vias. These choices always result in more expensive PCBs and should be considered only as a last resort.

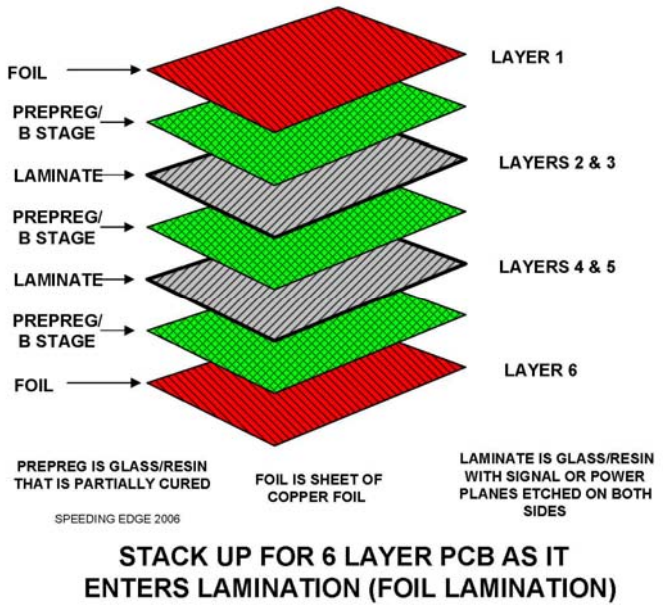

Figure 1. A Typical Six-Layer PCB Stackup Using Foil Lamination

It should be noted that PCB layers are built in pairs. Therefore, PCBs normally have an even number of layers. As a result, when additional layers are needed they will be added one pair at a time along with an additional prepreg layer. Designing a stackup with an odd number of layers when only one additional layer is needed does not result in a cheaper PCB than if a pair of layers is added. The reason for this is the fabricator will need to purchase a piece of laminate for the added layer that has copper foil on both sides. The copper foil that is not needed will be etched away when the foil side that is needed is etched.

As can be seen from Figure 1, three main components make up a multilayer PCB. These are:

- Sheets of laminate that have a sheet of copper foil bonded to each side which have the patterns for either signal layers or plane layers etched into the copper foils. These are often referred to as “details”. (Laminate is a combination of woven

glass cloth and a resin system such as epoxy or polyimide.) The thickness of the copper on each side of this laminate can vary from ½ ounce to 2 ounces. (Copper foil thickness is specified in ounces per square foot of surface area. 1 ounce is approximately 1.4 mil or 36 microns thick.)

- Sheets of uncured laminate called prepreg placed between the details and between details and the outer foil sheets. This prepreg is woven glass material coated with the same resin system that is used in the laminates. Unlike the laminates, the resin is only partially cured. During lamination heat will cause this resin to melt and flow into the voids in the adjacent copper layers, serving as the "glue" to bond the layers together and then cure it to the same rigid state as the resin in the laminate. After lamination prepreg is indistinguishable from laminate.

- Sheets of copper foil to form the outer layers. The reason the two outer layers are solid copper at this stage instead of etched with the outer layer patterns is to provide a path for the current required to plate copper into the holes drilled through the PCB for vias and component leads.

The task of the stackup designer is to select combinations of prepreg, laminate and foils that provide the desired electrical characteristics while satisfying cost and manufacturability goals.

ALTERNATIVE PCB FABRICATION METHODS

Figure 2 is an illustration of the "cap" lamination method of manufacturing a multilayer PCB. As can be seen, there are three pieces of laminate each with two conductor layers in this version of a six-layer PCB. The most obvious difference between this and foil lamination for this six-layer PCB is that only two pieces of laminate or details must be processed using foil lamination while three are required with cap lamination. This represents a cost increase over foil lamination. This was the method used to fabricate PCBs in the early days of multilayer PCB fabrication.

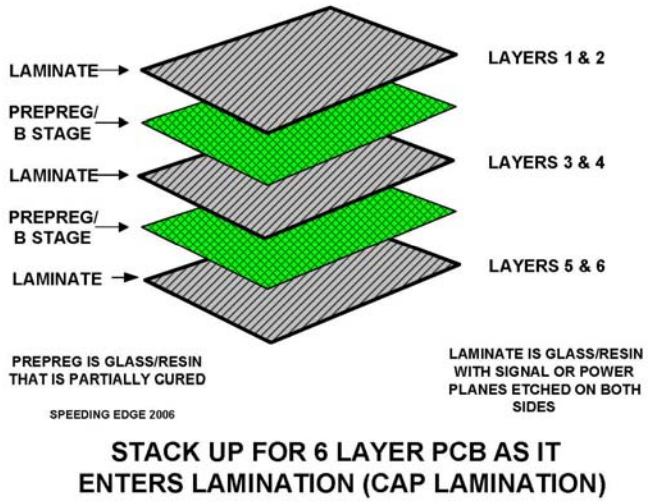

Figure 2. Typical Six-Layer PCB Using Cap Lamination

A third method for creating a multilayer PCB is by the use of buried and blind vias. In one version of this method, the internal n-2 layers are fabricated using either of the two methods shown above resulting in a complete sub-PCB with plated through holes running from layer 2 to layer n-1. Then, a piece of prepreg and a piece of foil are added to each side and the combination is laminated into a final PCB of n layers. After this second lamination step, holes are drilled through the entire stackup and plated. It is also common to drill blind vias from layer 1 to layer 2 and layer n to layer n-1 as well. It is easy to see that this method will result in a significantly more expensive PCB that takes longer to manufacture than either of the above choices. (In some cases PCBs designed to use buried vias can cost as much as twice what the same number of layers would cost using only through hole vias.)

CHOOSING A FABRICATOR AS A DESIGN PARTNER

One of the secrets to creating PCB stackups that are right the first time is to select a PCB fabricator to work with while trading off manufacturability of the final PCB stackup against signal integrity and cost goals. The right fabrication engineer can provide valuable insight into the manufacturability of proposed stackups as well as advice on how to improve a stackup. Clearly, for this to work the fabricator must have experience manufacturing PCBs of the complexity being designed. The design engineering department must have a clear, direct path to the engineering department of the fabricator. The classic method of allowing the purchasing or materials department to select fabricators based on cost does not work well with modern designs.

My first criterion in choosing fabricators is “Are they building PCBs like mine every day or will my design represent a stretch for them?” As always, selecting fabricators that demonstrate recent capability with the class of PCB being designed goes a long way toward insuring success on the first try. The best way to determine that there is a match is to conduct a vendor survey by visiting the factory and viewing the production line itself. Look for PCBs of your complexity being manufactured real time. (It is common for fabricators to display complex PCBs in conference rooms that do not represent the actual capability of the fabrication process as a way to impress customers.) This is the standard method used by companies such as Cisco to insure suppliers are matched to the need. These visits are conducted by a team of people that represent manufacturing, engineering and purchasing to make sure all areas are covered. Failing that, the next best way is by checking references to see how satisfied current customers are by asking for references that are willing to discuss their experiences with the supplier. If no references are forthcoming it is well to beware.

TYPES OF SIGNAL LAYERS

Figure 3 is a typical ten-layer PCB stackup. This example has three types of signal layers. They are: surface microstrip (L1 & L10), buried microstrip (L2 and L9) and off-center or dual stripline (L5 & L6).

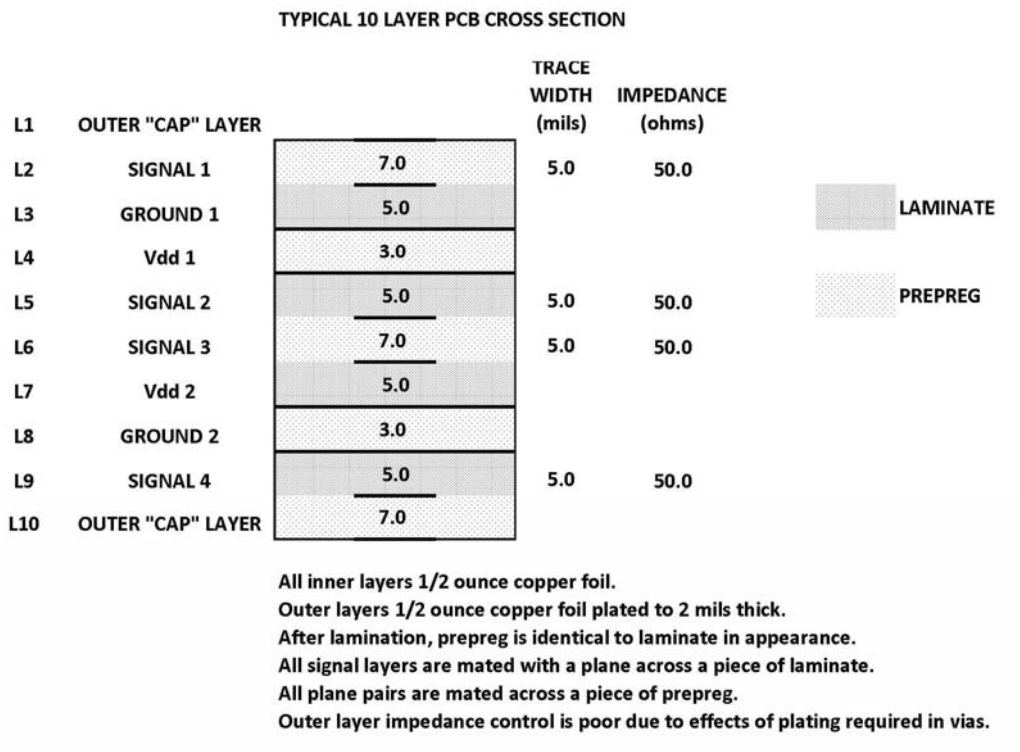

Figure 3. A Typical 10-Layer PCB Stackup

There is a fourth type of signal layer- centered or symmetrical stripline which is a single stripline layer centered between two planes. The reason that dual stripline is used more often than single stripline is that each time a single stripline layer is added to a stackup a plane must also be added to isolate signal layers from each other resulting in higher layer counts for a given number of signal layers. The method used to keep the two signal layers in the dual stripline configuration from interfering with each other (crosstalk) is to route signals on one layer horizontal and on the other vertical.

In this example, the two outer layers are not used for signals. The reason is impedance uniformity on these layers is difficult to control accurately due to the uneven plating of copper that often results when plating is done to plate copper in the holes that conduct current such as vias and power leads.

ALTERNATE WAYS TO STACK LAYERS

Figure 4 shows two different ways to arrange the layers in a ten-layer PCB. The short bars represent signal layers and the long bars represent planes. The stacking on the left appears to have two more signal layers than the one on the right due to the fact that the top and bottom layers on the right are not available for signals and this is true. The disadvantages of the stackup on the left are power-delivery related. Most high speed designs require plane capacitance to support fast switching edges. In order to create plane capacitance, pairs of planes must be close to each other (less than 4 mils, 100 microns). The stackup on the left has only one plane pair close together while the stackup on the right has two plane pairs.

A second benefit of the stackup on the right is that the plane pairs are separated by prepreg which can be made very thin, less than 3 mils, as shown in Figure 3. This is of significant value when designing a power delivery system.

A third benefit of the stackup on the right is that each signal layer is paired with a power plane across a piece of laminate. The benefit here is that during lamination, the thickness of the laminate does not change and this makes it possible to achieve tightly controlled impedances on the transmission lines. When a signal layer is mated with a plane across a piece of prepreg, impedance control is more difficult as the prepreg thickness can change significantly during the press cycle.

For all the reasons given above, the layer stacking on the right represents the best compromise between power delivery and impedance accuracy. If two more signal layers are needed, they would be added along with two more planes resulting in a 14-layer PCB. If four more signal layers are needed then four more signal and four more plane layers would be added resulting in an 18-layer PCB (Figure 6) and so on for 22 and 26 layers.

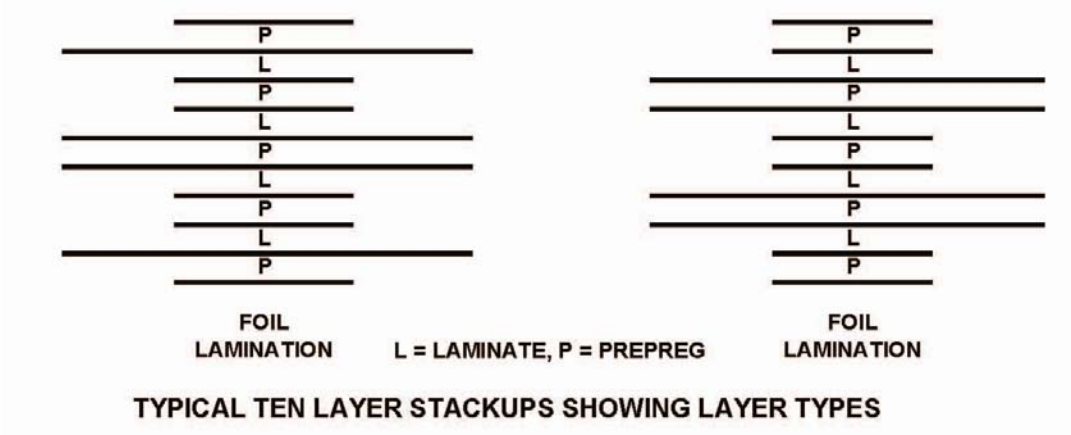

Figure 4. Two Ways to Arrange Plane and Signal Layers in a 10-Layer PCB

SELECTING AN IMPEDANCE

The starting point for most PCB stackup design is determining what impedance or impedances to use in each signal layer. A number of impedances have been used for controlled impedance PCBs. Among these are 62 or 65 ohms for PCI buses, 72 or 75 ohms for video signals, 50 ohms for ECL and high speed CMOS, 28 ohms for Rambus and an assortment of differential impedances for various differential signaling protocols.

Attempting to design stackups that accommodate more than one impedance value has proven to be difficult. A reasonable question to ask is whether or not multiple impedances are really necessary. The most common impedance found in multilayer PCBs is 50 ohms. It turns out that this impedance represents a happy medium between impedance value and ease of manufacture when more than two controlled impedance signal layers are needed. Therefore, it is worth examining the protocols that specify other

impedance values to see if they will operate successfully with a 50-ohm transmission line.

The most common PCB impedance is 50 ohms. This impedance is achieved on stripline layers with a trace width that is about the same as the dielectric thickness. In order to make a 62-ohm line for the PCI bus the trace width has to be made very narrow in stripline layers. Reference 1 explains how this impedance came into existence and demonstrates that the PCI bus works properly with 50-ohm transmission lines. A similar analysis will show that the Rambus protocol also works properly with 50-ohm transmission lines. (To make a 28-ohm line the trace width must be so wide that it will not fit between pins on a BGA.)

This leaves 72-ohm video and the various differential protocols. In almost all cases, the 72-ohm video requirement is to match 72-ohm coaxial cable bringing a signal onto a PCB or taking it off the PCB. Building a stackup that allows both 50 ohms and 72 ohms in the same signal layer is very difficult, if not impossible. Is that really necessary? I have found that if the IC using the video signal is located close to the edge of the PCB, as most are, a very short trace of 50 ohms is not going to significantly degrade the video signal. This can be easily validated using any good SI simulator.

The 100-ohm differential impedance requirement is an artifact of the need to provide two 50-ohm lines each parallel terminated in 50 ohms. (See Reference 2). From reference 2 it can be seen that the optimum way to route differential signals in a PCB is so that each member of a pair does not interact with the other. This is achieved by separating them from each other far enough so that one does not drive down the impedance of the other. When this is done, it is no longer necessary to specify differential impedance. As a result, all of the signals that need controlled impedance can be routed with the same impedance. The question is, what impedance?

From all of this, it can be seen that 50 ohms is a very good compromise impedance. It also happens to be in the “sweet spot” of the PCB fabrication process as well as of all the tools used to measure impedance and other characteristics of transmission lines. Therefore, it is wise to construct stackups that have a nominal impedance of 50 ohms.

In spite of what might be called out in some applications notes, every modern logic family fast enough to require controlled impedance and terminations is capable of driving a 50-ohm transmission line so there is no need to design complex stackups that require complex routing rules in order to make all of the nets fit into the space available in the signal layers.

MAKING ALL SIGNAL LAYERS THE SAME IMPEDANCE

Sometimes, in an attempt to provide more than one impedance on the same PCB, there is the temptation to make some layers of the stackup one impedance and others a different impedance. Examples of this are to make the PCI bus at 65 ohms and other signals 50 ohms. If this is done it is likely that the layers containing one impedance may be used

sparsely while layers containing the other impedance may be overcrowded. Therefore, it is wise to make all layers the same impedance so the task of routing is easy.

SELECTING LAMINATES

PCB material systems are defined by the resin systems used to make the laminate and prepreg. To a lesser extent the type of glass is also part of how a laminate system is differentiated from its competition. For the most part, a glass composition known as "E" glass is used.

Resin systems used to manufacture laminate include:

Epoxy-based systems (sometimes called FR4)
Polyimide
PPO- Polyphenylene Oxide
PPE- Polyphenylene Ester
BT- Bismalamine Triazine.
CE- Cyanate Ester
Phenolic cured epoxy
Cyanate Ester modified epoxy
Filled phenolic cured epoxy

For a detailed discussion of the merits and drawbacks of each of these resin systems, see Chapter 5 of reference 2 at the back of this document.

In the early years of PCB manufacture the resin system choices were epoxy and polyimide. Polyimide has very good high temperature characteristics but is very difficult to process and absorbs moisture to a level that causes it to fail leakage tests unless it is baked dry and then waterproofed. Epoxy-based systems are very easy to process and do not fail leakage tests, but don't tolerate the temperatures required to solder well. All of the other resin systems on the above list were developed in the hope of achieving the ease of processing of epoxy and withstanding the high temperatures associated with soldering and rework achieved with polyimide. The results have been mixed. The work horses of PCB fabrication are still variations of epoxy and polyimide.

In the United States, the resin systems of choice have been Isola Corporation's FR406 and FR408 and Nelco Corporation's N4000 series. When selecting a resin system for a project it is advisable to check with the probable fabricators and determine which laminate system in their production inventory works best. It is also advisable to choose a resin system that has an equivalent with both suppliers in order to avoid creating a single-source situation.

Most projects designed in the U.S. are destined for volume manufacture off shore in China, Taiwan, Japan or South Korea. The resins systems listed above are available in all of those countries. However, there are laminate manufacturers in all four countries that manufacture laminate locally. Among these are Mitsubishi, Panasonic, Matsushita and TUC. All of these suppliers have laminates that are equivalent to the main stream

laminates used in the U.S. When designing a stackup that will be prototyped in the U.S. and manufactured in volume off shore it is advisable to obtain the materials information from the offshore supplier and make sure the materials needed are available off shore.
Laminate systems are created in two parts. These are the cured laminate with copper foil on each side and partially cured laminate (prepreg) that will serve as the "glue" layers during lamination. When creating a stackup, it is necessary to get the specifications for both types of material in order to create a stackup that can be built with available materials. Figure 5 is this information for Isola's IS620i. Notice that each thickness of laminate is made with woven glass cloth and resin. The standard construction column specifies what type of glass cloth is used for each thickness. These numbers refer to a particular glass weave with precisely specified numbers of threads per inch and thread diameter. For more details on each glass style see Chapter 5 of reference 4.

Notice that the relative dielectric constant (e_r) varies in two ways. First, it varies with the ratio of glass to resin. Second, it varies with frequency. Therefore, it is necessary to specify both in order to achieve accurate impedance calculations. It is easy to see what e_r to use based on ratio of glass to resin. The big question is what frequency should be used for a given design. Virtually all modern designs will have components on them with 200 pSec or faster edges that must be properly controlled. It has been shown that the equivalent frequency for this rise time is approximately 2 GHz. Therefore, using the e_r value at 2-2.5 GHz will result in accurate impedance calculations.

Core Thickness	Standard Constructions	Resin Content	Dk at 100 MHz	Dk at 500 MHz	Dk at 1 GHz	Dk at 2.0 GHz	Dk at 5.0 GHz	Dk at 10.0 GHz
0.0020	1-106	70	3.30	3.29	3.29	3.28	3.24	3.24
0.0027	1-1080	60	3.52	3.51	3.51	3.51	3.47	3.47
0.0030	1-1080	63	3.45	3.45	3.44	3.44	3.40	3.40
0.0035	2-106	66	3.39	3.38	3.38	3.37	3.33	3.33
0.0035	1-2113	51	3.74	3.74	3.73	3.73	3.70	3.70
0.0040	2-106	70	3.30	3.29	3.29	3.28	3.24	3.24
0.0040	1-3070	49	3.80	3.79	3.79	3.78	3.75	3.75
0.0040	1 - 3313	55	3.64	3.64	3.63	3.63	3.59	3.59
0.0043	106/1080	62	3.48	3.47	3.47	3.46	3.42	3.42
0.0045	106/1080	63	3.45	3.45	3.44	3.44	3.40	3.40
0.0050	2-1080	57	3.59	3.59	3.58	3.58	3.54	3.54
0.0050	106/2113	55	3.64	3.64	3.63	3.63	3.59	3.59
0.0050	1-1652	43	3.96	3.95	3.93	3.94	3.92	3.92
0.0055	1-1652	47	3.85	3.84	3.84	3.84	3.81	3.81
0.0060	1080/2113	54	3.67	3.66	3.66	3.65	3.62	3.62
0.0060	106/ 1080	70	3.30	3.29	3.29	3.28	3.24	3.24
0.0065	1080/2113	57	3.59	3.59	3.58	3.58	3.54	3.54
0.0070	1080/2116	58	3.57	3.56	3.56	3.55	3.52	3.52
0.0070	2-2113	52	3.72	3.72	3.71	3.70	3.67	3.67
0.0075	2 - 3313	52	3.72	3.72	3.71	3.70	3.67	3.67
0.0080	2-3070	49	3.80	3.79	3.79	3.78	3.75	3.75
0.0100	2-1652	43	3.96	3.95	3.93	3.94	3.92	3.92
0.0100	3-1080	66	3.39	3.38	3.38	3.37	3.33	3.33
0.0100	2-2116	54	3.67	3.66	3.66	3.65	3.62	3.62
0.0120	2-2113/ 1652	48	3.82	3.82	3.81	3.81	3.78	3.78
0.0140	2-2116/1652	47	3.85	3.84	3.84	3.84	3.81	3.81
0.0160	3-1652	46	3.88	3.87	3.87	3.86	3.83	3.83
0.0180	2-3070/2-1652	46	3.88	3.87	3.87	3.86	3.83	3.83
0.0210	2-2116/2-1652	50	3.77	3.76	3.76	3.76	3.72	3.72

ISOLA IS 620I LAMINATE INFORMATION

Prepreg	Resin Content	Thickness (in)	Dk at 100 MHz	Dk at 500 MHz	Dk at 1 GHz	Dk at 2.0 GHz	Dk at 5.0 GHz	Dk at 10.0 GHz
106	75	0.0025	3.20	3.19	3.19	3.18	3.14	3.14
1080	65	0.0033	3.41	3.40	3.40	3.39	3.35	3.35
2113	58	0.0042	3.57	3.56	3.56	3.55	3.52	3.52
3313	54	0.0036	3.67	3.66	3.66	3.65	3.62	3.62
3070	55	0.0046	3.64	3.64	3.63	3.63	3.59	3.59
2116	55	0.0052	3.64	3.64	3.63	3.63	3.59	3.59
1652	51	0.0061	3.74	3.74	3.73	3.73	3.70	3.70

Prepreg	Resin Content	Thickness (in)	Df at 100 MHz	Df at 500 MHz	Df at 1 GHz	Df at 2.0 GHz	Df at 5.0 GHz	Df at 10.0 GHz
106	75	0.0025	0.0046	0.0050	0.0056	0.0058	0.0066	0.0073
1080	65	0.0033	0.0049	0.0052	0.0057	0.0059	0.0066	0.0072
2113	58	0.0042	0.0051	0.0054	0.0058	0.0060	0.0066	0.0071
3313	54	0.0036	0.0052	0.0055	0.0059	0.0060	0.0066	0.0071
3070	55	0.0046	0.0051	0.0055	0.0059	0.0060	0.0066	0.0071
2116	55	0.0052	0.0051	0.0055	0.0059	0.0060	0.0066	0.0071
1652	51	0.0061	0.0053	0.0055	0.0059	0.0060	0.0066	0.0070

ISOLA IS 620I PREPREG INFORMATION Courtesy of Isola Corporation

Figure 5. Typical Laminate Material Information

As can be seen in the above tables, there is a wide variety of glass styles used to manufacture laminate and prepreg. Prior to the advent of multigigabit differential signaling protocols, the glass style had little effect on signal quality. Since then, it has been shown that certain glass weaves can result in differential skew and excessive jitter in differential signal paths operating at or above 2.4 Gb/S. Reference 5 discusses this problem. It has since been shown that three weaves which exhibit this problem are 106, 1080 and 7628. Avoiding the use of these weaves in a high speed design obviates this problem. 3313 has been shown to be the most uniform weave of all those listed. For this reason, I use this weave between all my signal layers and their nearest planes.

As mentioned earlier, all of the common laminates use a glass known as “E” glass formulated to spin well and allow good adherence of resin to it. This glass happens to have a relatively high loss tangent. There is an alternate glass referred to as “S” glass that has a lower loss tangent. At least one laminate supplier, Nelco, uses this glass to create a low loss laminate known as N4000-13SI. This material does have a low loss, but at the expense of creating a single-sourced PCB design. The Isola IS620i shown above has proved to be a drop-in replacement for N4000-13SI if the need for lower loss laminate is encountered resulting in the equivalent of dual sourcing.

CONSIDERATIONS WHEN SELECTING A LAMINATE SYSTEM

There are a number of properties of laminates that must be taken into account when selecting a laminate system. Among these are:

- Does the PCB require lead free assembly?
- Does the PCB require a high Tg (ability to withstand high temperatures)
- Does the design require a low loss laminate?
- Can the program tolerate a single-source laminate?
- Will production volumes be manufactured in a different shop or country than the prototypes?

When most of these conditions must be met, many of the laminate types listed above will be eliminated from consideration.

OBTAINING LAMINATE INFORMATION

In order to properly design a PCB stackup it is necessary to obtain laminate information of the quality shown in Figure 5. There are two places to get this information. These are the fabricator and the laminate manufacturer. My first choice is to ask the fabricator for this data. Often, the engineering departments of fabricators do not have it. This is a sign that the fabricator is not up to the skill level required to successfully participate in designs of this complexity.

In the event the fabricator does not possess this information, the second choice is to contact the materials manufacturer directly. Laminate manufacturers accustomed to supplying materials to the high performance market will have their materials characterized in this manner and will openly share the data. There are laminate manufacturers who do not have this data. They have been supplying materials to the "low performance" market and should be avoided.

HOW THIN SHOULD LAMINATE AND PREPREG BE TO INSURE SUCCESSFUL MANUFACTURE?

As can be seen in Figure 5, laminate can be purchased with many different thicknesses, the thinnest being 2 mils or 51 microns for this material. Prepreg is available as thin as 2.5 mils or 63.5 microns. There are two considerations when deciding how thin either of these should be. The first consideration is minimum breakdown voltage between circuits of different polarity. Virtually all laminates based on epoxy or phenolic have breakdown voltages of at least 1000 volts per mil of thickness. In almost all products that contain logic circuits, the breakdown voltage requirement is 1500 Volts DC or less. If this is the specification to be met, all of the laminates listed in Table 5 can be used.

The second consideration is associated with prepreg and the fact that its thickness decreases during lamination due to the fact that some of the resin in the prepreg will flow into the voids in the adjacent signal and power layers. As this takes place the copper features in the adjacent plane and signal layers will be pressed into the resin and glass of the prepreg diminishing the final thickness to such an extent that shorts may result if the original thickness is not adequate. From experience I have found that the starting thickness for prepreg must be at least 3 mils (76 microns) to prevent this type of failure. Some fabricators have learned by experience that a minimum of two plies of the 106 prepreg are needed to guarantee short free PCBs. I have found that a single ply of 2113 works very well between adjacent plane layers that are intended to create interplane capacitance for the power delivery system (PDS). Accounting for the thickness decrease in the prepreg during lamination will be discussed later in this document.

A caution about 2 mil (51 micron) laminate: Sanmina has a series of patents for a material called ZBC© which is 2 mils thick intended to create interplane capacitance for the PDS. When stackups are created with planes separated by 2 mils that don't specifically call out ZBC©, there is a potential for legal proceedings initiated by Sanmina for violating their patents. In fact, the patents have been shown to be invalid. (See

reference 6 in the back of this document.) My solution to this problem is to design stackups that have prepreg between plane pairs, thus avoiding the use of 2 mil laminates altogether.

LAMINATE GLASS WEAVE STYLES

In Figure 5 there is a column labeled "standard construction". The numbers in this column refer to particular styles of woven glass cloth. Pictures of these glass cloth styles are shown on Page 109 in Reference 4 of this document. It has been shown that certain types of glass weave have an adverse effect on high data rate differential signals. The degradation takes the form of differential skew and is described in References 2 and 5 at the back of this document. When stackups are being designed for data rates of 2.4 Gb/S and higher it is imperative that these glass styles be avoided next to signal layers. The three glass styles that have been shown to cause this kind of problem are 106, 1080 and 7628. Two new glass weaves, 1067 and 1086 are "flat weaves" that replace 106 and 1080, respectively. These do not cause skew problems.

SELECTING THE PROPER COPPER FOIL THICKNESS

Copper foils are used as the conductive layers for a PCB. Virtually all copper foil used for this purpose is manufactured by a plating process rather than by rolling out copper as is done for aluminum foil. The reason for this is superior electrical characteristics as well as better ductility. Foils are produced in a variety of thicknesses. The primary thicknesses are 0.5 ounce, 1 ounce and 2 ounces. 1 ounce is equivalent to 1.4 mils (35.6 microns) thick. (This odd method of specifying foil thickness has its origins in the gold leaf business where thickness was specified by the number of ounces of metal spread out over one square foot of area.) Due to process variations the nominal thicknesses when finally used in a PCB are 0.5 mils, 1.2 mils and 2.6 mils, respectively.

Copper foils are used for two purposes in a PCB. One is to form plane layers and the other is to form signal layers. The stackup designer must balance foil thickness such that the copper is thick enough to perform properly as a conductor on the one hand and thin enough to allow accurate etching of features such as traces and plane clearances on the other.

When selecting foils for signal layers, it is desirable to select as thin a foil as possible in order to optimize accurate etching of traces and thick enough to form good signal conductors. Figure 6 is a plot of trace resistance vs. trace width for various foil thicknesses. This chart can be used to calculate trace cross section required to conduct DC current for traces used for connecting power to loads.

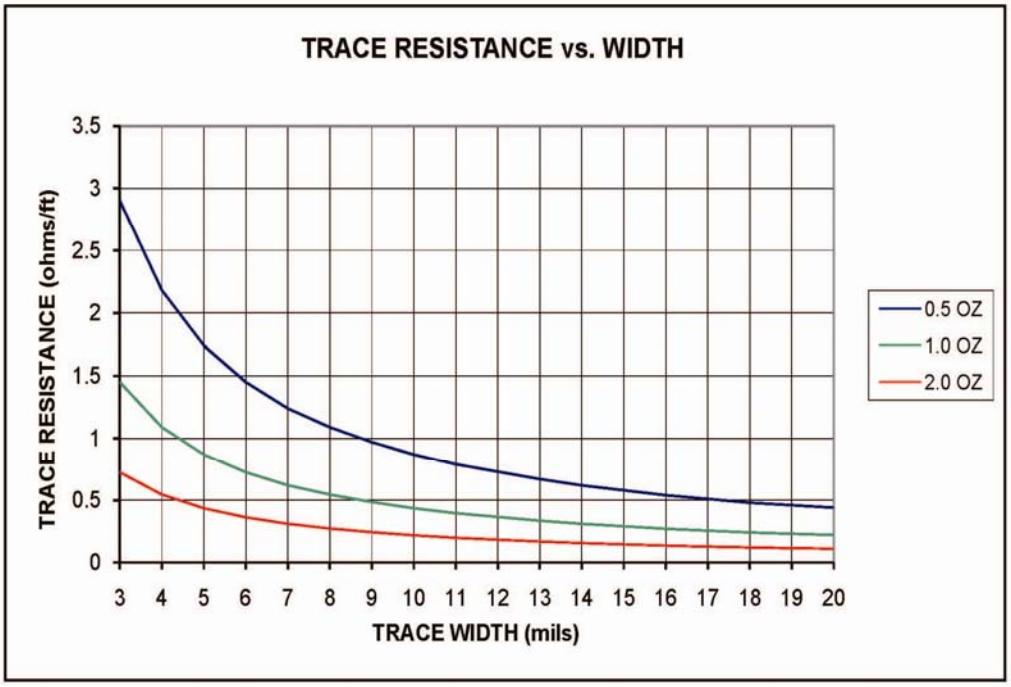

Figure 6. Trace Resistance vs. Foil Thickness and Width

Virtually all transmission lines operate at frequencies where skin effect losses determine how thick the copper in a trace needs to be. Figure 7 is a plot of skin depth versus frequency. Skin effect loss is defined as the increase in apparent trace resistance as frequency increases due to the fact that the current does not flow throughout the entire conductor but flows only near the surface. A complete treatment of this phenomenon is contained in several books on microwaves and RF. Skin depth is defined as the depth at which 67% of the current flows. Below this depth only 33% of the current is flowing and at twice this depth 90% of the current is flowing.

From Figure 7 it can be seen that at 100 MHz skin depth is approximately 0.25 mils or 6 microns and at 1 GHz it is approximately 0.075 mils or about 1.8 microns. Since nearly all modern logic has rise times less than 200 pSec which has an equivalent frequency on the order of 2 GHz, it is easy to see that trace thickness does not need to be more than half ounce copper or 0.6 mils (15.2 microns) to be thick enough so that skin effect loss dominates over bulk resistance of the trace. So it does not improve signal integrity to use copper thicker than 0.5 ounces in signal layers.

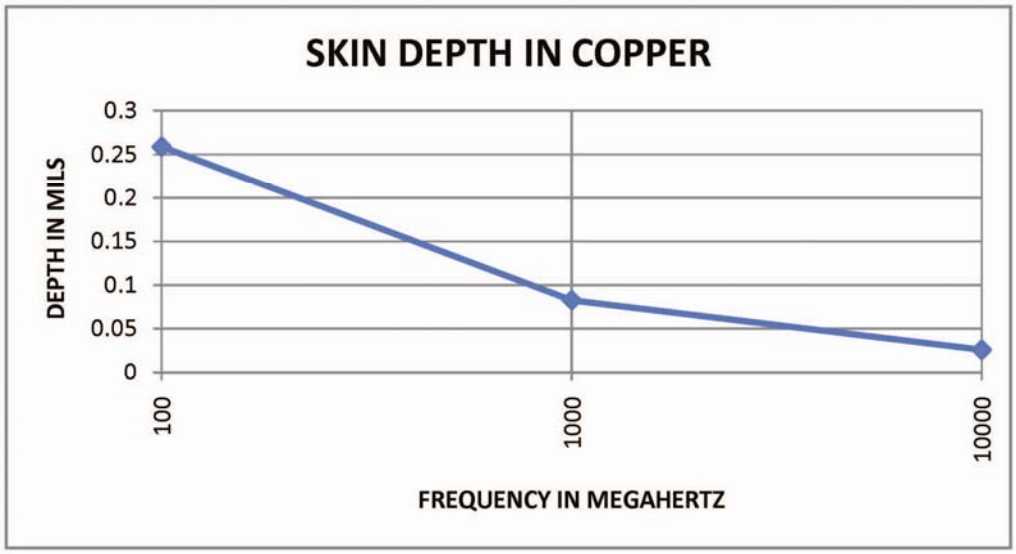

Figure 7. Skin Depth vs. Frequency

Designing stackups using 0.5 ounce copper in the signal layers has the benefit that trace width accuracy is improved significantly which results in more precise impedance control because etching can be done with more precision than with thicker copper foils. Trace width control on inner layers using ½ ounce copper can be done to an accuracy of ±0.5 mils (12.7 microns).

For the reasons described above, I have been designing PCB stackups using ½ ounce copper signal layers for the last ten or more years with excellent results.

Selecting foil thickness for power and ground layers is a balancing act between providing enough copper to conduct the currents in the PDS and optimizing manufacturability. Chapter 33 of reference 3 in the back of this document describes how to calculate voltage drops in power and ground planes as a method of determining minimum copper thickness for planes based on expected current flows.

It is likely that planes will be paired back to back with signal layers across pieces of laminate. Both sides of these pieces of laminate are etched at the same time during the manufacturing process. If the thickness of the copper on the two sides is not the same, it will be difficult to accurately form features on both sides. For example, if a plane layer is one ounce copper paired with a signal layer of ½ ounce copper across a piece of laminate, etching long enough to properly form the features in the plane layer will usually result in over etching the signal layer, resulting in impedance errors. Yes, there are fabricators that claim they have the ability to etch the two sides accurately because their etching equipment sprays etchant on the two sides at different rates. My experience has been that the level of control is not adequate to form features on both sides. The result has been impedance errors.

In order to guarantee good process control and impedance accuracy, it is advisable to design stackups with plane layers that are the same thickness as the signal layers.

With modern point of load regulators near their loads, it is reasonable to use ½ ounce plane layers in almost all cases.

CALCULATING IMPEDANCE

There are several ways to calculate the impedance of a PCB trace. Among these are various equations that have been developed to allow calculation using simple math and a fixed set of dimensions, as well as a variety of software tools that use Maxwell's Equations to precisely calculate impedance for any trace shape that can be imagined. These software tools are called field solvers and are often an integral part of a signal integrity tool such as Hyperlynx from Mentor Graphics or Allegro PCB Si from Cadence.

All of the equations used to calculate impedance were developed by constructing a large number of PCBs, measuring the impedance of their traces and then cross sectioning the PCBs to determine the dimensions that produced each impedance value. Curve fitting was then used to arrive at an equation that predicted the impedance. These equations are said to have a sweet spot where they are accurate. Outside this sweet spot results are uncertain.

Field solvers employ precise equations to calculate impedance no matter what the geometry of the transmission line. Figure 8 shows the results of calculating the impedance of surface microstrip, buried microstrip and stripline transmission lines using equations (the square curves) vs. the results using field solvers (the diamond curves).

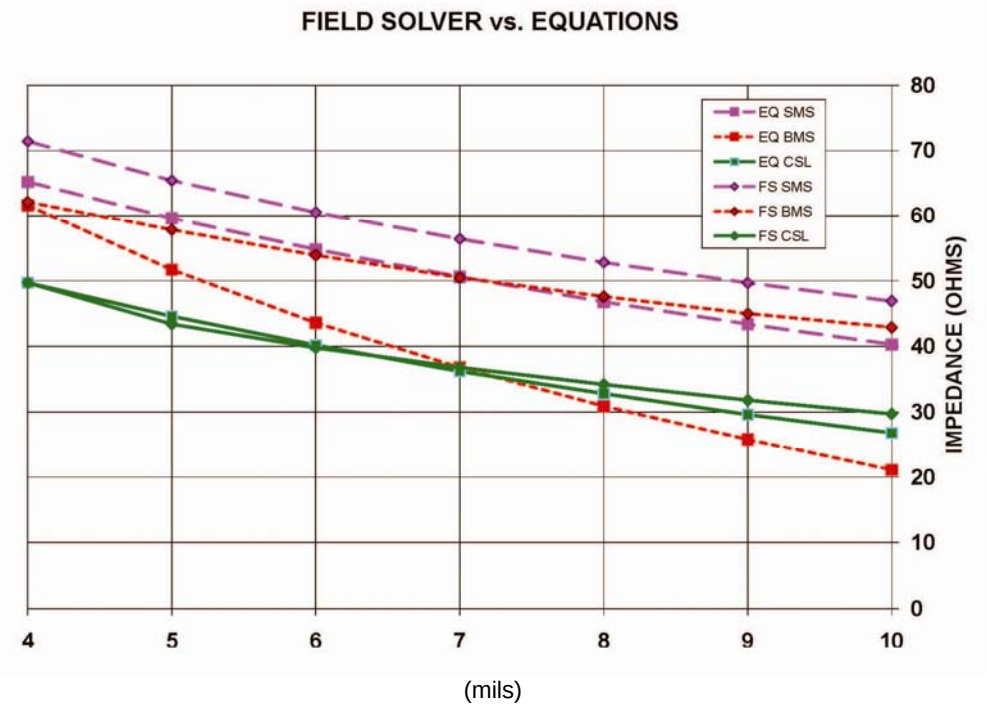

Figure 8. Impedance Results, Equations vs. Field Solvers

The conditions used for Figure 8 are: trace height above the nearest plane- 5 mils (127 microns), trace thickness- 1.4 mils (36 microns) and relative dielectric constant- 4. SMS is surface microstrip, EMS is embedded microstrip and CSL is centered stripline.

As can be seen in Figure 8, in most cases the equations predict impedances that are significantly different from the field solvers. The exception is the stripline equation vs. the field solver. The reason for this is the stripline equation was developed for the dimensions used in this example.

From experience using field solvers for hundreds of PCB designs and comparing final PCB impedance to that predicted by field solvers, I have observed that the solvers accurately predict impedance within our ability to measure it. Therefore, the difference between what the solvers predict and what the equations predict is an indicator of the accuracy of the equations. Some equations are very inaccurate and should not be used.

Therefore, field solvers should be the only tools used to calculate impedance. If a fabricator or designer uses equations instead of a field solver the result should be validated prior to using it to construct PCBs.

MEASURING IMPEDANCE

Impedance is a characteristic of a transmission line. It is expressed in ohms and is a measure of the "resistance" to the flow of energy along the transmission line. Impedance is different from resistance. Resistance is a DC characteristic while impedance is an "AC" characteristic, meaning that it is visible only with an alternating current signal. Therefore, measuring impedance cannot be done with an ordinary ohmmeter as is the case with resistance.

There are a number of ways to measure impedance. Among them are with a TDR (Time Domain Reflectometer), a Network Analyzer or an impedance bridge. The most common method of measuring impedance is with a TDR. This is the tool used by virtually all fabricators who make controlled impedance PCBs.

The basic principle on which a TDR is based is to send a fast rising edge pulse down a 50-ohm cable into the transmission line under test and observe how much, if any, of the energy in the pulse is reflected back to the source. If no energy reflects back, the impedance of the transmission line under test is the same impedance as the cable or 50 ohms. If some energy is reflected back and is the same polarity as the original pulse, the transmission line impedance is higher than that of the test cable. (See Figure 9.) If the reflected energy is in the opposite direction of the original pulse, the impedance of the line under test is lower than that of the test cable.

The ratio of the reflected pulse to the original pulse can be used to calculate the impedance of the line under test. This is the basic principal employed by all impedance testing TDR equipment.

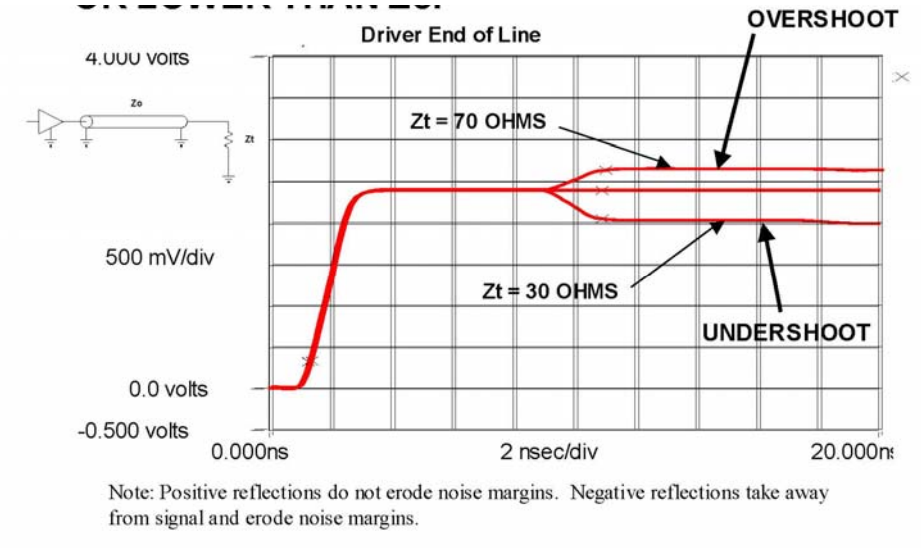

Figure 9. TDR Test Waveforms

IMPEDANCE TEST STRUCTURES

In order to verify that the desired impedance goals have been met in the final PCB, some form of test structures must be provided to allow measuring the impedance of each layer with an impedance specification. One way to do this is to use actual signal traces in each layer. The problem with this method is providing access to traces with a ground via nearby to which the probe is attached. A second problem is indicating where the test access is for each layer.

An alternative to this is to provide a test coupon with impedance test traces for each layer. These test coupons are detached from the PCB as it is routed from the panel on which the PCB was built. There are two problems with this method. The trace widths in the coupon may not be the same as in the PCB itself and the test coupons are often lost and cannot be found when needed.

A way to get around the above problems is to design impedance test traces into the body of the PCB itself. Figure 10 is an example of one way to do this. Notice that there is a "ground" via next to the via attached to each test trace. The dimensions shown fit the most common test probe systems. It is not necessary to have an access via at both ends of each trace. If the design rules spelled out in reference 2 at the back of this document for designing differential signal paths are used, namely that the spacing between members of a differential pair is enough so there is no interaction, it is not necessary to provide differential test structures as all traces will be the same impedance. Make sure to mark these test points on the silkscreen with the layer numbers to facilitate rapid testing.

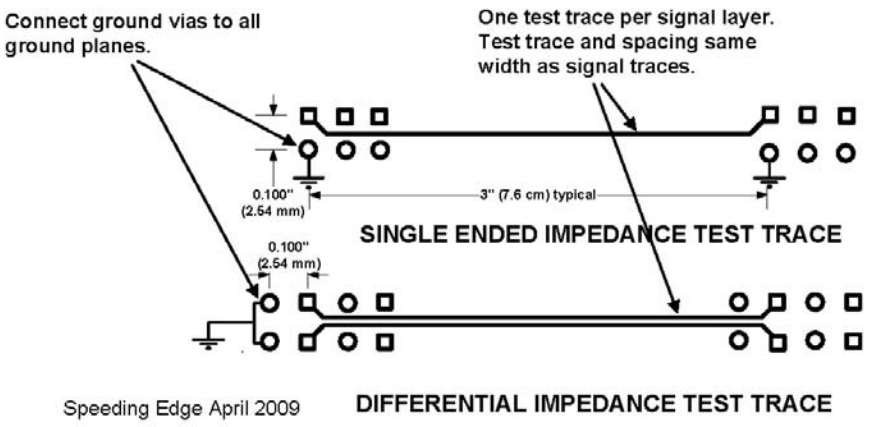

Figure 10. Typical Impedance Test Traces

IMPEDANCE ACCURACY

There are three places that impedance accuracy comes into play. These are: calculating initial impedance, measuring impedance and the accuracy of the PCB fabrication process. My experience is that when accurate dielectric values are used with field solvers, the predicted impedance is within the ability of the tools to measure it. The measurement tools can measure impedance to an accuracy of ±0.5%. The fabrication process is capable of yielding impedances within ±10% without incurring any premium charges over uncontrolled impedance PCBs. Requesting impedance accuracy tighter than ±10% is possible, but with substantial premiums added to the PCB price.

STEPS IN DESIGNING A STACKUP

From all of the above discussion, designing a proper PCB stackup might be a bit confusing. These are the steps I go through when designing a stackup. As mentioned early in this paper, I prefer the stackup approach shown on the right side of Figure 4 when the number of signal layers is beyond 2. Here are the steps I take:

1. Set the height of the signal layers above their plane partners as thin as is practical to yield good manufacturing results. This is 3 or 4 mils (76 or 102 microns) for most good fabricators.
2. Choose copper thickness for each layer that meets the signal integrity needs and is easy to manufacture.
3. Choose a glass style for these pieces of laminate that will result in uniform impedance and good differential pair performance at high data rates. (This will be laminate that does not include 106 or 1080 glass.)
4. Set the trace width to yield the proper impedance.
5. Set the trace-to-trace separation to meet crosstalk goals.
6. Set the thickness between planes to the thinnest prepreg that will result in good yields. (Thin is good for power delivery, meaning high interplane capacitance.)
7. Set the thickness between signal layers and between L2 and the surface and Ln-2 and the surface to meet the overall thickness goal. (Variations in the thickness of

these pieces of prepreg have an effect on trace impedance, but it is far smaller than variations in the thickness of the laminate between the trace layers and their nearest planes.) (See Figure 3 for an example of this.)

Once the laminate and prepreg choices have been made that meet all of the goals, these must be recorded on the stackup drawing so that multiple fabricators don't build different PCBs. In Figure 5, notice that there are three different choices for a 4-mil piece of laminate and three for 5 mils. The properties of these can be quite different, so listing only 4-mil or 5-mil dimensions on the stackup drawing is not enough to guarantee two fabricators will build the board the same way. I have had a number of students in my classes who were there because the fabricator was changed from prototyping to production and the production PCBs did not work. On investigation, it was determined that each fabricator used different laminate all of the same thickness.

Figure 10 is an example of a complete stackup drawing showing all parameters necessary to assure repeatability.

It is imperative that the exact glass styles used in each part of a stackup be listed on the stackup drawing.

ACCOUNTING FOR THE FACT THAT RESIN IN PREPREG FLOWS INTO ADJACENT SIGNAL AND PLANE LAYERS

Referring to Figure 10, there are two columns labeled Material Unpressed Thickness and Material Pressed Thickness. Listed in these columns are thicknesses for the prepreg layers. The reason for these two columns is the fact that the resin in the prepreg layers flows into the voids in the adjacent signal and power layers during lamination.

Estimating how much the thickness of each prepreg layer will diminish during lamination is a necessary part of getting the impedance right as well as getting the overall thickness right. In Figure 10, the internal layers are all ½ ounce copper which averages 0.6 mils (15.2 microns) thick when they have been through the cleaning and etching steps involved in creating them. If a conductor layer were etched until it had very little copper left on it (a signal layer) the final prepreg thickness would be reduced by 0.6 mils. Since there are usually moderate numbers of signals on signal layers, most of us reduce the final prepreg thickness by this amount.

Plane layers typically have most of the copper in place after etching, so very little resin from the prepreg flows into the voids in the plane layers. As a result we usually estimate that the prepreg thickness is diminished by about ½ of the plane layer copper thickness.

The best way to get this right is to provide the proposed stackup to the fabricator's engineering department for review.

A FULL STACKUP DRAWING

Figure 10 is a complete stackup drawing containing all of the information needed to insure a PCB is constructed to meet all of the signal integrity, power delivery and manufacturing goals. There is far more information on this stackup drawing than is usually found on such a drawing. The reasons for this have been explained previously in this document. This stackup is for a generic design that has as much routing in the horizontal direction as the vertical direction. Some designs, such as backplanes, may have substantially more wiring in one direction that the other. If this is the case, the dual stripline layers will not be well utilized due to the need to avoid routing traces one over the other in adjacent signal layers. In such cases, the stackup will need to have single stripline layers. Figure 11 is one such example.

Generic 22 Layer PCB Stackup, 93 mils thick, 09/03/09

	Layer #	Material Name	Material Type	Material Construction	Material Unpressed Er (at ~2 GHz)	Material Pressed Er (at ~2 GHz)	Material Unpressed Thickness (mils)	Material Pressed Thickness (mils)	Picture	Copper Thickness (mils)	Copper Thickness (oz)		Single Ended Trace Width (mils)	Single Ended Imped. (ohms)	
								0.7	Solder Mask						
Top	1								1	2.2	1.5				
		FR-408HR	Prepreg	1 x 3313 RC = 53.8%	3.7		3.7	3.5	Prepreg						
S1	2								2	0.6	0.5		4.5	51.0	
		FR-408HR	Core	1 x 1086 RC = 58%	3.6			3.5	Core						
Ground	3								3	0.6	0.5				
		FR-408HR	Prepreg	1 x 2113 RC = 57%	3.63		4	3	Prepreg						
V1	4								4	0.6	0.5				
		FR-408HR	Core	1 x 3313 RC = 53.8%	3.7			4	Core						
S2	5								5	0.6	0.5		4	49.5	
		FR-408HR	Prepreg	1 X 3313 RC = 53.8%	3.7		4	3.4	Prepreg						
S3	6								6	0.6	0.5		4	49.5	
		FR-408HR	Core	1 x 3313 RC = 53.8%	3.7			4	Core						
Ground	7								7	0.6	0.5				
		FR-408HR	Prepreg	1 x 2113 RC = 57%	3.63		4	3	Prepreg						
V2	8								8	0.6	0.5				
		FR-408HR	Core	1 x 3313 RC = 53.8%	3.7			4	Core						
S4	9								9	0.6	0.5		4	49.5	
		FR-408HR	Prepreg	1 X 3313 RC = 53.8%	3.7		4	3.4	Prepreg						
S5	10								10	0.6	0.5		4	49.5	
		FR-408HR	Core	1 x 3313 RC = 53.8%	3.7			4	Core						
Ground	11								11	0.6	0.5				
		FR-408HR	Prepreg	1 x 2113 RC = 57%	3.63		4	3	Prepreg						
V3	12								12	0.6	0.5				
		FR-408HR	Core	1 x 3313 RC = 53.8%	3.7			4	Core						
S6	13								13	0.6	0.5		4	49.5	
		FR-408HR	Prepreg	1 X 3313 RC = 53.8%	3.7		4	3.4	Prepreg						
S7	14								14	0.6	0.5		4	49.5	
		FR-408HR	Core	1 x 3313 RC = 53.8%	3.7			4	Core						
Ground	15								15	0.6	0.5				
		FR-408HR	Prepreg	1 x 2113 RC = 57%	3.63		4	3	Prepreg						
V4	16								16	0.6	0.5				
		FR-408HR	Core	1 x 3313 RC = 53.8%	3.7			4	Core						
S8	17								17	0.6	0.5		4	49.5	
		FR-408HR	Prepreg	1 X 3313 RC = 53.8%	3.7		4	3.4	Prepreg	<-					
S9	18								18	0.6	0.5		4	49.5	
		FR-408HR	Core	1 x 3313 RC = 53.8%	3.7			4	Core						
V5	19								19	0.6	0.5				
		FR-408HR	Prepreg	1 x 2113 RC = 57%	3.63		4	3	Prepreg						
Ground	20								20	0.6	0.5				
		FR-408HR	Core	1 x 1086 RC = 58%	3.6			3.5	Core						
S10	21								21	0.6	0.5		4.5	51.0	
		FR-408HR	Prepreg	1 x 3313 RC = 53.8%	3.7		3.7	3.5	Prepreg						
Bottom	22								22	2.2	1.5				
								0.7	Solder Mask						
								--------		--------					
								76.0	92.4	16.4					
								Material Thickness	Total Thickness	Copper Thickness					

Note: Place only information to left of dark line on fabrication drawing. Do not place impedance information on fabrication drawing.
Prepared by Speeding Edge, 09/03/09

Figure 10. A Complete Stackup Drawing for a 22-Layer PCB

GENERIC 22 LAYER SWITCH FABRIC PCB STACKUP 09/03/09

	Layer #	Material Name	Material Type	Material Construction	Material Unpressed Er (at ~2 GHz)	Material Pressed Er (at ~2 GHz)	Material Unpressed Thickness (mils)	Material Pressed Thickness (mils)	Picture	Copper Thickness (mils)	Copper Thickness (oz)		Single Ended Trace Width (mils)	Single Ended Imped. (ohms)
								0.7	Solder Mask 1					
Top	1									2.2	1.5			
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.4	Prepreg 2					
S1	2									0.6	0.5		4.5	50.0
		FR-408	Core	1 x 2113 RC = 44%	4.2			3	Core 3					
Ground	3									0.6	0.5			
		FR-408	Prepreg	1 x 2113 RC = 57%	4		4	3	Prepreg 4					
V1	4									0.6	0.5			
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core 5					
S2	5									0.6	0.5		4	51.0
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepreg 6					
Ground	6									0.6	0.5			
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core 7					
S3	7									0.6	0.5		4	51.0
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepreg 8					
Ground	8									0.6	0.5			
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core 9					
S4	9									0.6	0.5		4	51.0
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepreg 10					
Ground	10									0.6	0.5			
		FR-408	Core	1 x 2113 RC = 44%	4.2			3	Core 11					
V2	11									0.6	0.5			
		FR-408	Prepreg	2 x 106 RC = 63.3%	3.7		4	3.4	Prepreg 12					
Ground	12									0.6	0.5			
		FR-408	Core	1 x 2113 RC = 44%	4.2			3	Core 13					
V3	13									0.6	0.5			
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepreg 14					
S7	14									0.6	0.5		4	51.0
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core 15					
Ground	15									0.6	0.5			
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepreg 16					
S8	16									0.6	0.5		4	51.0
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core 17					
Ground	17									0.6	0.5			
		FR-408	Prepreg	1 X 3313 RC + 1 X 106 = 56%	3.7		6.5	6	Prepreg 18	<-				
S9	18									0.6	0.5		4	51.0
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core 19					
V6	19									0.6	0.5			
		FR-408	Prepreg	2 x 106 RC = 63.3%	4		4	3	Prepreg 20					
Ground	20									0.6	0.5			
		FR-408	Core	1 x 2113 RC = 44%	4.2			3	Core 21					
S10	21									0.6	0.5		4.5	50.0
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.4	Prepreg 22					
Bottom	22									2.2	1.5			
								0.7	Solder Mask					
								89.6	106.0	16.4				
								Material Thickness	Total Thickness	Copper Thickness				

Note: Place only information to left of dark line on fabrication drawing. Do not place impedance information on fabrication drawing.
Prepared by Speeding Edge, 09/03/09
Layers 1 and 22 are to be used for component mounting and traces that are not controlled impedance.

Figure 11. A Stackup Drawing for a 22-Layer Switch Fabric

TOOLS FOR CREATING PCB STACKUPS

There are a number of commercially available tools based on field solvers that permit the design of a complete stackup. Among these are:

- Hyperlynx Linesim from Mentor Graphics
- Allegro PCB Si from Cadence
- Si9000 and Speedstack 2008 from Polar Instruments

The problem with all of these tools is the lack of a place to record the laminate type and weave for each opening in the stackup. To solve this problem, some colleagues of mine developed the EXCEL spreadsheet shown in Figures 10 and 11 for this purpose. The reader is encouraged to use this form if it makes recording stackup information convenient.

WHAT ABOUT FOUR LAYER PCBS?

All of the discussion above has involved designing PCB stackups that have sufficient numbers of layers to meet all of the signal integrity requirements of high speed designs. Many designs that are cost driven require the use of four layer PCBs. These PCBs usually contain two planes and two signal layers and are stacked signal, plane, plane, signal. The three main signal integrity considerations when designing a PCB stackup are impedance control, crosstalk control and creation of interplane capacitance for the PDS. In order to minimize crosstalk the signal layers must be close to the planes. In order to create interplane capacitance the planes must be close to each other. These two considerations are in direct conflict with each other. Figure 12 illustrates a stackup that has been designed to meet the crosstalk and impedance goals.

Notice that the two signal layers are on the outside of the stackup and the two planes are on the inside. Further, the two signal layers are very close to the plane layers. This results in excellent crosstalk and impedance control. In order to meet the overall thickness goal, something close to 60 mils, (1.52 mm) the plane layers are very far apart. As a result, there is no useful plane capacitance for use by the PDS.

It has been demonstrated many times that high speed single-ended buses require plane capacitance in order for them to function correctly. How is it possible to make a high speed design such as a PC with wide single-ended PCI and memory buses function properly with such a stackup? The answer is that the necessary high quality capacitance is built into the ICs themselves. As a result, there is no need for plane capacitance on the PCB. When a four-layer PCB is used with ICs that don't have built-in capacitance, signal integrity problem nearly always are part of such a design.

	GENERIC 4 LAYER PCB 090909													
	Layer #	Material Name	Material Type	Material Construction	Material Unpressed Er (at ~2 GHz)	Material Pressed Er (at ~2 GHz)	Material Unpressed Thickness (mils)	Material Pressed Thickness (mils)	Picture	Copper Thickness (mils)	Copper Thickness (oz)		Single Ended Trace Width (mils)	Single Ended Imped. (ohms)
								0.7	Solder					
Top	1								1	2.2	1.5		4.5	50.0
		FR-408	Prepreg	1 X 3313 R	3.7		4	3.4	Prepreg					
Ground	2								2	0.6	0.5			
		FR-408	Core	6 x 7628 R	4.06			42	Core					
V1	3								3	0.6	0.5			
		FR-408	Prepreg	1 X 3313 R	3.7		4	3.4	Prepreg					
Bottom	4								8	2.2	1.5		4.5	50.0
								0.7	Solder	--------				
								--------	55.8	5.6				
								50.2	Total Thickness	Copper Thickness				

Figure 12. A Stackup Drawing for a Generic Four-Layer PC Motherboard

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