Sequential Circuit Timing

Objectives

This section covers several timing considerations encountered in the design of synchronous sequential circuits. It has the following objectives:

- Define the following global timing parameters and show how they can be derived from the basic timing parameters of flip-flops and gates.
  - Maximum Clock Frequency
  - Maximum allowable clock skew
  - Global Setup and Hold Times
- Discuss ways to control the loading of data into registers and show why gating the clock signal to do this is a poor design practice.

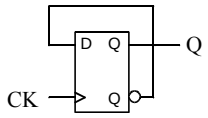
Reading Assignment

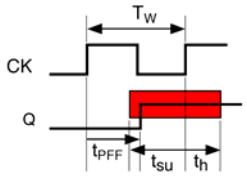
- Sections 3.5 and 3.6. Please also see .ppt slides posted on the web - the animation helps a lot!

13.1. Maximum Clock Frequency

- The clock frequency for a synchronous sequential circuit is limited by the timing parameters of its flip-flops and gates. This limit is called *the maximum clock frequency* for the circuit. The *minimum clock period* is the reciprocal of this frequency.
- Relevant timing parameters
  - Gates:
    - Propagation delays: min t_{PLH}, min t_{PHL}, max t_{PLH}, max t_{PHL}
  - Flip-Flops:
    - Propagation delays: min t_{PLH}, min t_{PHL}, max t_{PLH}, max t_{PHL}
    - Setup time: t_{su}
    - Hold time: t_h

- Example





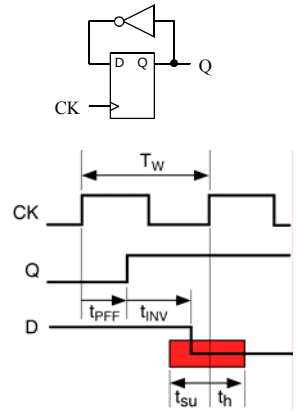
$T_W \geq \max t_{PFF} + t_{su}$

- For the 7474, max t_{PLH} = 25ns, max t_{PHL} = 40ns, t_{su} = 20ns

  $T_W \geq \max (\max t_{PLH} + t_{su,} \max t_{PHL} + t_{su})$

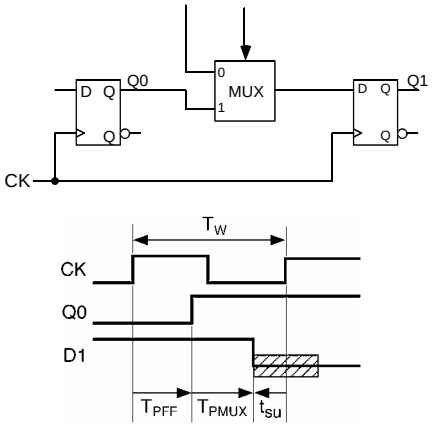
  $T_W \geq \max (25+20, 40+20) = 60$

Example



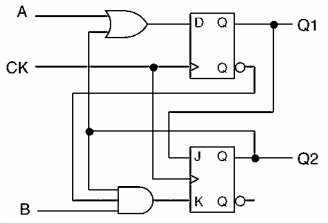
$$T_W \geq \max t_{PFF} + \max t_{PINV} + t_{su}$$

Example



$$T_W \geq \max t_{PFF} + \max t_{PMUX} + t_{su}$$

Example



	t_P	t_{su}
D Flip-Flop:	20 ns	5 ns
JK Flip-Fllp:	25 ns	10 ns
AND Gate:	12 ns	
OR Gate:	10 ns	

Paths from Q1 to Q1: None

Paths from Q1 to Q2: $T_W \geq \max t_{PDFF} + t_{JKsu} = 20 + 10 = 30$ ns

$T_W \geq \max t_{PDFF} + \max t_{AND} + t_{JKsu} = 20 + 12 + 10 = 42$ ns

Paths from Q2 to Q1: $T_W \geq \max t_{PJKFF} + t_{OR} + T_{Dsu} = 25 + 10 + 5 = 40$ ns

Paths from Q2 to Q2: $T_W \geq \max t_{PJKFF} + \max t_{AND} + t_{JKsu} = 25 + 12 + 10 = 47$ ns

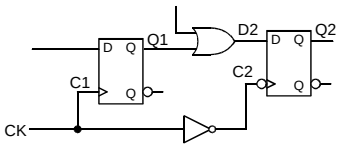
$$TW \geq 47 \text{ ns}$$

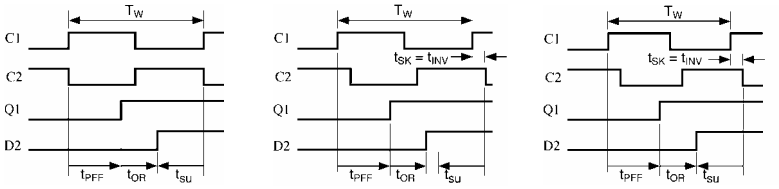
Clock Skew

- If a clock edge does not arrive at different flip-flops at exactly the same time, then the clock is said to be *skewed* between these flip-flops. The difference between the times of arrival at the flip-flops is said to be the amount of *clock skew*.
- Clock skew is due to different delays on different paths from the clock generator to the various flip-flops.
  - Different length wires (wires have delay)
  - Gates (buffers) on the paths
  - Flip-Flops that clock on different edges (need to invert clock for some flip-flops)
  - Gating the clock to control loading of registers (a very bad idea)

Example (Effect of clock skew on clock rate)

- Clock C2 skewed after C1

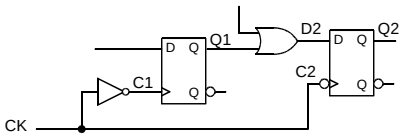


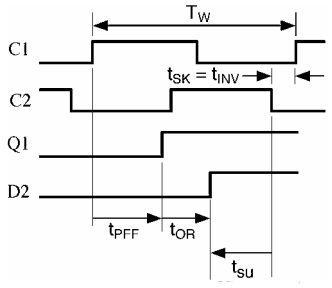


$T_W \geq \max T_{PFF} + \max t_{OR} + t_{su}$
(if clock not skewed, i.e., $t_{INV} = 0$)

$T_W \geq \max T_{PFF} + \max t_{OR} + t_{su} - \min t_{INV}$
(if clock skewed, i.e., $t_{INV} > 0$)

- Clock C1 skewed after C2

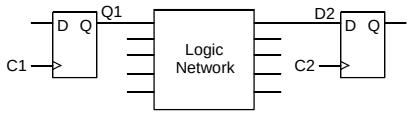


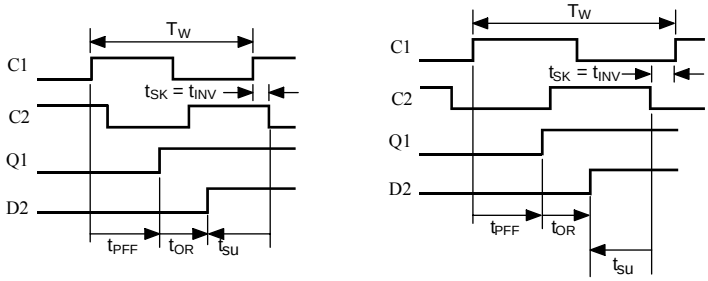


$T_W \geq \max T_{PFF} + \max t_{OR} + t_{su}$
(if clock not skewed, i.e., $t_{INV} = 0$)

$T_W \geq \max T_{PFF} + \max t_{OR} + t_{su} + \max t_{INV}$
(if clock skewed, i.e., $t_{INV} > 0$)

Summary of maximum clock frequency calculations

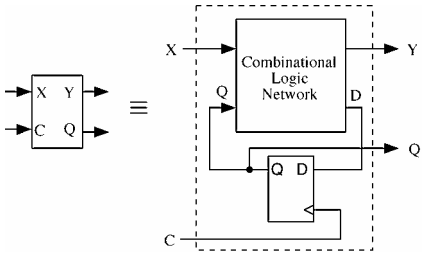




C2 skewed after C1: $T_W \geq \max T_{PFF} + \max t_{NET} + t_{su} - \min t_{INV}$

C2 skewed before C1: $T_W \geq \max T_{PFF} + \max t_{NET} + t_{su} + \max t_{INV}$

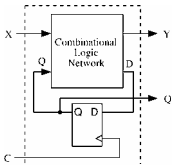
Example

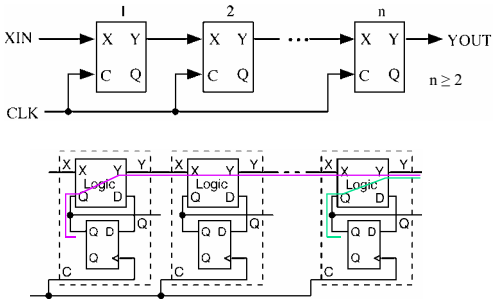


t_{XY} = Network delay from X to Y
t_{XD} = Network delay from X to D
t_{QY} = Network delay from Q to Y
t_{QD} = Network delay from Q to D

- For each of the following two connections find
  - The minimum clock period
  - The maximum and minimum delay from CLK to YOUT

■ Circuit 1:





t_{XY} = Network delay from X to Y
t_{XD} = Network delay from X to D
t_{QY} = Network delay from Q to Y
t_{QD} = Network delay from Q to D

Minimum Clock Period:

$$Tw \geq \max t_{PFF} + \max t_{QY} + (n-2) \max t_{XY} + \max t_{XD} + t_{su} \geq T_W$$

$$Tw \geq \max t_{PFF} + \max t_{QD} + t_{su}$$

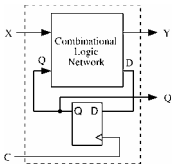
Maximum Delay:

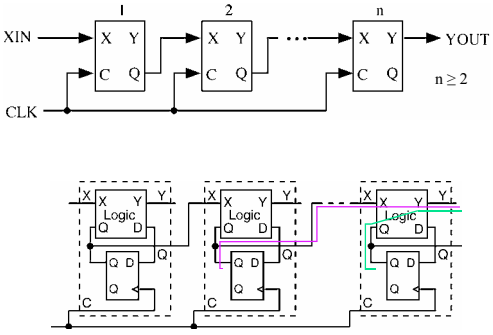
$$T_{CY} \leq \max t_{PFF} + \max t_{QY} + (n-1) \max t_{XY}$$

Minimum Delay:

$$T_{CY} \geq \min t_{PFF} + \min t_{QY}$$

■ Circuit 2:





t_{XY} = Network delay from X to Y
t_{XD} = Network delay from X to D
t_{QY} = Network delay from Q to Y
t_{QD} = Network delay from Q to D

Minimum Clock Period:

$$Tw \geq \max t_{PFF} + \max t_{XD} + t_{su}$$

$$Tw \geq \max t_{PFF} + \max t_{QD} + t_{su}$$

Maximum Delay:

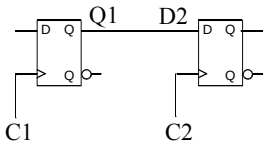
$$T_{CY} \leq \max t_{PFF} + \max (\max t_{XY}, \max t_{QY})$$

Minimum Delay:

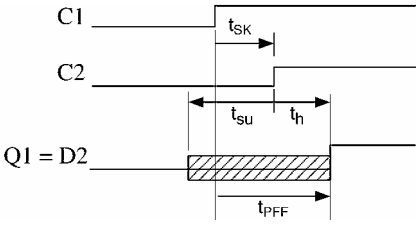
$$T_{CY} \geq \min t_{PFF} + \min (\min t_{XY}, \min t_{QY})$$

2. Maximum Allowable Clock Skew

- How much skew between C1 and C2 can be tolerated in the following circuit?



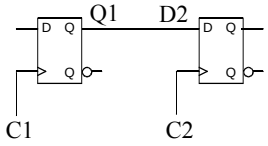
- Case 1: C2 delayed after C1

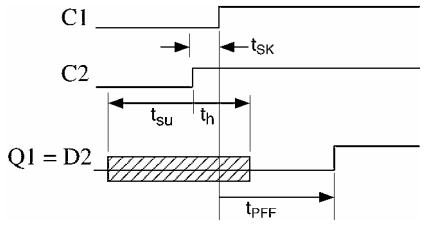


$t_{PFF} > t_h + t_{SK}$

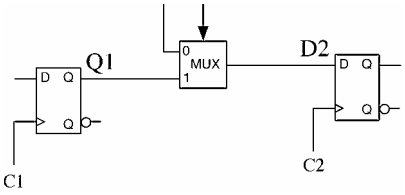
$t_{SK} < \min t_{PFF} - t_h$

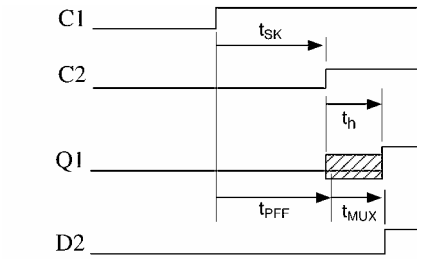
- Case 2: C1 delayed from C2





- How does additional delay between the flip-flops affect the skew calculations?

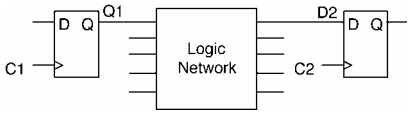


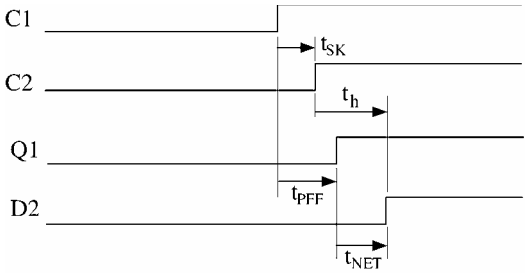


$t_{SK} \leq \min t_{PFF} - t_h$

$t_{sk} \leq \min t_{PFF} + \min t_{MUX} - t_h$

- Summary of allowable clock skew calculations

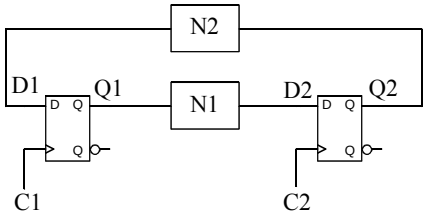


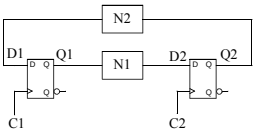


$t_{SK} + t_h \leq t_{PFF} + t_{NET}$

$t_{SK} \leq \min t_{PFF} + \min t_{NET} - t_h$

- Example: What is the minimum clock period for the following circuit under the assumption that the clock C2 is skewed after C1 (i.e., C2 is delayed from C1)?





- First calculate the maximum allowable clock skew.

  $t_{SK} < \min t_{PFF} + \min t_{N1} - t_h$

- Next calculate the minimum clock period due to the path from Q1 to D2.

  $T_W > \max t_{PFF} + \max t_{N1} + t_{su} - \min t_{SK}$

- Finally calculate the minimum clock period due to the path from Q2 to D1

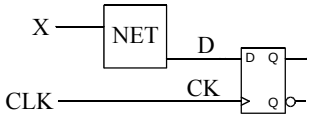
  $T_W > \max t_{PFF} + \max t_{N2} + t_{su} + \max t_{SK}$

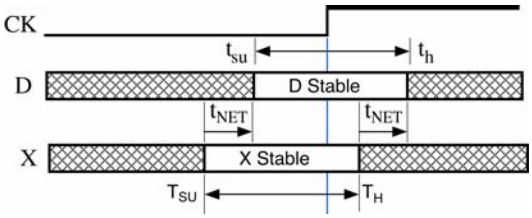
  $T_W > \max t_{PFF} + \max t_{N2} + t_{su} + (\min t_{PFF} + \min t_{N1} - t_h)$

  $T_W > \max t_{PFF} + \min t_{PFF} + \max t_{N2} + \min t_{N1} + t_{su} - t_h$

3. Global Setup Time, Hold Time and Propagation Delay

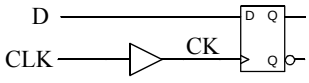
- Global setup and hold times (data delayed)

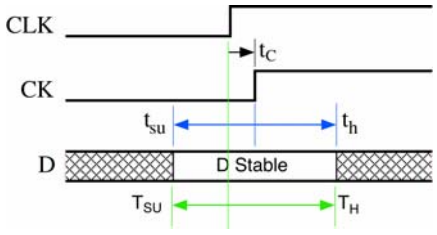




$T_{SU} = t_{su} + \max t_{NET}$ $T_H = t_h - \min t_{NET}$

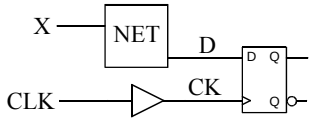
- Global setup & hold time (clock delayed)

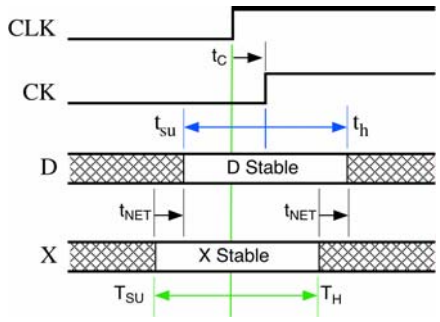




$T_{SU} = t_{su} - \min t_C$ $T_H = t_h + \max t_C$

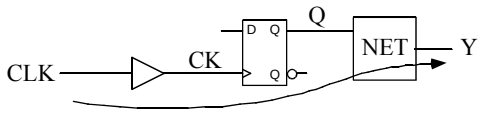
Global setup & hold time (data & clock delayed)

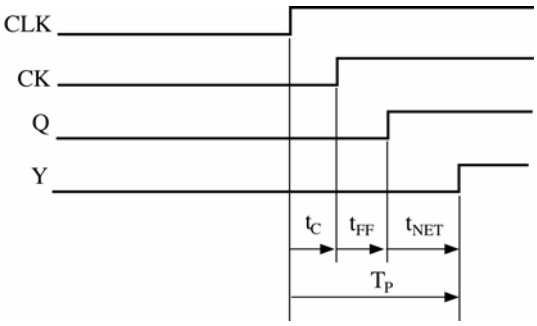




$T_{SU} = t_{su} + \max t_{NET} - \min t_C$ $\quad T_H = t_h - \min t_{NET} + \max t_C$

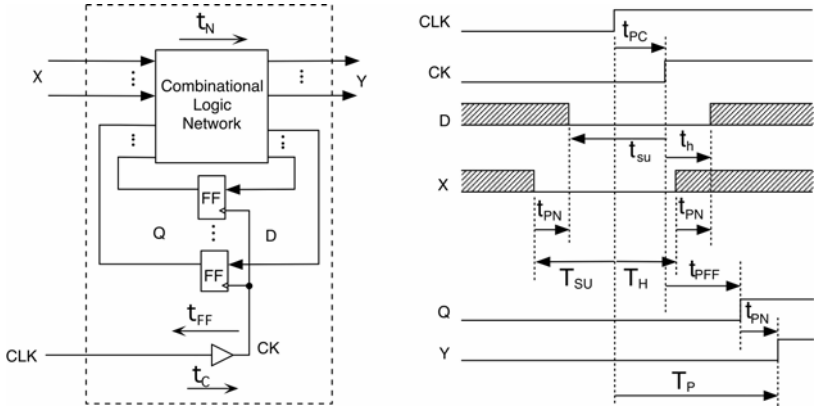
Global propagation delay





$T_P = t_C + t_{FF} + t_{NET}$

Summary of global timing parameters

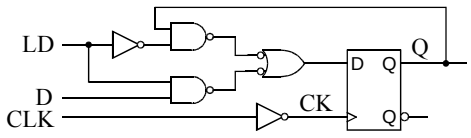


$$T_{SU} = t_{su} + \max t_{PN} - \min t_{PC} \le t_{su} + \max t_{PN}$$

$$T_H = t_h + \max t_{PC} - \min t_{PN} \le t_h + \max t_{PC}$$

$$T_P = t_{PFF} + t_{PN} + t_{PC}$$

Example



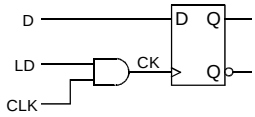
- Find T_{SU} and T_H for input signal LD relative to CLK.

$$T_{SU} = t_{su} + \max t_{NET} - \min t_C$$
$$= t_{su} + \max t_{INV} + \max t_{NAND} + \max t_{NAND} - \min t_{INV}$$

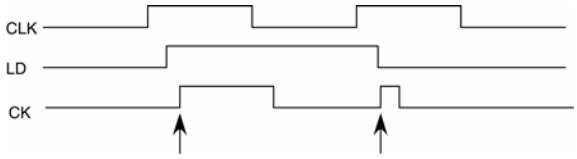
$$T_H = t_h - \min t_{NET} + \max t_C$$
$$= t_h - \min t_{NAND} - \min t_{NAND} + \max T_{INV}$$

4. Register load control (gating the clock)

- A very bad way to add a load control signal LD to a register that does not have one is shown below

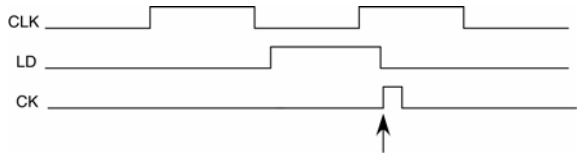


- The reason this is such a bad idea is illustrated by the following timing diagram.

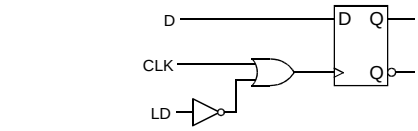


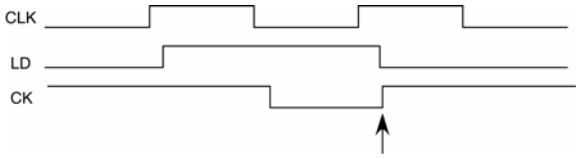
- The flip-flop sees two rising edges and will trigger twice. The only one we want is the second one.

- If LD was constrained to only change when the clock was low, then the only problem would be the clock skew.



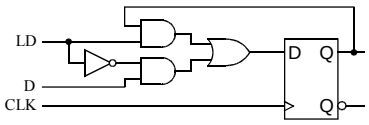
- If gating the clock is the only way to control the loading of registers, then use the following approach:



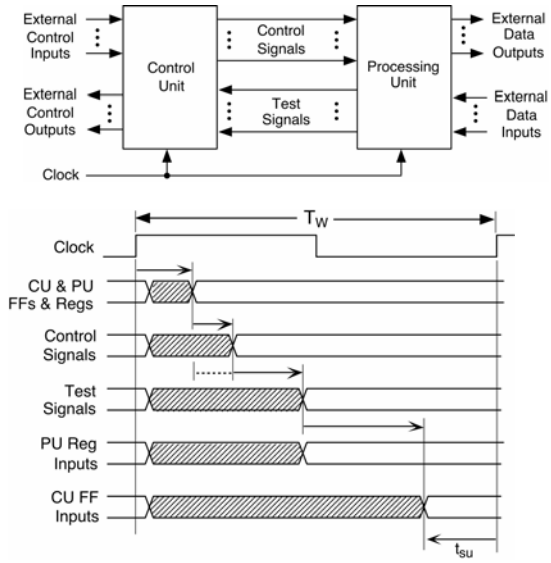


  - There is still clock skew, but at least we only have one triggering edge.

- The best way to add a LD control signal is as follows:



5. Synchronous System Structure and Timing



6. Review

- How the flip-flop and gate timing parameters affect the maximum possible clock frequency.
  - How clock skew affect maximum possible clock frequency.
- How the delay of logic between flip-flops affects the maximum allowable clock skew.
- How flip-flop setup and hold times are translated by the combinational logic delays to get global setup and hold times.
- The detrimental effect of gating the clock signal.

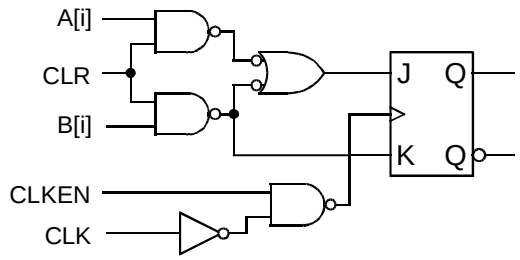
Extra Timing Problems

- The following logic diagram shows the implementation of the i^{th} bit slice of a register. Derive the global setup and hold times T_{SU} and T_H for CLR and the maximum and minimum propagation delays max T_P and min T_P from CLK to the flip-flop outputs. Use the following timing parameters.

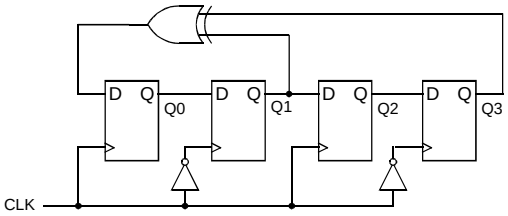
  JK Flip-Flop: $5ns \le t_{PFF} \le 15ns$ $t_{su} = 12ns$ $t_h = 6ns$

  NAND Gate: $3ns \le t_{PNAND} \le 10ns$

  Inverter: $2ns \le t_{PINV} \le 8ns$



- Determine the minimal clock period T_W for the following circuit. Use the following delay values for the flip-flops and gates.
  - Flip-Flop: $5 \le t_{PFF} \le 14ns$; $t_{su} = 6ns$; $t_h = 10ns$
  - Inverter: $2 \le t_{PINV} \le 12$
  - XOR Gate: $7 \le t_{XOR} \le 22$



Part a) Work the problem under the assumption that the clock is symmetrical. That is, it is high for 50% of the clock period and low for 50% of the clock period.

Part b) Work the problem under the assumption that the clock is high for 20% of the clock period and low for 80% of the clock period.