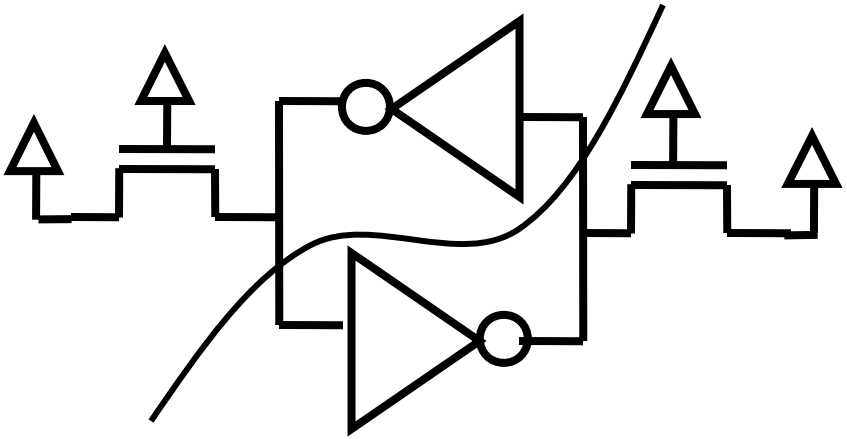
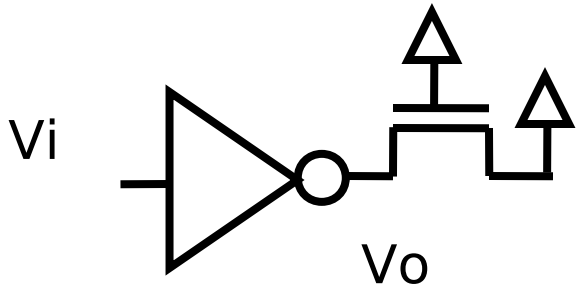
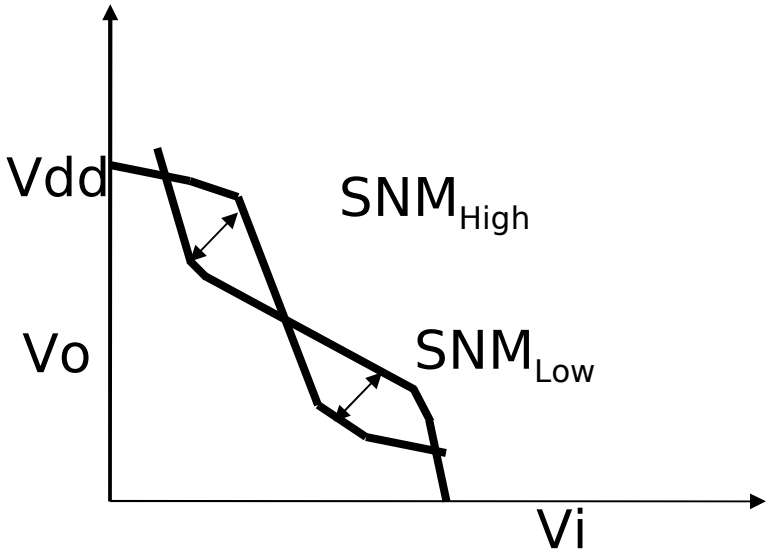
SRAM Design

Increase Read Noise Margin





$\beta_d >> \beta_a$



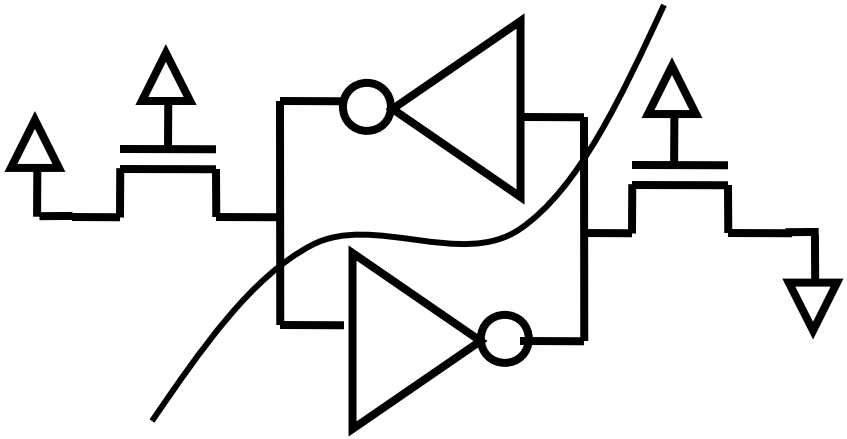
Increase cell Vdd

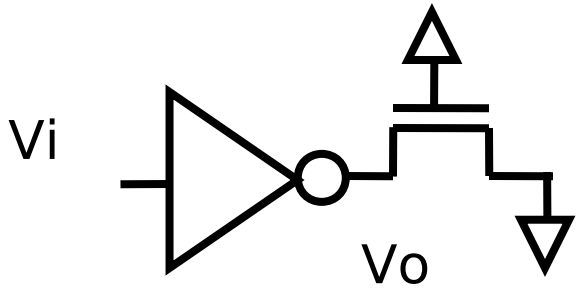
Increase Vth

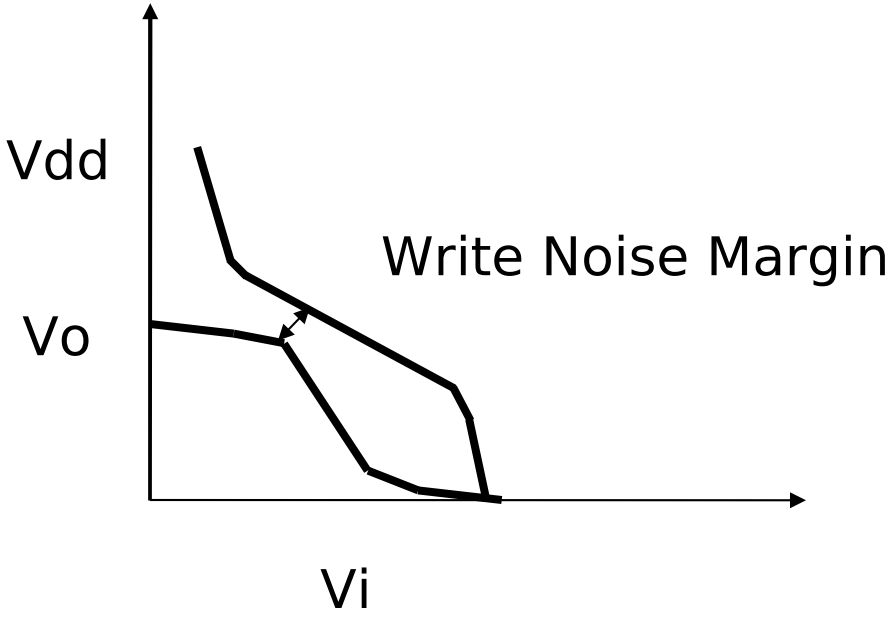
Reduce wordline Vdd

Don’t allow readcurrent through cell

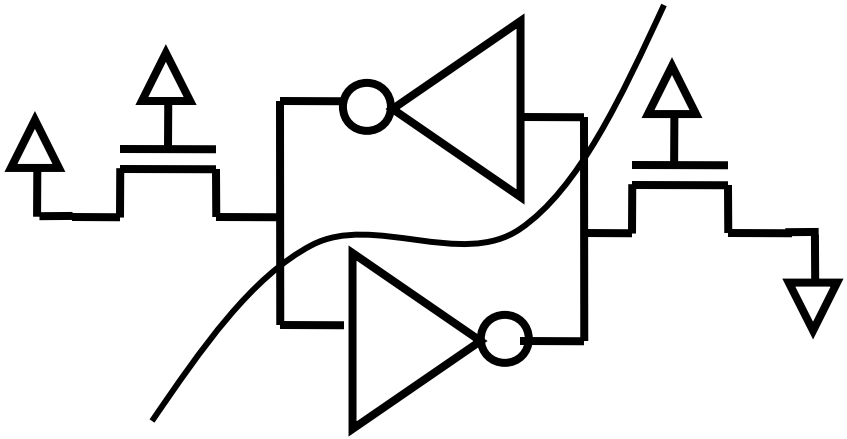
SRAM Cell Design: Write Margin

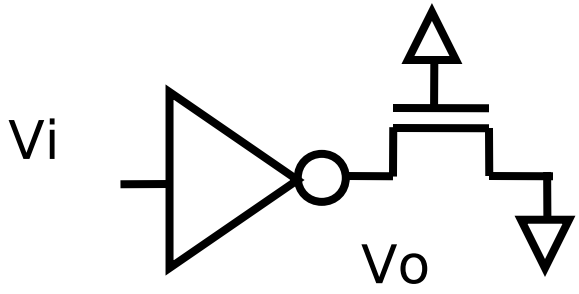






How to Improve Write Margin

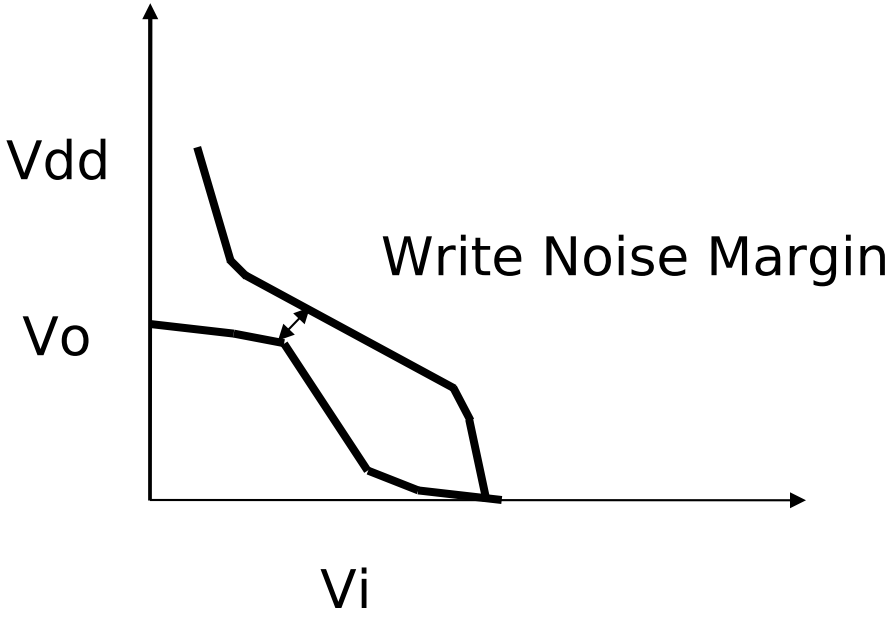




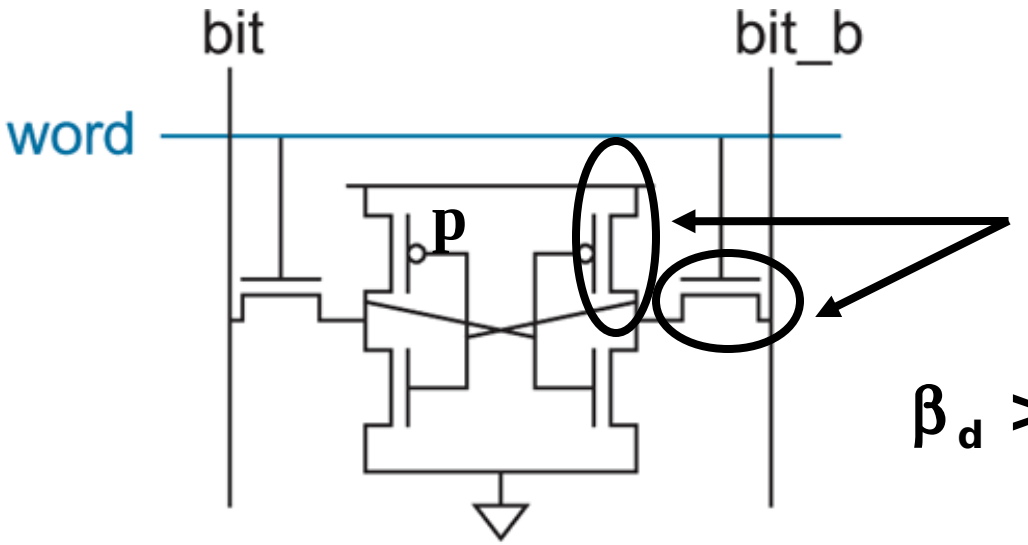
$\beta_a >> \beta_p$

Decrease Cell Vdd

Increase WL Vdd



SRAM Cell Sizing



Tradeoffs

Read Noise Margin

Cell Read Current

Write Noise Margin

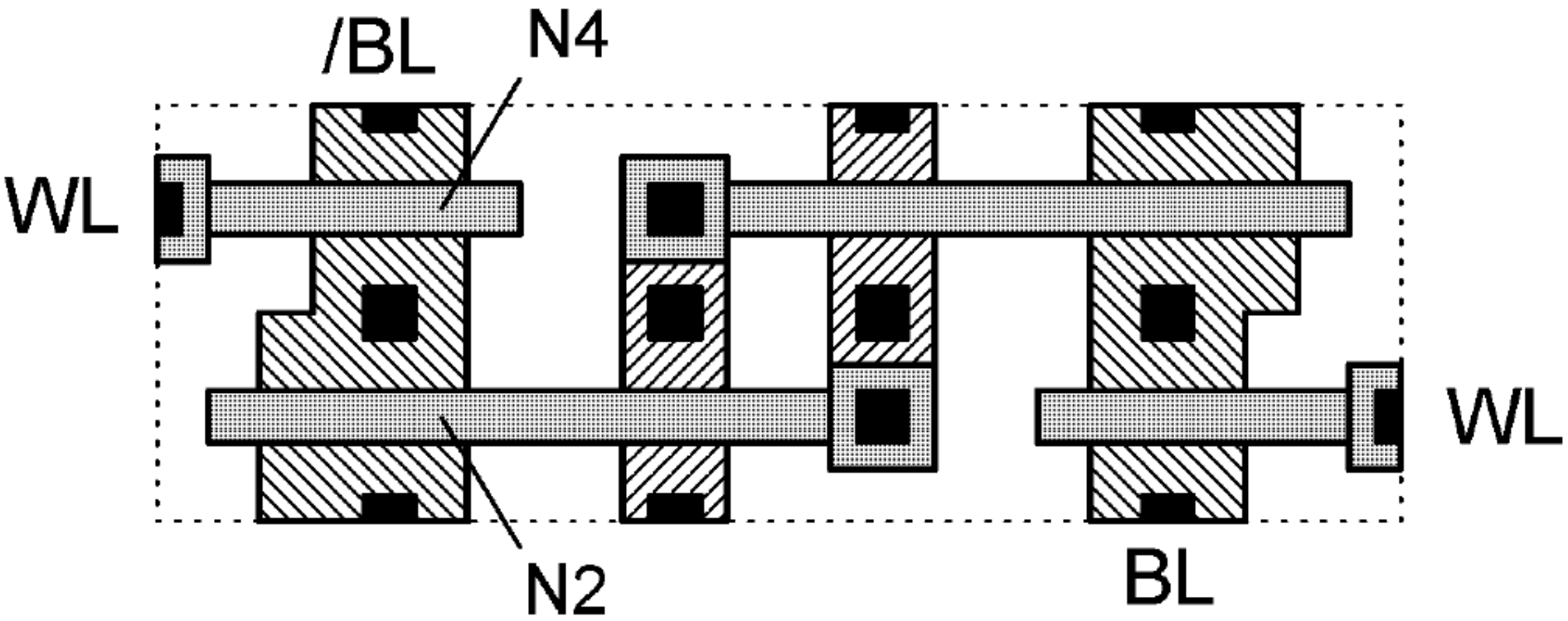
Cell Size

$\beta_d >> \beta_a$

$\beta_d \sim 3 \times \beta_a$

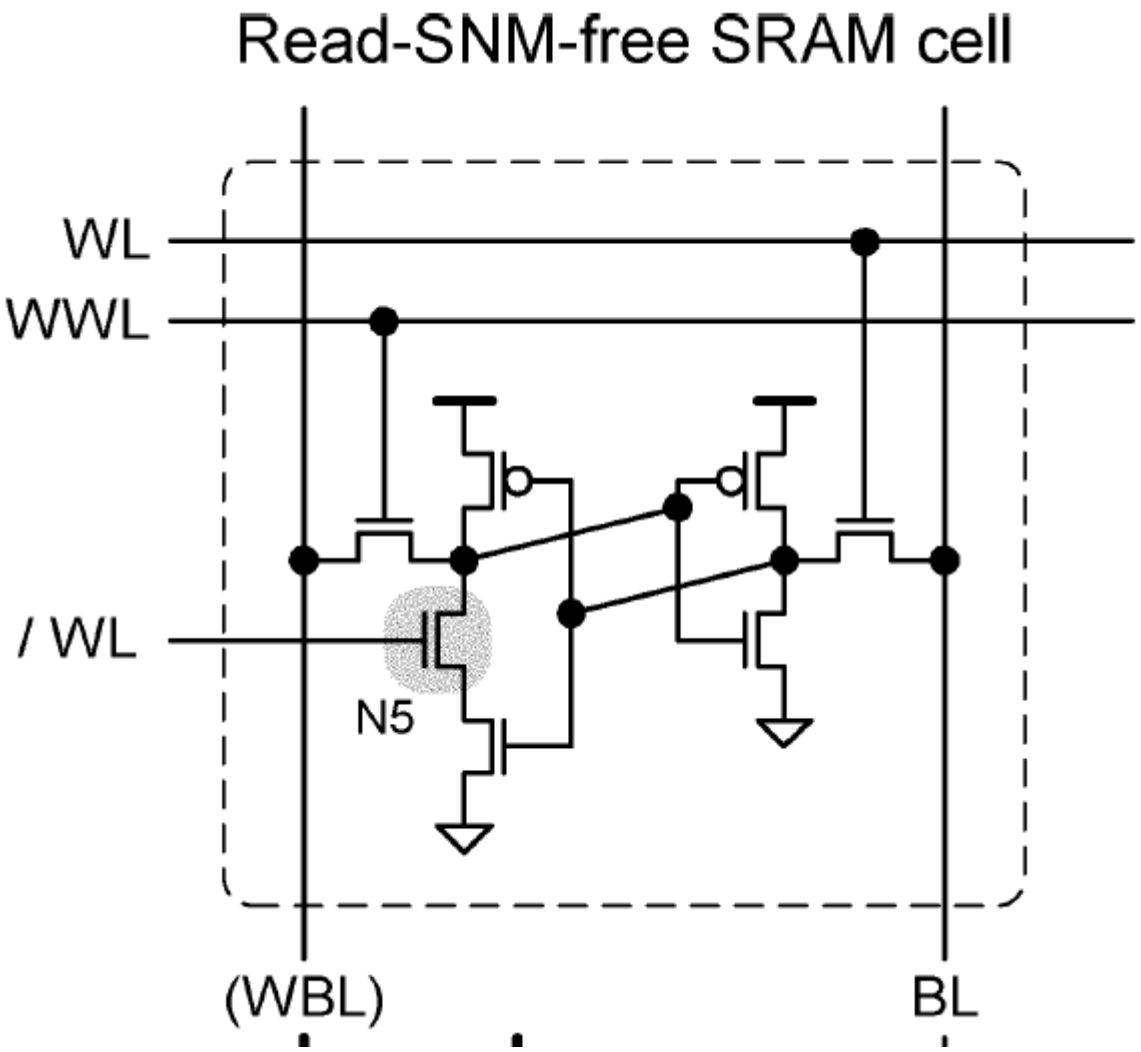
$\beta_a >> \beta_p$

Layout of SRAM Cell



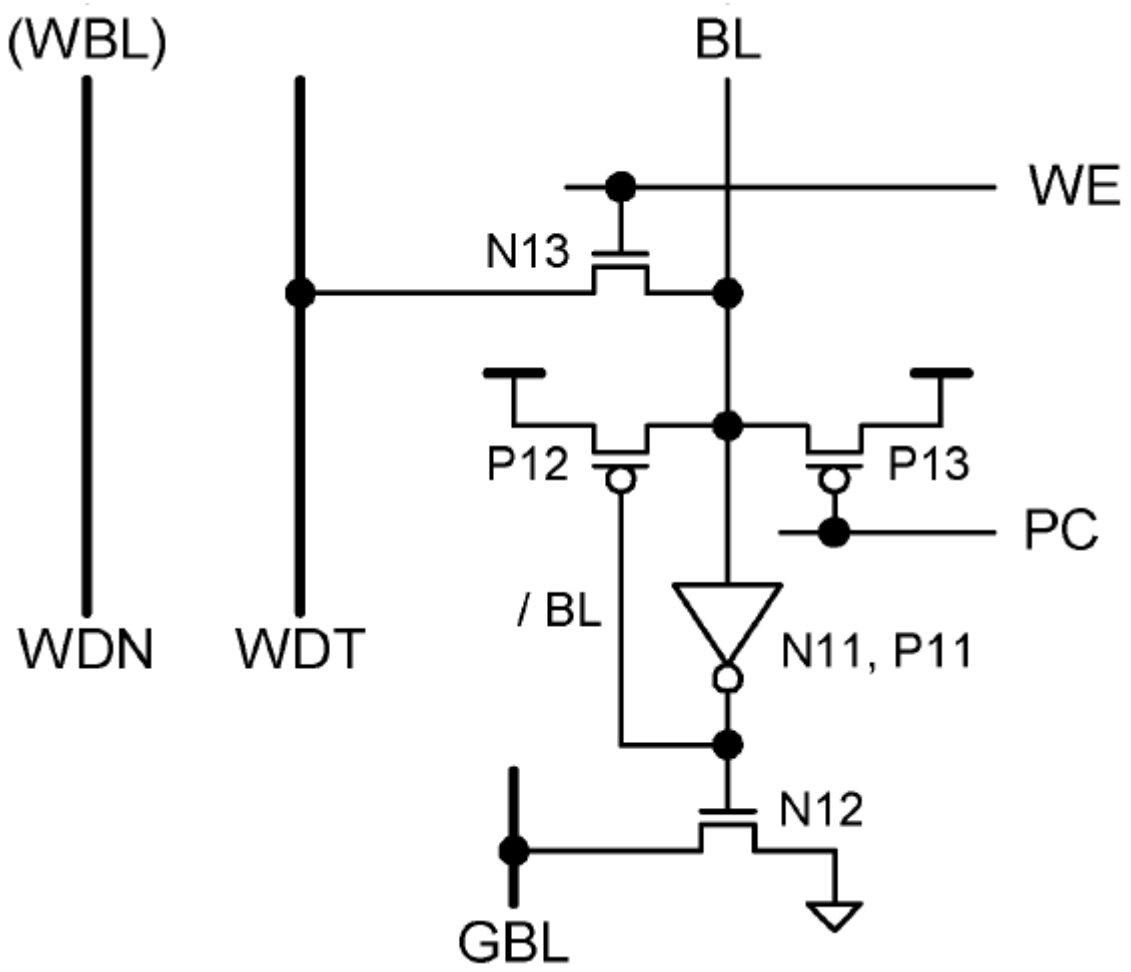
[Takeda, et. al., JSSC, Jan 2006]

7-T Cell



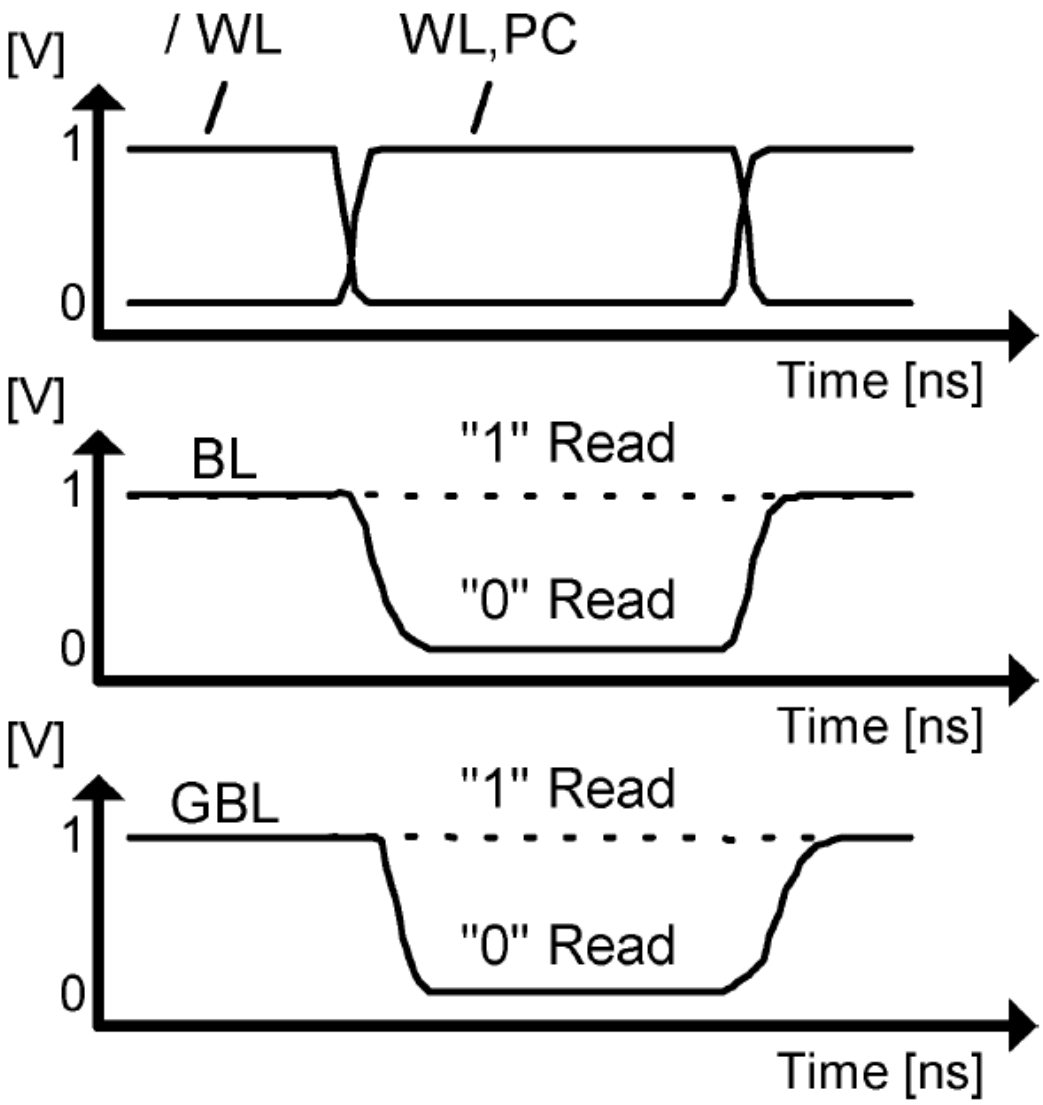
[Takeda, et. al., JSSC, Jan 2006]

Read/Write Circuitry



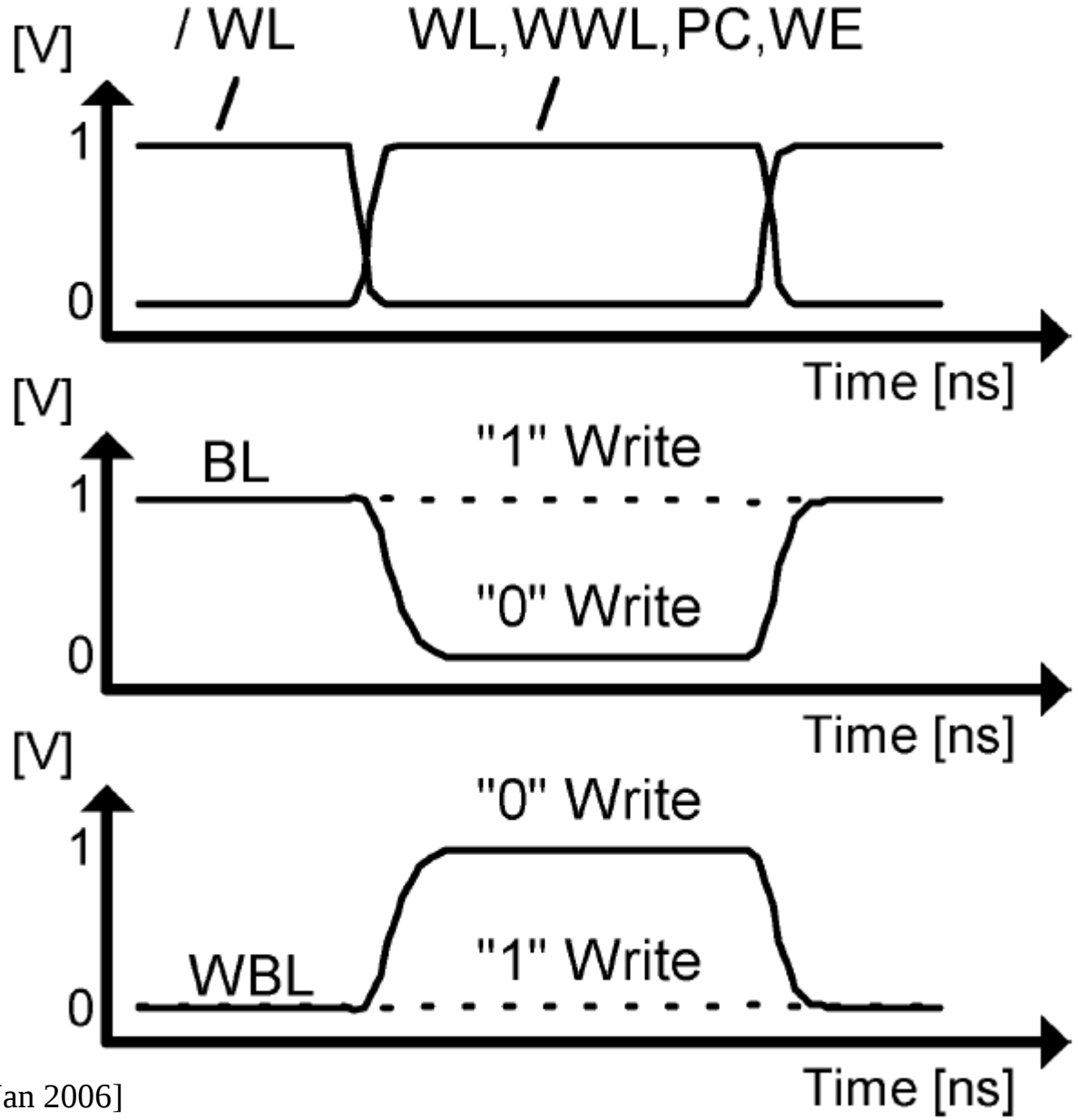
[Takeda, et. al., JSSC, Jan 2006]

Read Waveforms



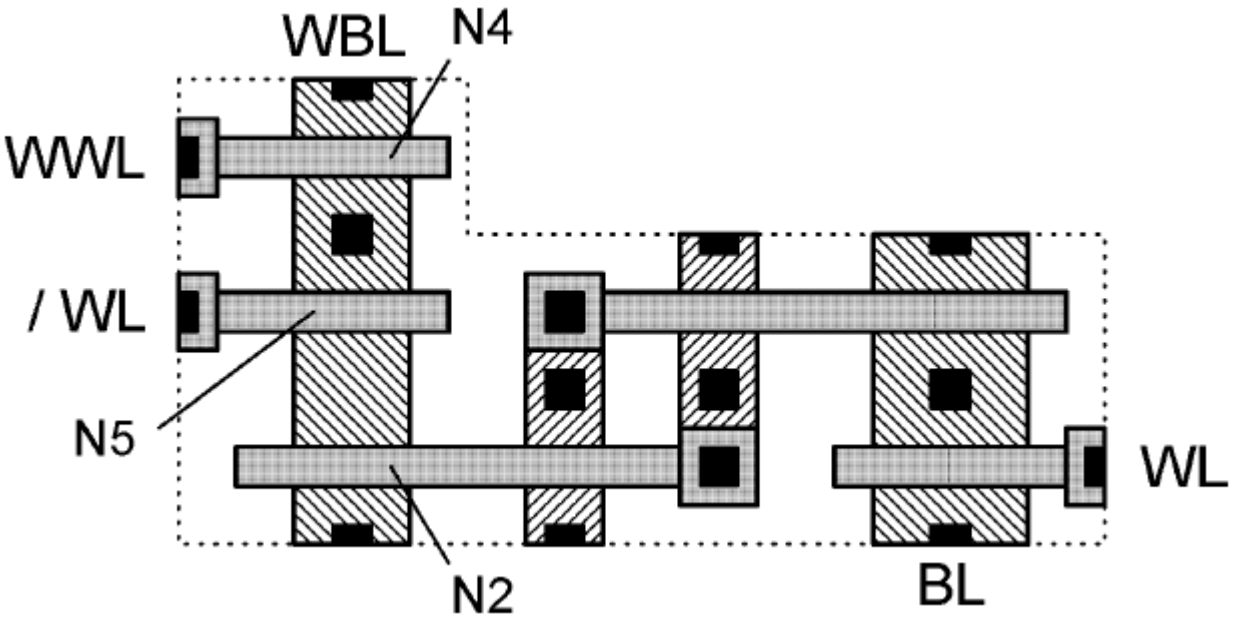
[Takeda, et. al., JSSC, Jan 2006]

Write Waveforms



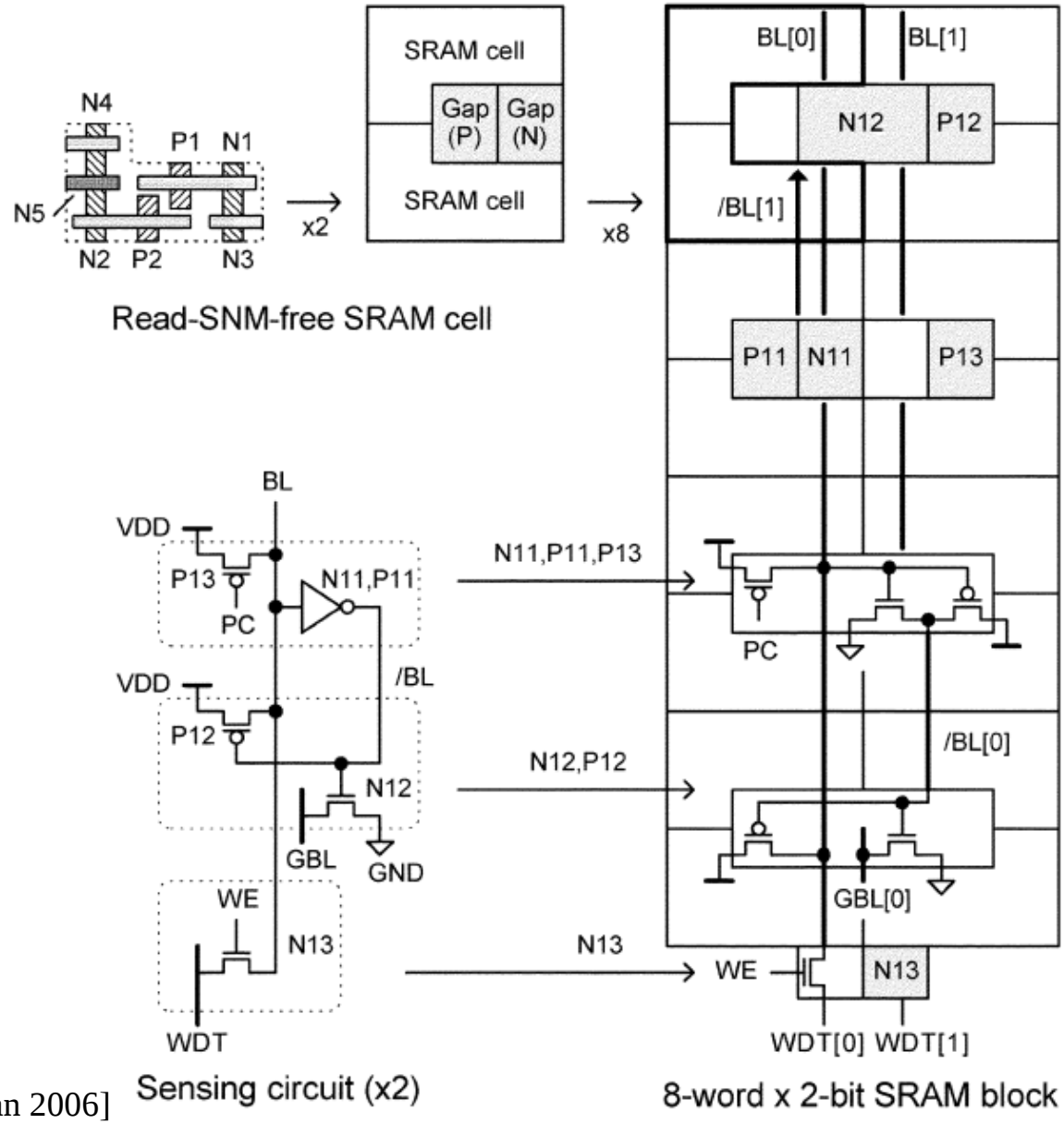
[Takeda, et. al., JSSC, Jan 2006]

7-T Cell Layout



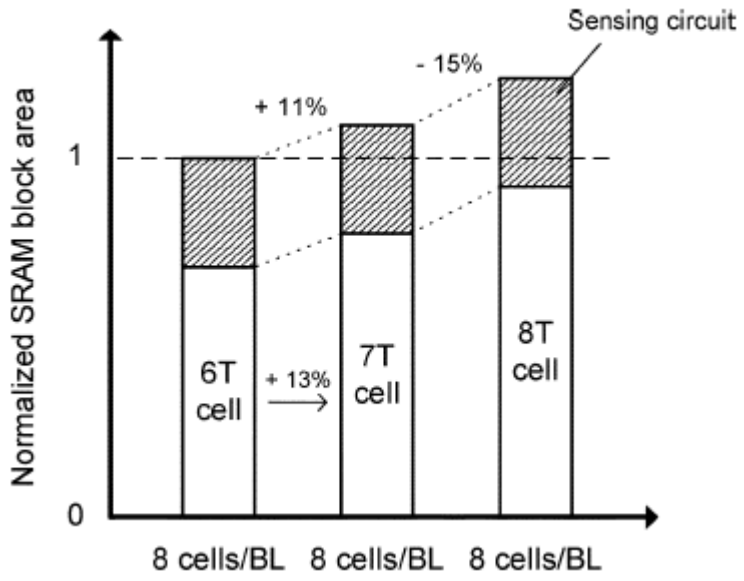
[Takeda, et. al., JSSC, Jan 2006]

Hiding gaps

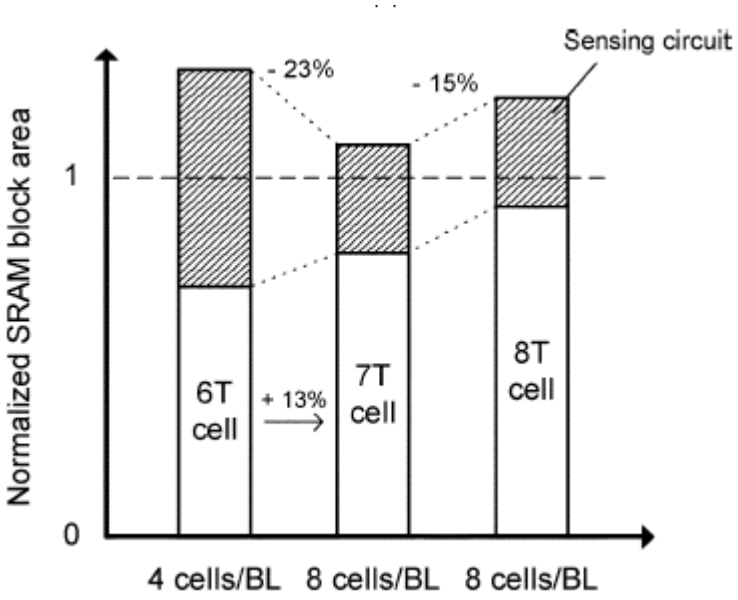


[Takeda, et. al., JSSC, Jan 2006]

Area overheads



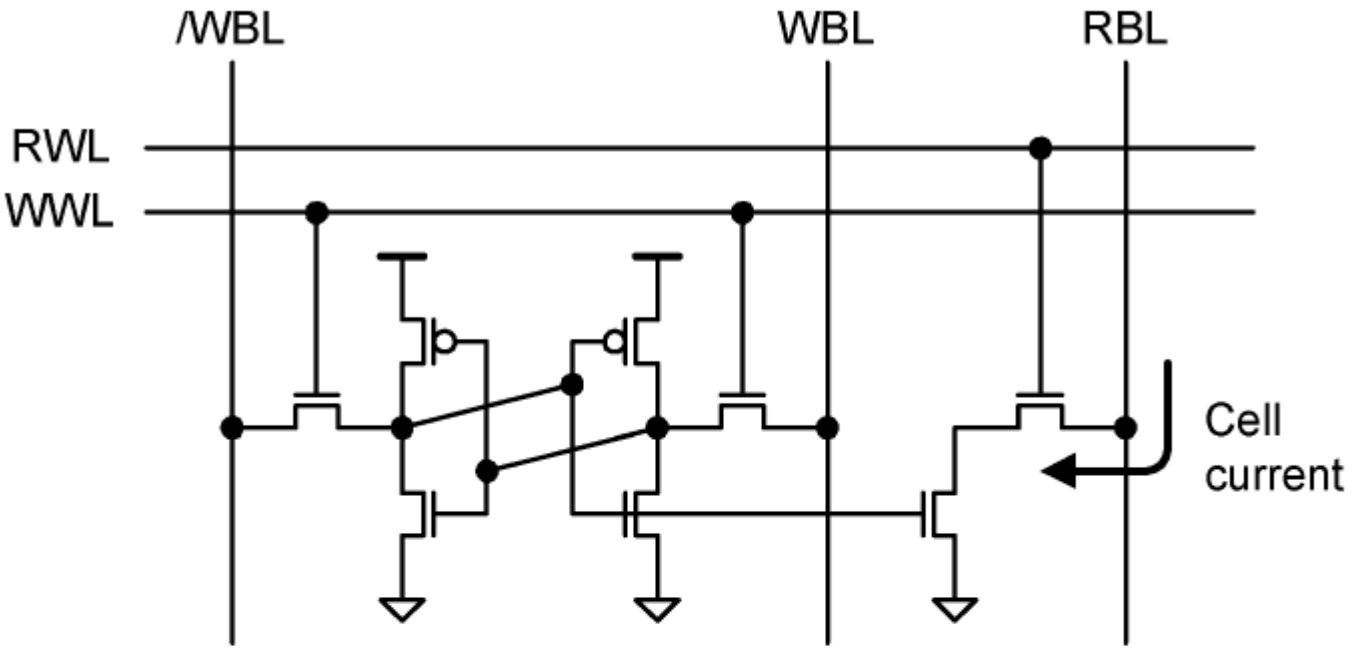
Same configuration



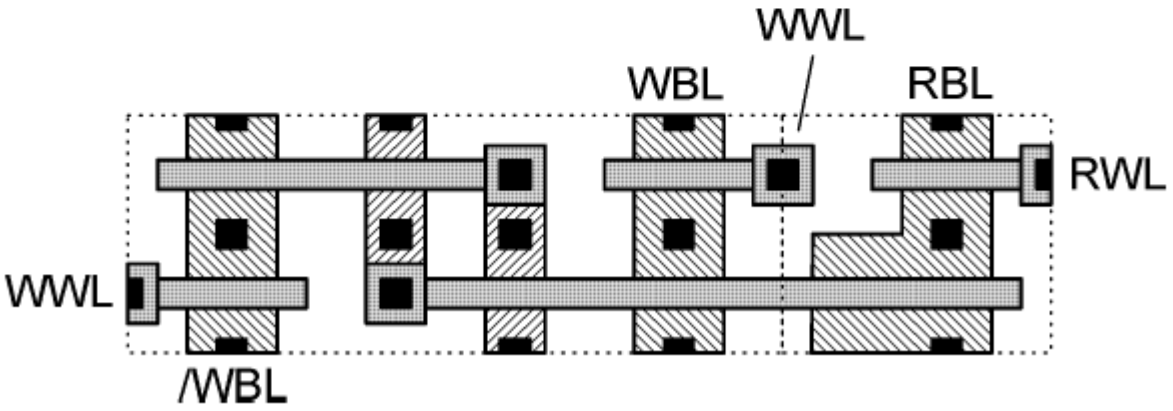
Same Speed

[Takeda, et. al., JSSC, Jan 2006]

8-T Cell



(a)



(b)

[Takeda, et. al., JSSC, Jan 2006]