Application Report
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Using PWM Output as a Digital-to-Analog Converter on a TMS320F280x Digital Signal Controller

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ABSTRACT

This application report presents a method for utilizing the on-chip pulse width modulated (PWM) signal generators on the TMS320F280x™ family of digital signal controllers as a digital-to-analog converter (DAC). The method involves analog low-pass filtering the PWM signal to remove high frequency components, leaving only the low-frequency content. Theoretical and experimental results are presented to quantify the achievable bit resolution and bandwidth, which depend upon the analog low-pass filter employed, the PWM frequency, and the DSP operating frequency. When coupled with a second order passive RLC filter, the hi-resolution PWM module on the TMS320F280x device is seen capable of providing greater than 9 bits of DAC resolution with 100 kHz bandwidth. Alternately, 50 kHz DAC bandwidth is possible with better than 10 bits of resolution. These resolutions and bandwidths make the PWM/DAC a legitimate lower cost alternative to dedicated off-chip DACs in TMS320F280x based systems.

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1 Introduction

The PWM signal outputs on a TMS320F280x[1] device are variable duty cycle square-waves with 3.3 volt amplitude. These signals can each be decomposed into a D.C. component plus a new square-wave of identical duty-cycle but with a time-average amplitude of zero. Figure 1 depicts this graphically. It will be shown in Section 2 that the amplitude of the D.C. component is directly proportional to the PWM duty cycle.

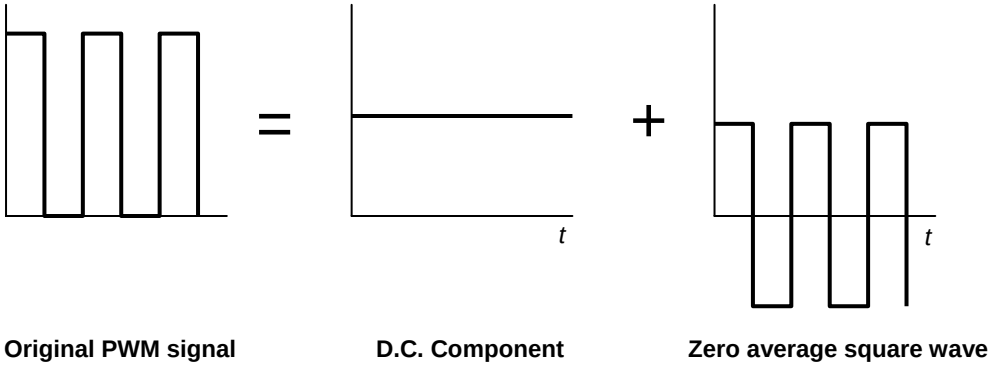

Figure 1. Decomposition of a PWM Signal

The idea behind realizing digital-to-analog (D/A) output from a PWM signal is to analog low-pass filter the PWM output to remove most of the high frequency components, ideally leaving only the D.C. component. This is depicted in Figure 2. The bandwidth of the low-pass filter will essentially determine the bandwidth of the digital-to-analog converter. A frequency analysis of the PWM signal is given in the next section in order to provide a theoretical basis for the filtering strategy.

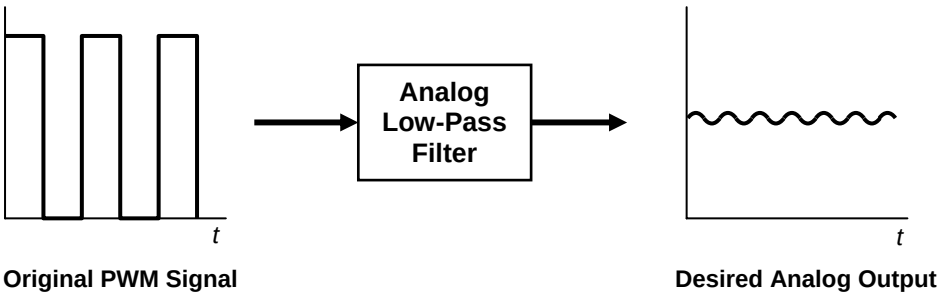

Figure 2. Analog Filtering of PWM Signal

[1] TMS320F280x will hereafter refer specifically to TMS320F2801, TMS320F2806, TMS320F2808, and UCD9501 devices.

The PWM/DAC approach is not new, but performance limitations have historically confined its use to low-resolution, low-bandwidth applications. The performance of the method relates directly to the ability of the low-pass filter to remove the high-frequency components of the PWM signal. Use a filter with too low a cut-off frequency, and DAC bandwidth suffers. Use a filter with too high a cut-off frequency or with slow stop-band rolloff, and DAC resolution suffers. These issues will be discussed in more detail later in this report, but one way to alleviate both of these problems is to increase the frequency of the PWM. However, as PWM frequency increases on conventional microprocessor generated PWM, digital resolution problems begin to manifest. It will be seen in this report that the hi-resolution PWM module (HRPWM) on the TMS320F280x family of digital signal controllers is able to overcome these performance limitations to a great extent and offer real-world useable DAC performance.

2 Frequency Analysis of the PWM Signal

Fourier theory states that any periodic waveform can be decomposed into an infinite sum of harmonics at integer multiple frequencies of the periodic frequency. Without loss of generality, the Fourier series representation of the PWM signal can be simplified by judiciously placing the time origin so that the signal becomes an even mathematical function, as shown in Figure 3.

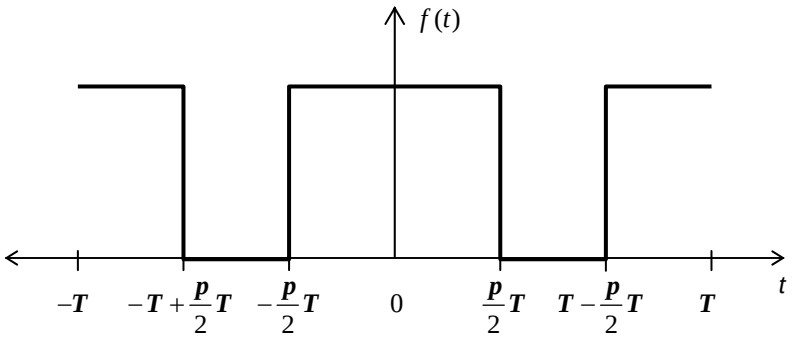

Figure 3. PWM Signal Time-Shifted for Even Symmetry

In Figure 3, p denotes the PWM duty cycle ($0 \le p \le 1$), and T denotes the carrier period in seconds. Note that a TMS320F280x controller can generate both asymmetric and symmetric PWM. This should not be confused with even symmetry, which is a mathematical property of a function. The signal depicted in Figure 3 applies equally well to either type of PWM.

The Fourier series representation of an even periodic function f(t) may be computed as follows (see reference [1]):

$$f(t) = A_0 + \sum_{n=1}^{\infty}\left[A_n \cos\left(\frac{2n\pi t}{T}\right) + B_n \sin\left(\frac{2n\pi t}{T}\right)\right] \quad (1)$$

where:

$$A_0 = \frac{1}{2T}\int_{-T}^{T} f(t)dt \quad (2)$$

$$A_n = \frac{1}{T}\int_{-T}^{T} f(t)\cos\left(\frac{2n\pi t}{T}\right)dt \quad (3)$$

$$B_n = \frac{1}{T}\int_{-T}^{T} f(t)\sin\left(\frac{2n\pi t}{T}\right)dt \quad (4)$$

Let K denote the amplitude of the signal f(t) in Figure 3. One obtains the following results after performing the integrals (2) - (4):

$$A_0 = K \cdot p \qquad A_n = K \cdot \frac{1}{n\pi}\left[\sin(n\pi p) - \sin(2n\pi(1-p/2))\right] \qquad B_n = 0 \quad (5)$$

The zero result for B_n is expected for an even function, and will not be discussed further here. The D.C. component A_0 is seen equal to the PWM amplitude multiplied by the PWM duty cycle. This is the desired D/A output. By selecting the proper duty cycle, any D/A output voltage can be obtained within the range 0 to K volts. The A_n terms represent the amplitudes of the high frequency harmonic components of the PWM signal, which are seen to exist at integer multiples of the PWM carrier frequency $2\pi/T$ (Hz). For example, when using 1 MHz PWM, the harmonics occur at 1 MHz, 2 MHz, 3 MHz, and so on. An ideal brick-wall low-pass filter with a cut-off at any frequency below the 1 MHz carrier frequency will completely remove the high frequency harmonics, leaving only the D.C. component. Additionally, it will allow the PWM duty cycle to be varied at frequencies up to the cut-off frequency and reflect this variation with a corresponding voltage level change in the D.C. output. Of course, one cannot build an ideal filter, and a real filter will always allow some portion of the harmonics to pass. This produces ripple in the desired output, as was illustrated in Figure 2.

3 D/A Resolution Issues

Two main sources of error affect the desired D/A output. First, the PWM duty cycle can only be specified with finite resolution. On the TMS320F280x, there are two components to this. The course resolution is directly related to the PWM carrier frequency used. For example, suppose 100 kHz PWM is desired with the PWM module driven by a 100 MHz CPU clock. The time-base of the PWM provides 1000 clock counts per cycle of PWM at which to specify the timer compare value and hence the duty cycle. When using the standard PWM on the TMS320F280x devices, this equates to just less than 10-bit resolution. In other words, the desired D.C. output can only be specified in steps of 3.3 mV (i.e. 3.3V/1000 counts). However, the enhanced PWM modules (ePWM) on the TMS320F280x devices offer a TI proprietary high-resolution PWM mode that provides approximately 6 additional bits of resolution beyond the standard time-base resolution (see reference [4]). In this example, that equates to ~16 bits of resolution.

The second source of error is the peak-to-peak ripple produced by unfiltered harmonics. The two error sources sum together to yield the total uncertainty:

total uncertainty = harmonic ripple + duty cycle resolution (6)

Figure 4 depicts the error sources and their summation graphically.

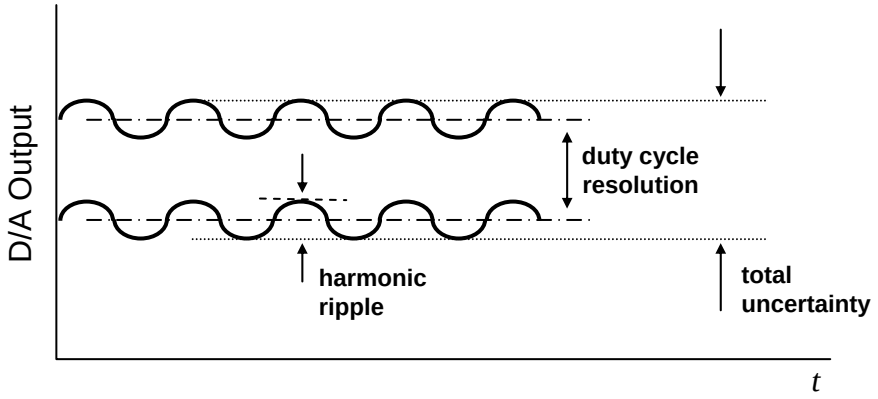

Figure 4. Total Uncertainty in the D/A Output

One approach for improving the duty cycle resolution is to decrease the carrier frequency of the PWM. In the previous example, reducing the carrier frequency to 50 kHz from 100 kHz cuts the step size in half to 1.65 mV (i.e. ~11 bits resolution in standard resolution PWM mode, ~17 bits resolution in high resolution PWM mode). However, the lower carrier frequency also decreases the base frequency of the unwanted harmonics in equation (1). In particular, the first harmonic will now appear at 50 kHz rather than 100 kHz, and more of it will pass through the analog low-pass filter, thereby increasing the harmonic ripple.

Methods for reducing the harmonic ripple involve modifying the analog low-pass filter to increase the stop-band roll-off (i.e., a higher order filter) or to decrease the pass-band cut-off frequency. Both of these methods have drawbacks however. Increasing the stop-band roll-off generally means a more complex analog filter circuit, and correspondingly a higher cost. Alternately, decreasing the pass-band cut-off frequency also decreases the bandwidth of the DAC. In other words, the DAC is limited in bandwidth by the bandwidth of the analog low-pass filter.

For a given analog low-pass filter, it is clear that a trade-off exists between harmonic ripple and PWM duty cycle resolution when selecting the PWM carrier frequency. The optimal carrier frequency is the one where the total uncertainty is smallest.

4 Analog Low-Pass Filters

The performance of filtered PWM as a digital-to-analog converter depends heavily on the choice of the analog low-pass filter. When one thinks of filter performance, they tend to think of active filters (built using op-amps) rather than passive filters (composed solely of resistors, inductors, and capacitors). Active filters avoid the impedance loading issues suffered by passive filters, where the upstream or downstream impedances surrounding the filter can change the filter properties. Passive filters can offer lower cost and reduced design complexity.

With active filters, one must also consider the gain bandwidth of the op-amps used. The gain bandwidth represents the upper frequency that the op-amp can effectively handle when used in a closed-loop circuit configuration with small signal input. In terms of active low-pass filters, input signal components with frequency above the gain bandwidth will be attenuated since the op-amp will not have the ability to handle such frequencies. As a practical matter, it is desirable to use an op-amp with gain bandwidth at least 5 to 10 times greater than the highest expected input frequency so that the gain bandwidth of the op-amp does not influence the circuit. In other words, if you design a filter to have particular low-pass specifications, you do not want the

limitations of the op-amp changing your design. In addition, the gain bandwidth of a particular op-amp can vary greatly from device to device, giving unpredictable filter performance from system to system). As will be seen in Section 5, PWM frequencies above 1 MHz are not uncommon in the PWM/DAC application. Op-amps with sufficient gain bandwidth to handle these frequencies are relatively expensive, and at some point one may as well just use an actual DAC chip!

Passive filters do not suffer as much from a gain bandwidth problem, although they do have their own high-frequency design issues (especially inductors). The biggest drawback of passive filters has always been impedance related: upstream and downstream impedances can affect the performance properties of the filter. In the PWM/DAC application, upstream of the filter will be the PWM output from the DSP. This is a low output-impedance source that will not significantly affect the filter. In the downstream direction, one can use a low-cost voltage follower op-amp to create a high-impedance input. Since the op-amp is in the signal chain after the low-pass filter, an op-amp with large gain bandwidth is not needed.

A nearly endless supply of textbooks exist that provide a complete treatment on the subject of analog filters. Any undergraduate textbook on signal processing is likely to contain a full theoretical analysis of 1st and 2nd order linear time-invariant filters, including the frequency response of the filter and the time-domain response to a step input. In addition, any basic circuit design textbook will contain standard circuits for building different filters, both passive and active. Only a brief review will be presented here to highlight the design properties of the filters that are relevant to this application report.

Two important filter properties in the PWM/DAC application are the bandwidth and the stop-band rolloff rate. The filter bandwidth is defined as the frequency at which the filter frequency response magnitude equals 0.707 (i.e., -3 dB). The filter bandwidth directly relates to the maximum signal frequency that the PWM/DAC will effectively handle. The stop-band rolloff rate is the slope of the frequency response magnitude at high frequency. Combined with the bandwidth, the rolloff rate determines the amount of harmonic ripple that will be seen in the output of the filter. In general, low-pass analog filters rolloff at a rate of -20 dB/decade per filter order (e.g., -20 dB/decade for a 1st order filter, -40 dB/decade for a 2nd order filter, etc.).

4.1 1st Order Low-Pass Filter

The continuous-time domain transfer function for a 1st order filter is given by the equation

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{\tau s + 1} \tag{7}$$

where the time constant τ is in units of seconds. It is straightforward to show that the filter bandwidth is

$$BW = \frac{1}{\tau} \quad \text{(rad/s)} \tag{8}$$

A passive 1st order low-pass filter may be constructed from a single resistor and capacitor, as shown in Figure 5.

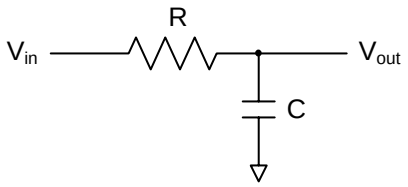

Figure 5. 1st Order Passive Low-Pass Filter Circuit

Simple circuit analysis shows the time constant to be τ = RC, and therefore from equation (8) the filter bandwidth is BW = 1/RC (rad/s).

The passive RC filter offers the advantages of simplicity and low cost, as the price is nothing more than that of a resistor and a capacitor. However, the stop-band rolloff rate is a sluggish 20 dB/decade, giving the 1st order filter less than desirable performance in the PWM/DAC application.

4.2 2nd Order Low-Pass Filter

The 2nd-order low-pass filter offers 40 dB/decade of stop-band rolloff, which is a two-fold improvement over the 1st order filter. The transfer function is given by the equation

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{9}$$

where ω_n is the undamped natural frequency in units of $(rad/s)^2$, and ζ is the non-dimensional damping ratio. It is straightforward to show that the filter bandwidth is

$$BW = \omega_n \left[\left(1 - 2\zeta^2\right) + \sqrt{4\zeta^4 - 4\zeta^2 + 2} \right]^{1/2} \tag{10}$$

The step response of the filter is an important measure of performance for the practical situation of changing the DAC output from one voltage level to another. In terms of step response rise time, it is desirable to use as low a damping ratio as possible in order to have fast rise times. However, low damping ratios produce large step response overshoots and long settling times. The smallest damping ratio with no overshoot in the step response is ζ=1, and such a system is called critically damped. It is also desirable to avoid having a resonant peak in the frequency response magnitude of the filter. The smallest damping ratio with no resonant peak is ζ=0.707 (i.e., $2^{-1/2}$). The choice of damping ratio will depend on the particular requirements of your system. A reasonable trade-off is often to choose the filter damping ratio between 0.707 and 1.0. Note that when ζ = 0.707, the bandwidth in equation (10) is equal to ω_n.

A passive 2nd order RC filter can be constructed by cascading two 1st order RC filters in series.

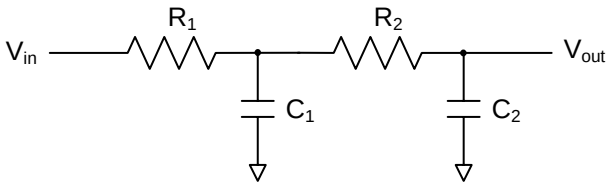

Figure 6. 2nd Order Passive RC Low-Pass Filter Circuit

Simple circuit analysis shows the transfer function parameters in equation (9) to be:

$$\omega_n = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \qquad \text{and} \qquad \zeta = \frac{\left(R_1 C_1 + R_1 C_2 + R_2 C_2\right)}{2\sqrt{R_1 R_2 C_1 C_2}} \tag{11}$$

Due to the arrangement of components in the circuit, it turns out that the 2nd-order passive RC filter is unable to realize damping ratios less than 1. The passive RLC filter shown in Figure 7 offers such flexibility.

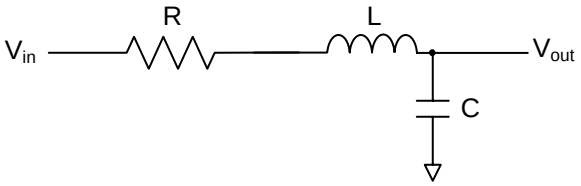

Figure 7. 2nd Order Passive RLC Low-Pass Filter Circuit

Simple circuit analysis of the passive RLC filter shows the transfer function parameters in equation (9) to be:

$$\omega_n = \frac{1}{\sqrt{LC}} \qquad \text{and} \qquad \zeta = \frac{R}{2} \cdot \sqrt{\frac{C}{L}} \tag{12}$$

Inductors have traditionally been shunned in instrumentation and control circuits due to their relatively large physical size, expense, and deviation from the ideal mathematical model. However, their use in the present low-pass filter application is reasonable since only a single inductor is needed to build a second order low-pass filter, and the tolerance of the application to component model and value variation is fairly high. In other words, it is not important in the PWM/DAC application to build a filter with exact bandwidth.

4.3 Higher Order Low-Pass Filters

Higher order filters offer progressively better stop-band rolloff rates, and hence remove more of the unwanted ripple in equation (6). However, design complexities associated with thermal drift and component value variation increase with filter order. Cost and board space consumption also increases. At some point, an actual DAC chip becomes a better solution.

5 Simulation of D/A Performance

While the duty cycle resolution is easy to compute for a given carrier frequency, analytically quantifying the harmonic ripple is considerably more difficult (if not impossible) due to the infinite summation in equation (1). Therefore, simulation using MATLAB/Simulink™ was used to determine the steady-state ripple of various low-pass filters, with equation (6) then applied to determine the total DAC resolution. For purposes of this study, the high-resolution mode PWM was assumed to provide 6 additional bits of duty cycle resolution. In addition, the value p = 0.5 (from Figure 3) was used in the simulations since this value maximizes the energy of the n=1 harmonic (see Appendix A). This harmonic is the most troublesome, since the energy in higher harmonics decreases as a function of $1/n^2$ regardless of the duty cycle.

Seven different filters were simulated. Table 1 shows the filter parameters, and Figures 8 and 9 show the filter frequency responses. The phase response of the filter should be considered in addition to magnitude when designing a closed-loop control system or when otherwise analyzing the filter outputs (i.e. the DAC output) since the frequency components of the output signal will each be phase delayed by a different amount, and hence distortion of the signal can occur. Higher order filters offer superior magnitude response at the expense of increased phase delay.

Figures 10 through 16 show the achievable D/A resolution for each low-pass filter for selected CPU clock speeds [2]. Each figure clearly shows the trade-off between harmonic ripple and PWM duty-cycle resolution that one occurs when selecting the PWM frequency. At low PWM frequencies, the harmonic ripple heavily dominates the total resolution, and hence the D/A resolution converges to the same value regardless of the CPU frequency. At high PWM frequencies, the duty cycle resolution dominates and the D/A resolution becomes independent of which low-pass filter is used. The peak of each curve represents the PWM frequency where the trade-off between harmonic ripple and PWM duty-cycle maximizes the D/A resolution.

Table 1. Filter Parameters used in Simulation Study

Filter #	Order	Bandwidth (kHz)	ζ	ω_n (rad/s)
1	1st	10	-	-
2	1st	20	-	-
3	2nd	20	0.707	125664
4	2nd	50	0.707	314159
5	2nd	100	0.707	628319
6	2nd	100	1.0	976011
7†	4th	100	ζ_1 = 0.707 ζ_2 = 0.707	ω_{n1} = 782885 ω_{n2} = 782885

† Filter #7 is the series cascade of two 2nd order filters.

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[2] The 150 MHz clock speed is representative of Texas Instruments TMS320F2812, TMS320F2811, and TMS320F2810 devices. TMS320F280x devices (e.g., F2808, F2806, F2801, etc.) operate at a maximum clock of 100 MHz.

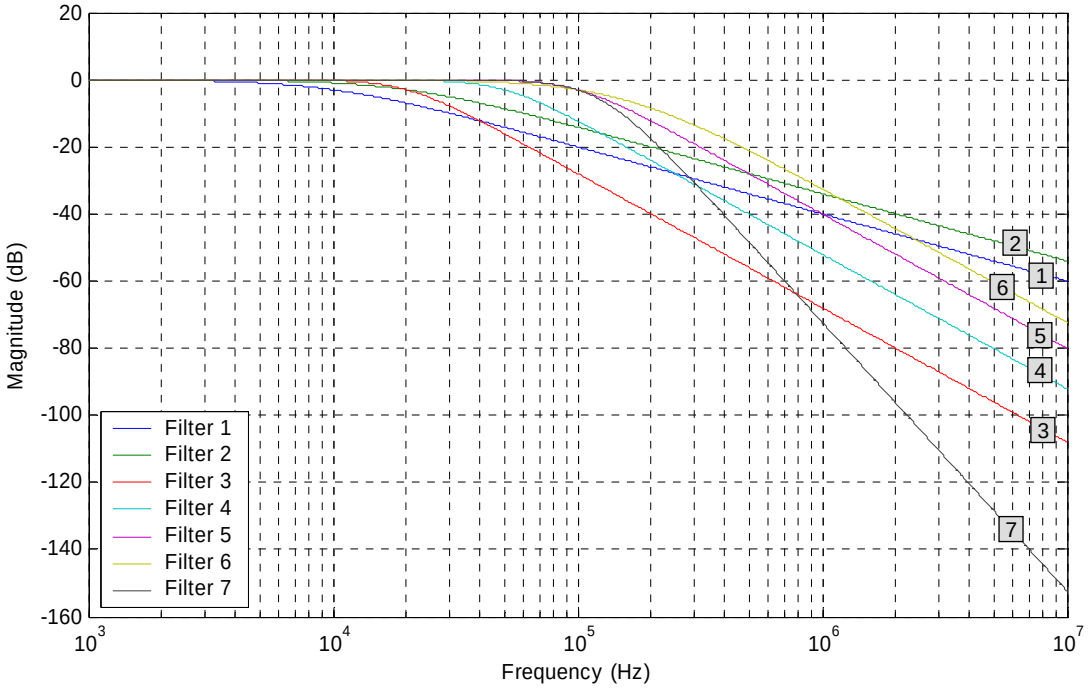

Figure 8. Magnitude Response of the Analog Low-Pass Filters

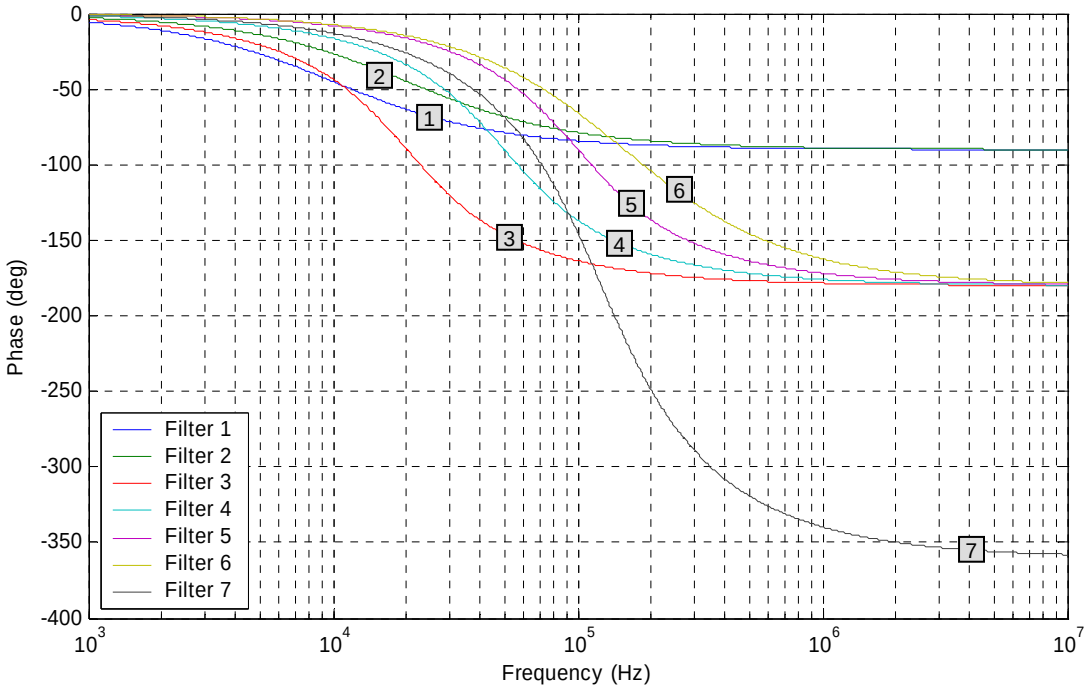

Figure 9. Phase Response of Analog Low-Pass Filters

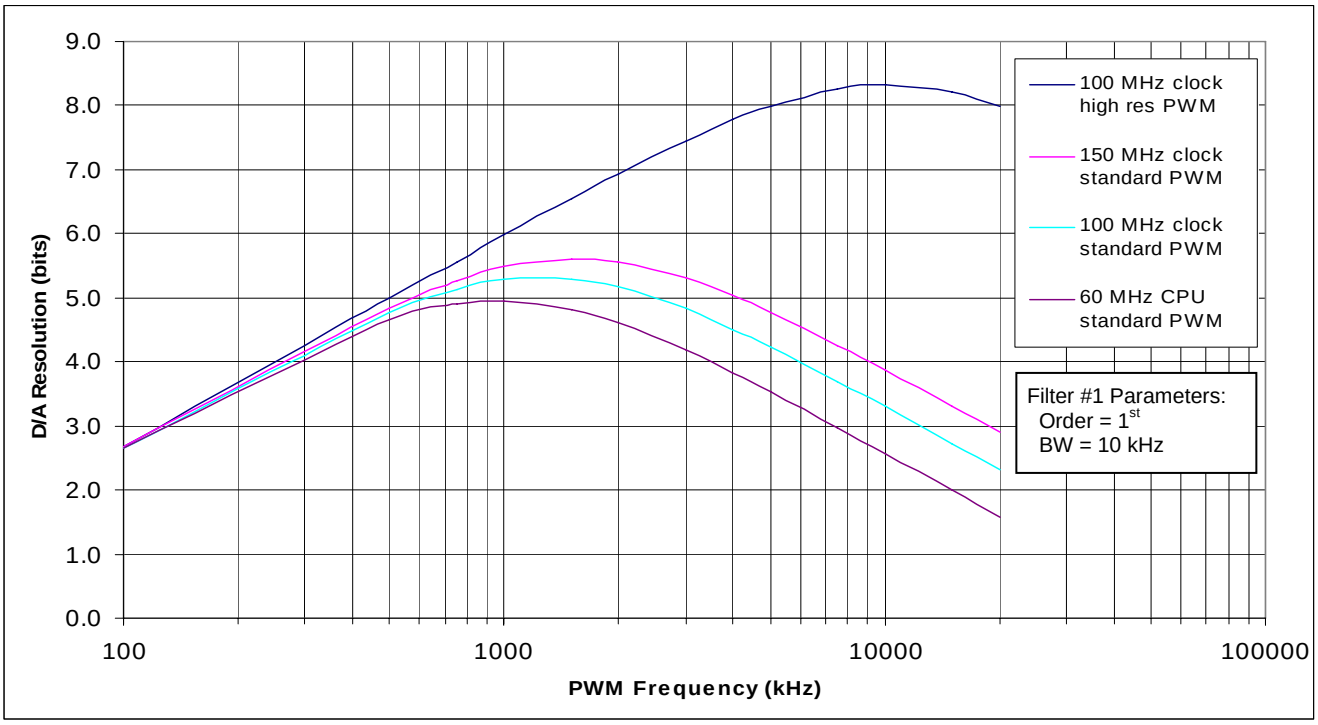

Figure 10. D/A Resolution vs. PWM Frequency, Filter #1 (from Simulation)

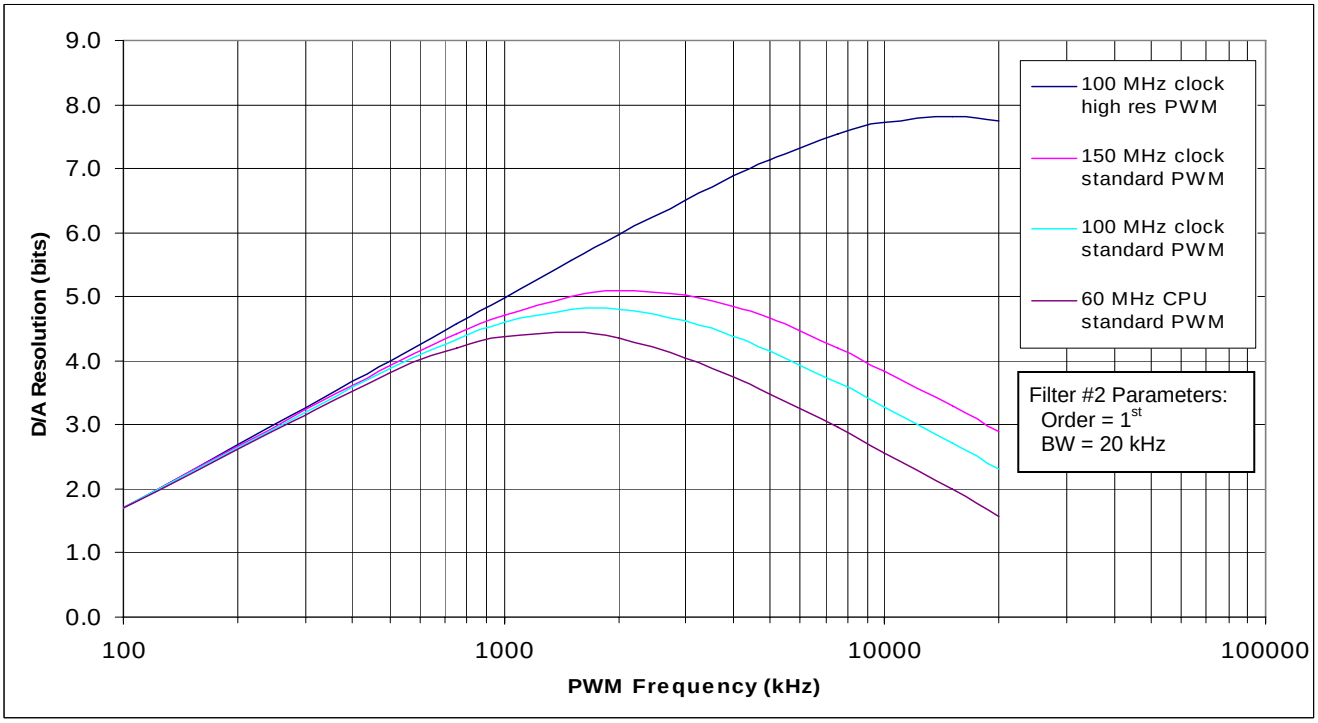

Figure 11. D/A Resolution vs. PWM Frequency, Filter #2 (from Simulation)

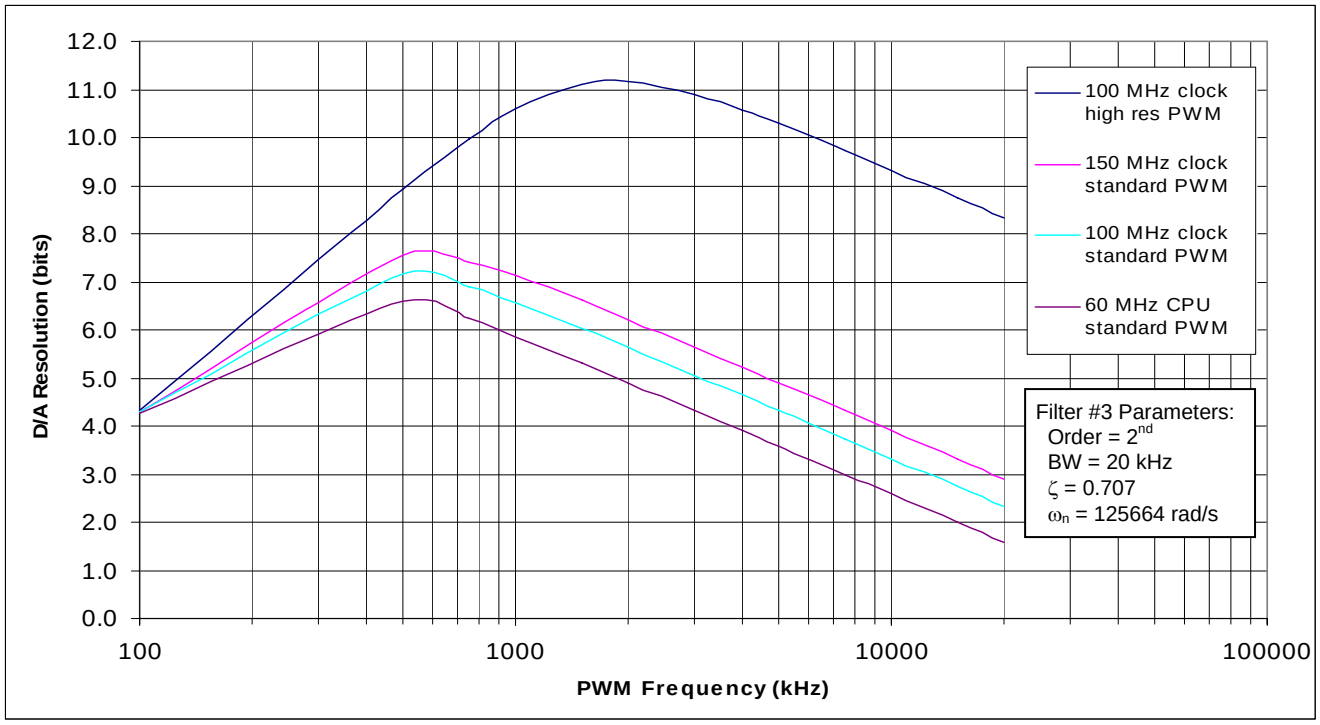

Figure 12. D/A Resolution vs. PWM Frequency, Filter #3 (from Simulation)

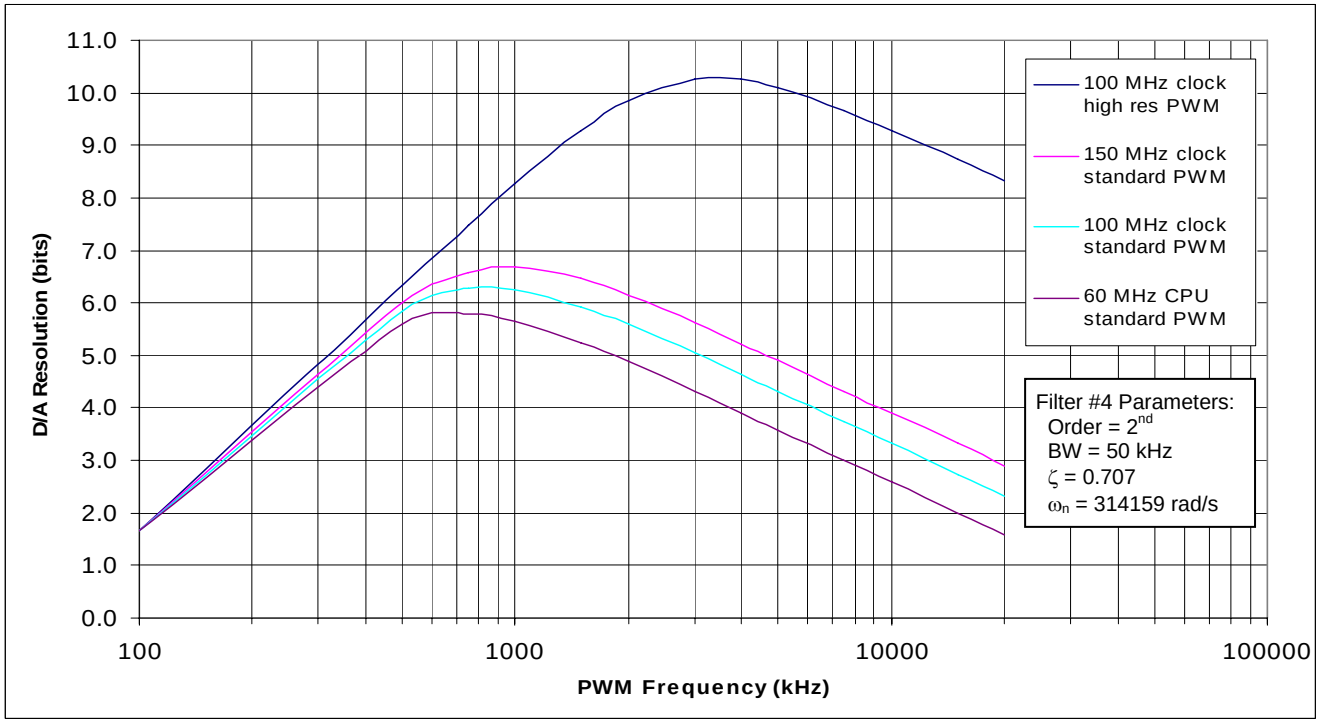

Figure 13. D/A Resolution vs. PWM Frequency, Filter #4 (from Simulation)

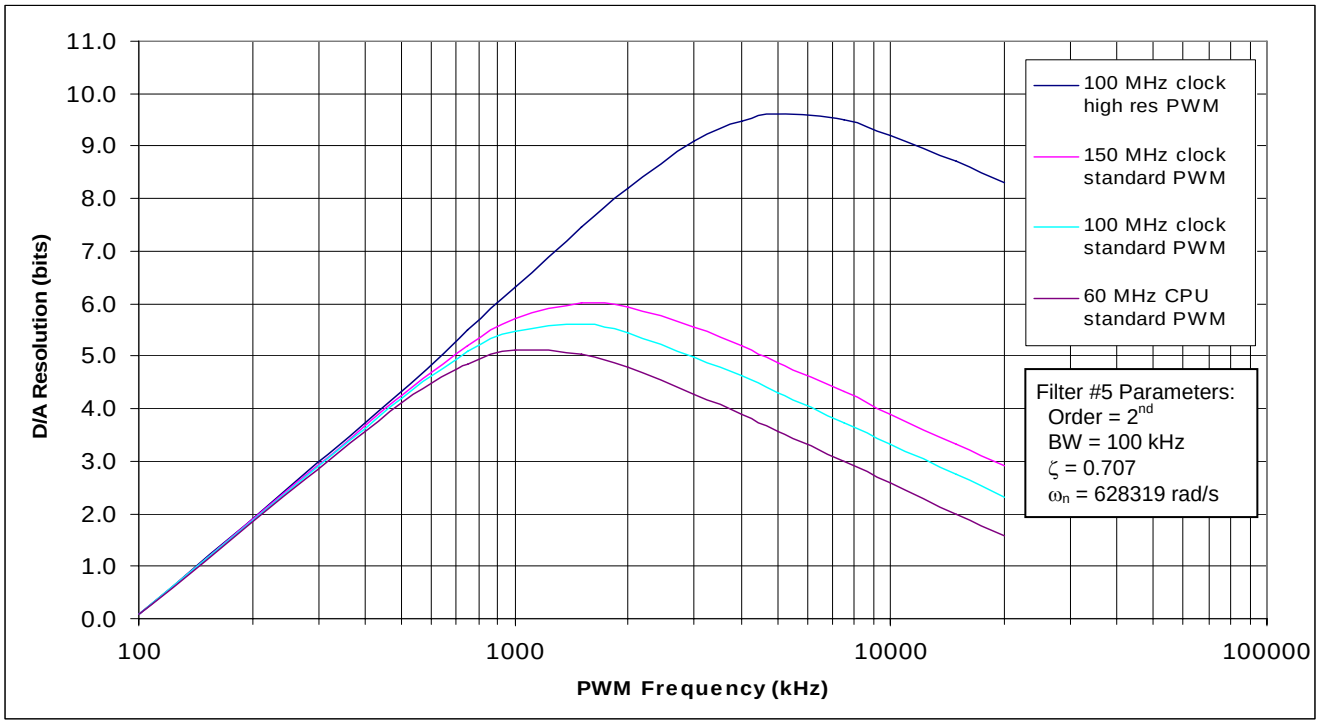

Figure 14. D/A Resolution vs. PWM Frequency, Filter #5 (from Simulation)

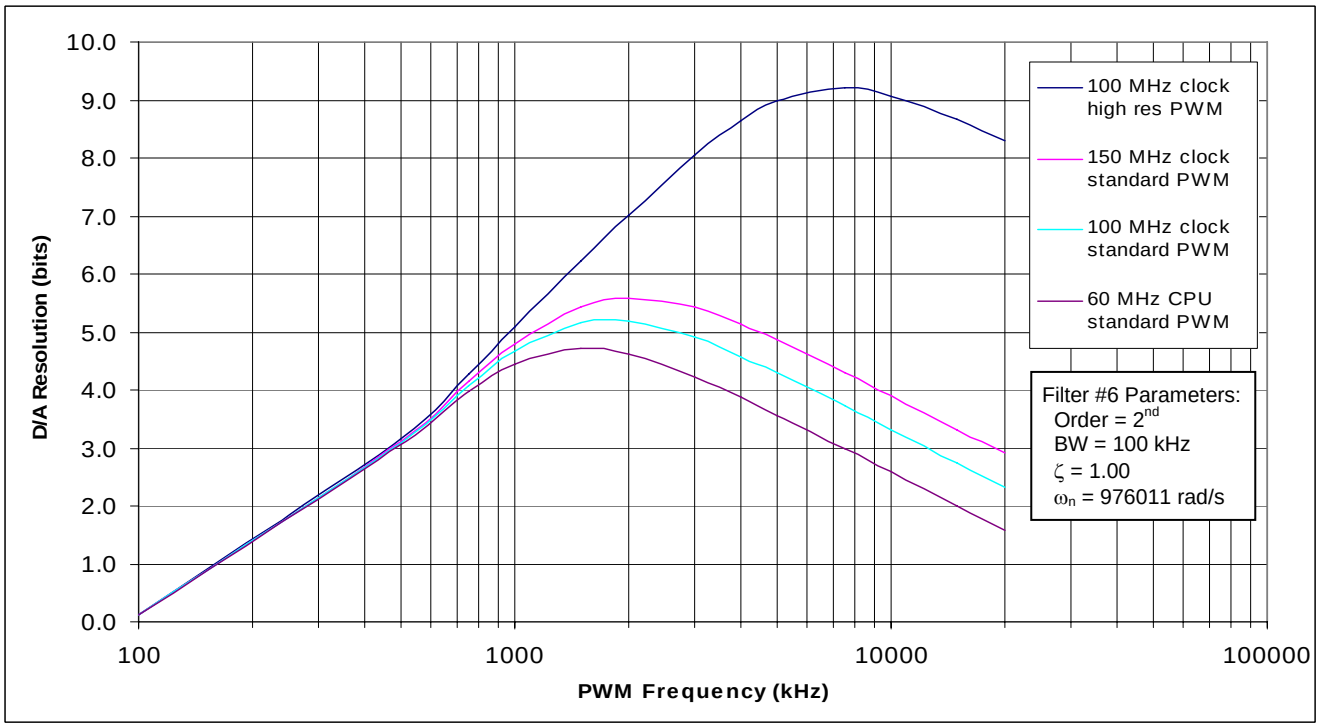

Figure 15. D/A Resolution vs. PWM Frequency, Filter #6 (from Simulation)

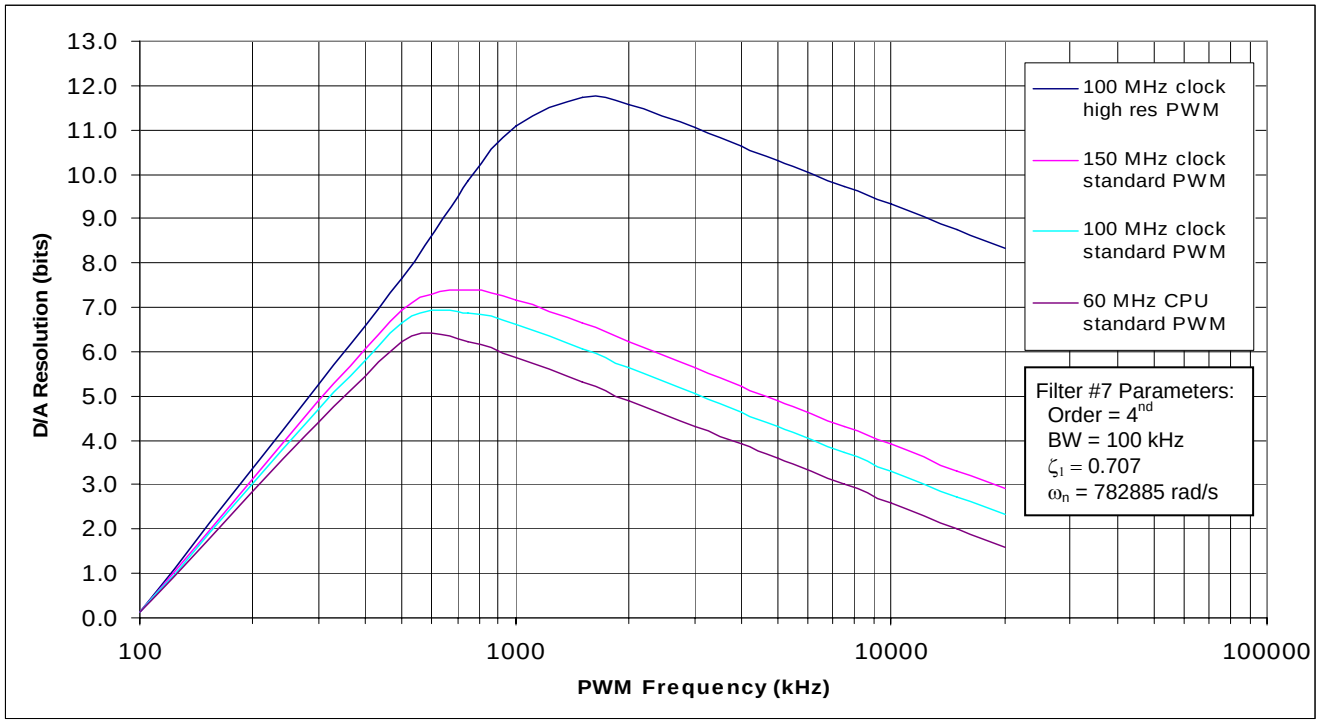

Figure 16. D/A Resolution vs. PWM Frequency, Filter #7 (from Simulation)

6 Experimental Setup and Results

Experimentation was performed to evaluate the performance of Filter #5. This filter was implemented using the RLC circuit of Figure 7 with the following component values: [3]

R = 91 Ω L = 100 μH C = 0.022 μF

Applying these values to equation (12), the transfer function parameters are seen to be:

$\omega_n = 674200\,\text{rad/s}$ (107.3 kHz) and $\zeta = 0.675$

These are close to the Filter #5 parameters given in Table 1, and can be considered equivalent from a practical viewpoint. The eZdspF2808™ development board served as the DSP platform with a 100 MHz CPU clock. Per Figure 14, the PWM frequency was chosen as 5 MHz since that frequency gives the best D/A resolution for Filter #5 using hi-resolution PWM at 100 MHz CPU clock. The PWM amplitude was 3.3V, as directly output from the DSP chip.

6.1 Sinusoidal Output Results

The DSP was configured to output a sine wave on the PWM/DAC. To do this, a timer interrupt was setup at a 250 kHz rate, with the PWM compare value updated at each interrupt using a 256 point full sine look-up table. This produces a 976.6 Hz sine wave (i.e., 250 kHz / 256). Figure 17 shows the superimposed scope traces of the D/A output using the hi-resolution and standard resolution PWM modes. Whereas the hi-resolution PWM produces a smooth signal output, the resolution limitations of the standard resolution PWM are clearly visible in the stepped output signal[4]. In addition, the hi-resolution PWM curve shows the correct sine wave maximum and minimum peak voltages (2.5V and 0.5V respectively), whereas the standard resolution PWM curve does not (2.68V and 0.68V respectively, as measured on the scope) due to PWM resolution issues.

[3] The PWM pin output impedance was seen to be roughly 61 Ω such that a 30 Ω resistor was used to construct the actual low-pass filter circuit.

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[4] The utilized 5 MHz is not the optimal PWM frequency for standard resolution PWM with a 100 MHz CPU clock, per Figure 14. The smoothness of the standard resolution curve in Figure 17 could be improved slightly by lowering the PWM frequency to ~1.5 MHz. However, the affect of the PWM resolution on the signal would still be visible as the lower PWM frequency would only add one additional bit of D/A resolution.

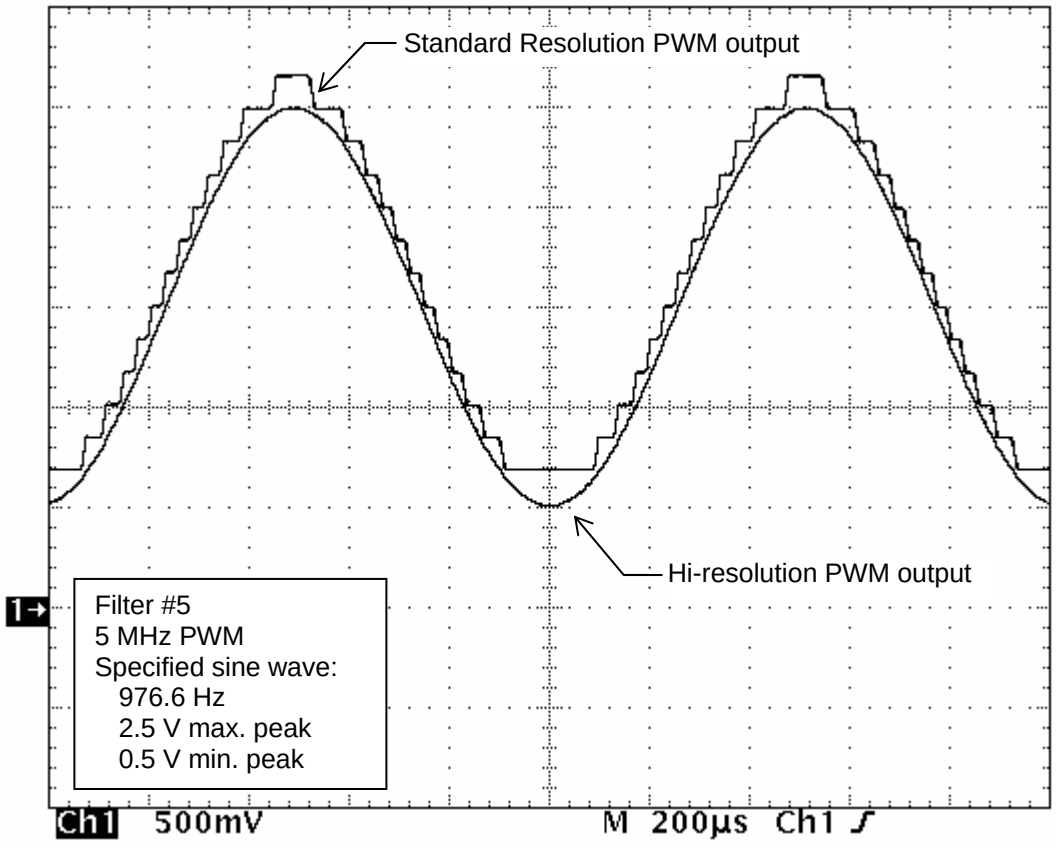

Figure 17. Filter #5 Output of PWM Sine Wave

6.2 Step Response Results

Figure 18 shows the experimental step response of Filter #5. The graph shows the standard 10% to 90% rise time as being 3.0 μsec. As a more practical performance measure, the combined rise and settling time from 0% to ~100% is roughly 10 μsec. The experimental step response matches well with the theoretical response from simulation shown in Figure 19. The simulation results show a 3.04 μsec 10% - 90% rise time.

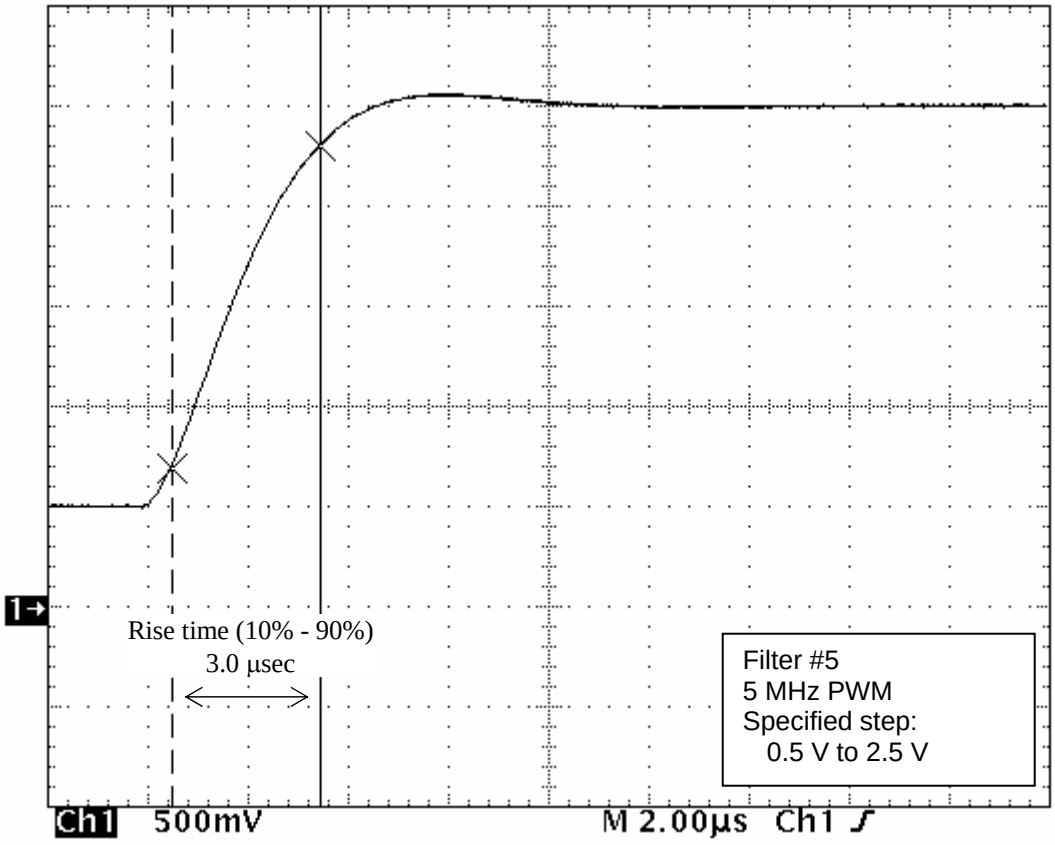

Figure 18. Filter #5 Step Response

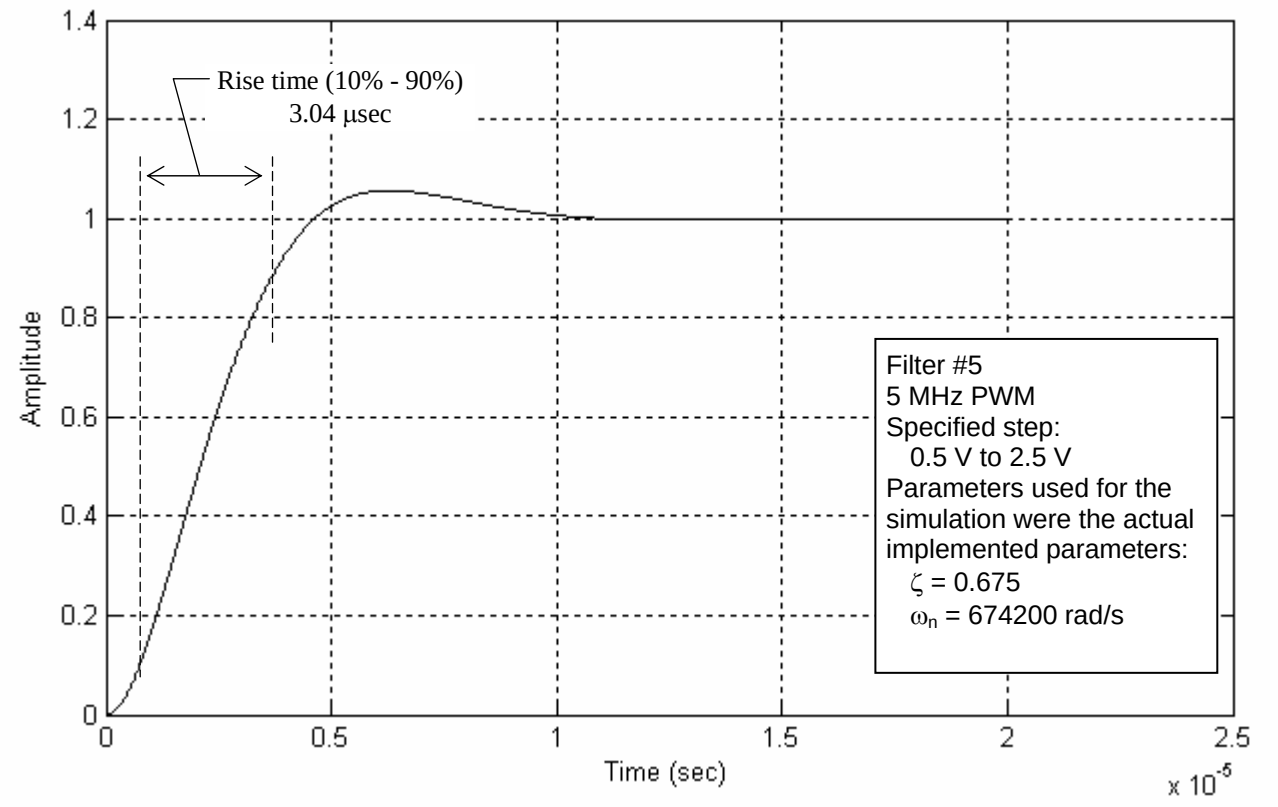

Figure 19. Theoretical Filter #5 Unit Step Response (from Simulation)

7 Additional Issues and Possibilities

7.1 HRPWM Duty Cycle Range Limitation on the TMS320F280x

HRPWM limitations exist in TMS320F280x devices near 0% and 100% duty (see reference [4]). Specifically, the HRPWM output reverts to that of standard PWM during the first three and the last two SYSCLKOUT cycles of the PWM period. These two limitations manifest themselves as a loss of resolution at the upper and lower ends of the D/A output range, as can be seen in Figure 20.

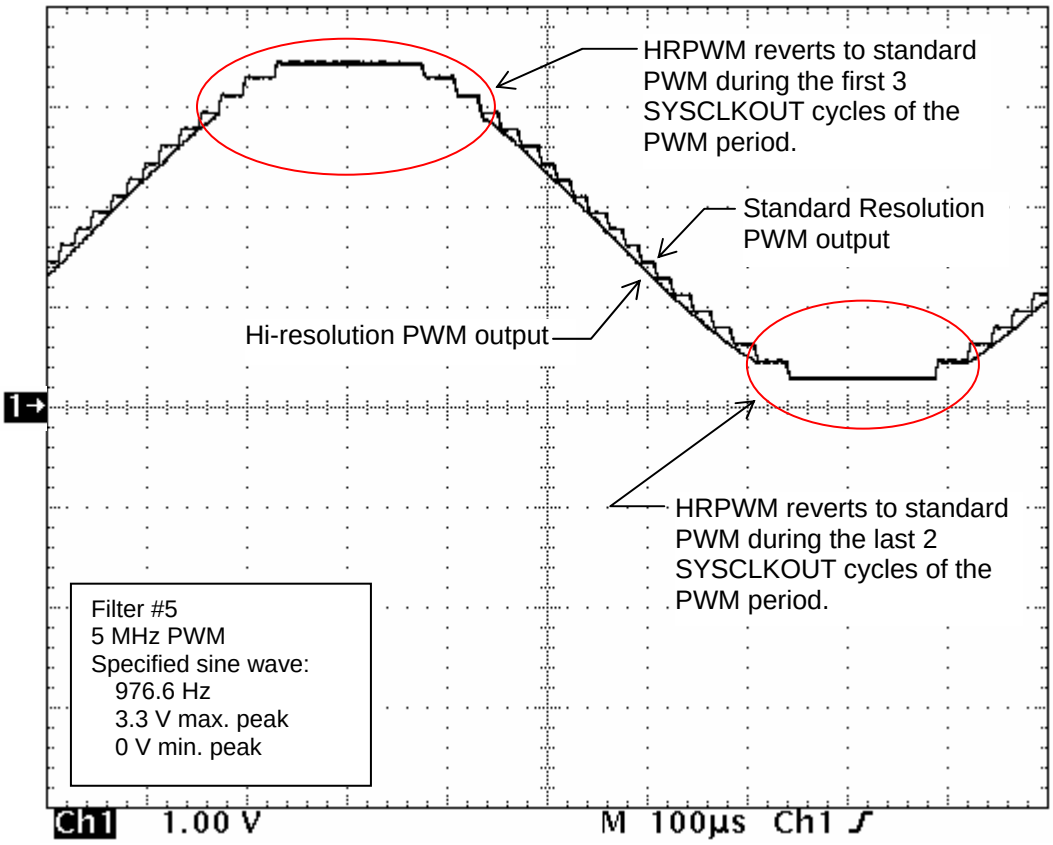

Figure 20. Filter #5 Output of PWM Sine Wave Showing Range Limits

To avoid this problem, one can simply limit, in software, the maximum duty cycle of the PWM such that the turn-on point is at least 3 SYSCLKOUT cycles from the beginning of the PWM period, and no more than 2 SYSCLKOUT cycles from the end of the PWM period. This will reduce the full-scale range of the D/A by a small amount that is a function of the carrier frequency of the PWM. For example, with 5 MHz PWM, the upper-end DAC output reduction is 3 parts (i.e., 3 SYSCLKOUT cycles) out of 20 (number of SYSCLKOUT cycles in a PWM period), or 15% of the upper limit. Therefore, the HRPWM will become inactive at 85% of the 3.3 volt full-scale range, which is 2.8 volts. One can see in Figure 20 that the HRPWM does in fact become inactive when the sine wave exceeds 2.8 volts. On the lower end of the DAC output range, the reduction is 2 parts out of 20, or 10%. Therefore, the HRPWM will become inactive below 10% of the 3.3 volt full-scale range, which is 0.33 volts. Figure 21 shows the effective full-scale range of the PWM/DAC for different PWM frequencies after accounting for the duty cycle range limitations.

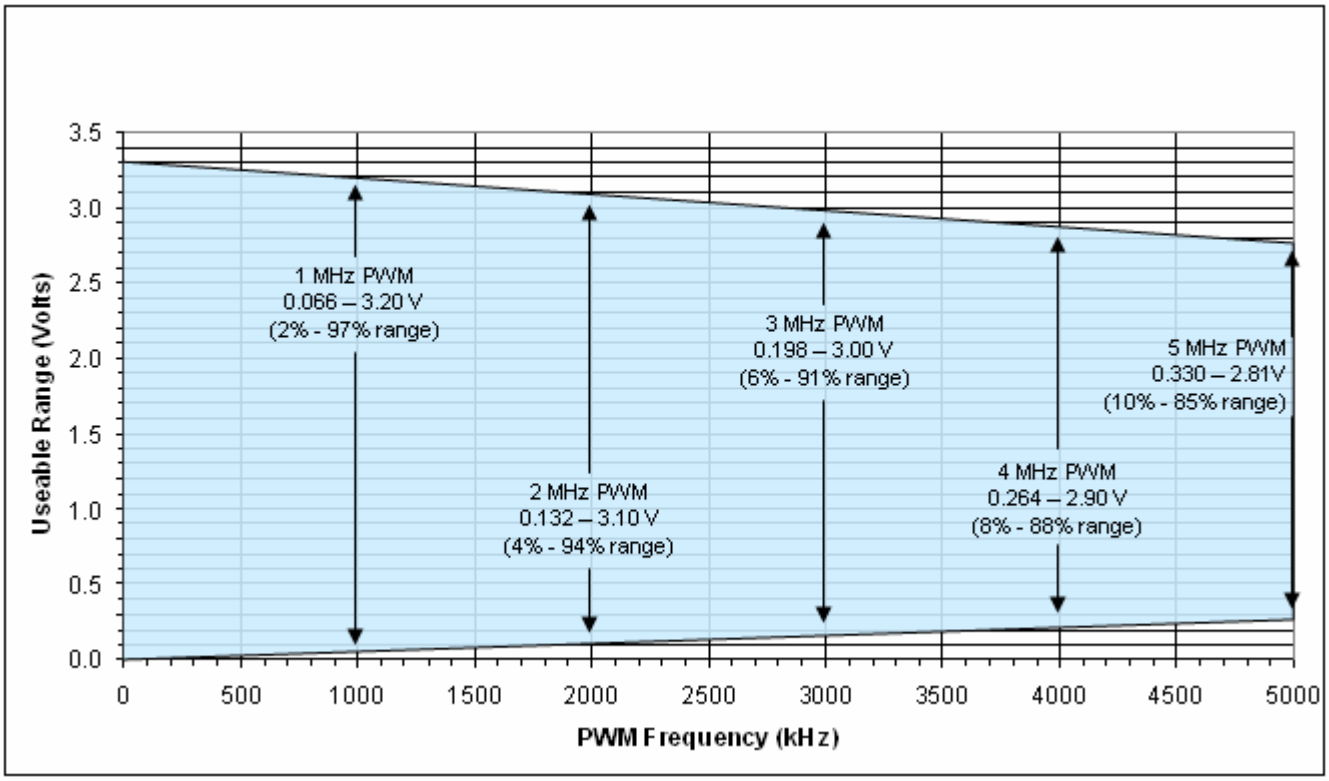

Figure 21. Effective Full-Scale D/A Range using HRPWM module

7.2 Calibration

The on-chip 12-bit analog-to-digital converter (ADC) in TMS320F280x devices provides a very convenient means of calibrating the PWM/DAC. In particular, the design of the HRPWM module introduces a small amount of offset error into the PWM/DAC output. By using the ADC to read back the PWM/DAC output at the lower end of the effective full-scale range output, the offset error is readily determined. The TMS320F280x software can then be modified to compensate for the offset. Gain error could be compensated for by taking a second reading near the upper end of the effective full-scale range and performing the necessary computations. Note however that it is unlikely that significant gain error would exist since the presented PWM/DAC contains no analog amplifiers. However, if a buffer amp were used on the output of the PWM/DAC to, for example, decrease the output impedance of the circuit, one could compensate for the gain (and offset) error of this amp as described.

8 C-Code Example

8.1 General Overview

A code download containing a simple PWM/DAC example for TMS320F280x devices accompanies this application report. This is the same code used in Section 6 to obtain the presented experimental results. The code was developed on the eZdspF2808 development board, but will run on any TMS320F2801, TMS320F2802, TMS320F2806, TMS320F2808, TMS320F2809, TMS320F28015, or TMS320F28016 device platform. The code will also likely run on future TMS320F280x family devices, although the user should be careful of potential device differences. The development tools were Code Composer Studio™ v3.3.80.11 with the C28x C-Compiler v5.0.2.

Figure 22 shows the basic flow of the example code. The code consists of a single interrupt loop that drives the PWM/DAC update at a periodic rate in order to generate the example output waveforms (e.g., sine wave output).

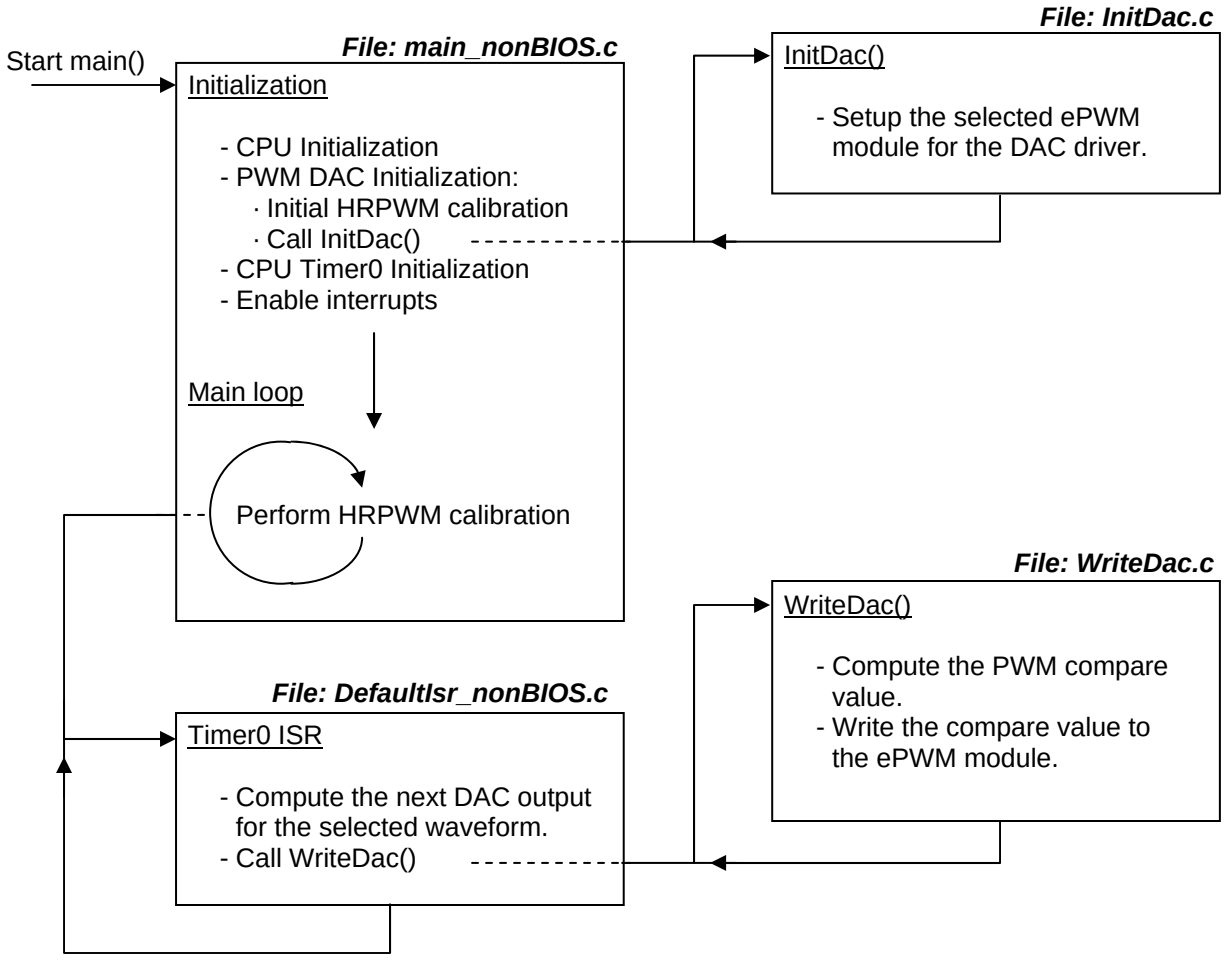

Figure 22. Flow of PWM/DAC Example Code

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8.2 Directory Structure and Filenames

The example code is fully self-contained, and requires no external libraries or files. The code includes and uses components from both the DSP280x peripheral header file download v1.60 (see reference [5]), and the TMS320F280x scale factor optimization (SFO) library (file SFO_TI_Build.lib, part of reference [5]). Table 2 shows the directory structure of the example code, while Table 3 provides a complete inventory of the files provided with the example.

Table 2. Directory Structure of Example Code

Directory	Contents
\cmd	Contains linker command files (.cmd files).
\DSP280x_headers\include	Contains the needed include files from the DSP280x Header File structures v1.60.
\DSP280x_headers\cmd	Contains the needed linker command file for the DSP280x header files.
\include	Contains include files (.h files).
\lib	Contains external code libraries (.lib).
\projects	Contains the example project file for Code Composer Studio (.pjt file).
\src	Contains the source code files (.c and .asm files).

Table 3. File Inventory for Example Code

Filename	Contents
\cmd\f2808_nonBIOS_ram.cmd	Main linker command file
\DSP280x_headers\cmd\DSP280x_Headers_nonBIOS.cmd[1]	DSP280x header file linker command
\DSP280x_headers\include\DSP280x_Adc.h[1]	Part of DSP280x header files
\DSP280x_headers\include\DSP280x_CpuTimers.h[1]	Part of DSP280x header files
\DSP280x_headers\include\DSP280x_DevEmu.h[1]	Part of DSP280x header files
\DSP280x_headers\include\DSP280x_Device.h[1]	Part of DSP280x header files
\DSP280x_headers\include\DSP280x_ECan.h[1]	Part of DSP280x header files
\DSP280x_headers\include\DSP280x_ECap[1]	Part of DSP280x header files
\DSP280x_headers\include\DSP280x_EPwm[1]	Part of DSP280x header files
\DSP280x_headers\include\DSP280x_EQep[1]	Part of DSP280x header files
\DSP281x_headers\include\DSP280x_Gpio.h[1]	Part of DSP280x header files
\DSP280x_headers\include\DSP280x_I2c.h[1]	Part of DSP280x header files
\DSP280x_headers\include\DSP280x_PieCtrl.h[1]	Part of DSP280x header files
\DSP280x_headers\include\DSP280x_PieVect.h[1]	Part of DSP280x header files
\DSP280x_headers\include\DSP280x_Sci.h[1]	Part of DSP280x header files
\DSP280x_headers\include\DSP280x_Spi.h[1]	Part of DSP280x header files

\DSP280x_headers\include\DSP280x_SysCtrl.h[1]	Part of DSP280x header files
\DSP280x_headers\include\DSP280x_XIntrupt.h[1]	Part of DSP280x header files
\include\Dac.h	PWM/DAC function prototypes
\include\DSP280x_DefaultIsr.h[1]	Part of DSP280x header files
\include\f2808_HRPWM_DAC.h	Main include file for project
\include\SFO.h	Include file for HRPWM SFO library
\lib\SFO_TI_Build.lib	Library file for HRPWM SFO library
\projects\f2808_HRPWM_DAC.pjt	Code Composer Studio project file
\src\CodeStartBranch.asm	Bootloader destination target
\src\DefaultIsr_nonBIOS.c	Interrupt service routines
\src\DSP280x_GlobalVariableDefs.c[1]	Part of DSP280x header files
\src\Gpio.c	GPIO initialization function
\src\InitDac.c	PWM/DAC initialization function
\src\main_nonBIOS.c	Main function
\src\PieCtrl_nonBIOS.c	PIE initialization function
\src\PieVect_nonBIOS.c	PIE vector initialization table
\src\SetDBGIER.asm	Utility function
\src\Sine256Q15.c	Q15 sine wave lookup table
\src\SysCtrl.c	F280x CPU initialization function
\src\Timer.c	F280x CPU timer initialization function
\src\WriteDac.c	PWM/DAC output function
\disclaimer.txt	Documentation file
\readme.txt	Documentation file

Table 3 Notes:

[1] This file is identical to the file of the same name found in the DSP280x peripheral header file download (see reference [5]).

8.3 Additional Information

1. The code can be run out-of-the-box on the eZdspF2808 board. As is, the code outputs PWM on the ePWM1A pin that, when low-pass filtered, will produce a 976.6 Hz, 2 volt peak-to-peak sine wave with 0.5 volts offset (i.e., 0.5 volts minimum, 2.5 volts maximum).

2. The key functions *InitDac()* and *WriteDac()* are generic for any ePWM module with HRPWM capability, and may be called independently for each PWM/DAC channel in use.

3. The HRPWM uses proprietary micro-edge positioning (MEP) technology that requires a calibrated software scaling factor. This scaling factor is obtained by running a scale factor calibration function. The usage approach employed in this example is to continuously run the calibration function in the background on an ePWM module not being used for HRPWM. In other words, the PWM/DAC uses one ePWM module, while the calibration function uses a second, different ePWM module. There are alternate HRPWM calibration approaches. See reference [4] for more information.

4. A number of user selectable options exist in the file *f2808_HRPWM_DAC.h*:

   - Selection of the PWM frequency.
   - Selection of the ePWM module to use as the PWM/DAC.
   - Selection of the ePWM module to use as the HRPWM calibration module.
   - Selection of the DAC output waveform (square wave, sine wave, or constant)
   - Selection of the DAC output waveform amplitude and offset.
   - Selection of the Timer0 period (DAC output update rate for selected waveform). Adjusting this changes the frequency of the sine wave or square wave PWM/DAC output.

   Details of each option are provided in the comment header of the file *f2808_HRPWM_DAC.h*. After adjusting any options, the project should be rebuilt.

9 Conclusion

The high-resolution PWM on the TMS320F280x DSP family has been used to implement a digital-to-analog converter with the addition of an external analog low-pass filter. Such an approach can offer a lower-cost alternative to a dedicated DAC chip. Using a 2nd order passive RLC filter, greater than 9 bits DAC resolution is achievable while still maintaining 100 kHz bandwidth. Alternately, greater than 10 bits of DAC resolution is achievable with 50 kHz bandwidth by modifying the filter component values. This is sufficient resolution and bandwidth for adoption in a wide variety of applications.

References

1. Hildebrand, F.B., “Advanced Calculus for Applications,” Prentice-Hall Inc., Englewood Cliffs, New Jersey, 2nd edition, 1976, ISBN 0-13-011189-9, pp. 214-223.
2. *TMS320F2809, TMS320F2808, TMS320F2806, TMS320F2802, TMS320F2801, TMS320C2802, TMS320C2801, TMS320F2801x DSPs Data Manual*, Texas Instruments Inc. (SPRS230).
3. *TMS320x28xx, 28xxx Enhanced Pulse Width Modulator (ePWM) Module Reference Guide*, Texas Instruments Inc. (SPRU791).
4. *TMS320x28xx, 28xxx High-Resolution Pulse Width Modulator (HRPWM) Reference Guide*, Texas Instruments Inc. (SPRU924).
5. C280x, C2801x C/C++ Header Files and Peripheral Examples, Texas Instruments Inc. (SPRC191). (Version at time of publication: v1.60).

Appendix A. Derivation of Worst-case Duty Cycle

Given the square-wave function f(t) depicted in Figure 3 where T denotes the period, p denotes the duty cycle, and K denotes the amplitude, it is desired to find the duty cycle p that maximizes the amplitude of the first Fourier harmonic of the signal, $0 \leq p \leq 1$.

The Fourier Series representation of f(t) was previously determined as:

$$f(t) = A_0 + \sum_{n=1}^{\infty}\left[A_n \cos\left(\frac{2n\pi t}{T}\right) + B_n \sin\left(\frac{2n\pi t}{T}\right)\right] \tag{1}$$

where

$$A_0 = K \cdot p \qquad A_n = K \cdot \frac{1}{n\pi}\left[\sin(n\pi p) - \sin(2n\pi(1-p/2))\right] \qquad B_n = 0 \tag{5}$$

The Fourier harmonics are given by the infinite summation term in equation (1), with the first harmonic obtained when n=1. Since the B_n terms are all zero, the components of the Fourier harmonics can be written as:

$$g_n(t) = A_n \cos\left(\frac{2n\pi t}{T}\right), \quad n = 0, 1, 2, \ldots \tag{A.1}$$

The energy content of a cosine waveform is proportional to the square of the signal. Therefore, maximum energy is obtained when the partial derivative of $g_n^2(t)$ with respect to p is equal to zero.

$$\begin{aligned}\frac{\partial}{\partial p}\left(g_n{}^2(t)\right) &= \frac{\partial}{\partial p}\left(A_n^2 \cos^2\left(\frac{2n\pi t}{T}\right)\right) \\ &= \cos^2\left(\frac{2n\pi t}{T}\right) \cdot \frac{\partial}{\partial p}\left(A_n^2\right) \\ &= \cos^2\left(\frac{2n\pi t}{T}\right) \cdot 2A_n \frac{\partial}{\partial p}\left(A_n\right) \overset{?}{=} 0\end{aligned} \tag{A.2}$$

Now, the cosine term is invariant to p, so it is not considered to meet the equality above. In addition, the term $2A_n$ is zero only when p is 0 or 1. This case represents the minimum energy content in the harmonics, where the PWM signal is simply a constant value of either 0 (when p=0), or K (when p=1). Thus, the energy maximizing solution in equation A.2 is found by setting the remaining term, the partial derivative of A_n, equal to zero.

$$\begin{aligned}\frac{\partial}{\partial p}(A_n) &= \frac{\partial}{\partial p}\left(\frac{1}{n\pi}\left[\sin(n\pi p)-\sin(2n\pi(1-p/2)\right]\right)\\ &= \cos(n\pi p)+\cos(2n\pi(1-p/2)\\ &= \cos(n\pi p)+\cos(2n\pi-n\pi p)\\ &= \cos(n\pi p)+\cos(2n\pi)\cdot\cos(n\pi p)+\sin(2n\pi)\cdot\sin(n\pi p) \overset{?}{=} 0\end{aligned} \quad \text{(A.3)}$$

Noting that cos(2nπ) equals 1 for all n, and that sin(2nπ) equals 0 for all n, one can re-write equation A.3 as:

$$2\cos(n\pi p) \overset{?}{=} 0 \quad \text{(A.4)}$$

Equation A.4 shows that maximum energy in each harmonic is obtained at different duty cycles. For example:

n=1 $\Rightarrow$ p=1/2 $\Rightarrow$ the 1st harmonic has maximum energy at 50% duty cycle

n=2 $\Rightarrow$ p=1/4 and 3/4 $\Rightarrow$ the 2nd harmonic has maximum energy at 25% and 75% duty cycle

It has thus been shown that p=1/2 maximizes the energy content of the 1st Fourier harmonic of the PWM waveform.

Revision History

Revision	Date	Who	Description of Major Changes from Previous Version
SPRAA88A	Sep. 2008	D. Alter	- Updated code for CCS v3.3.80.11 and C28x C-Compiler v5.0.2 (from v3.1 and v4.1.1 respectively). - Corrected op-amp gain bandwidth discussion in Section 4.
SPRAA88	Feb. 2006	D. Alter	- Original version.

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