Energy Efficiency Through Innovation

APPLICATION NOTE

SiC MOSFET
SPICE Model Usage Instructions

CONTENTS

This application note provides information on installing and using GeneSiC Semiconductor's SPICE models. The SPICE model package for each part consists of:

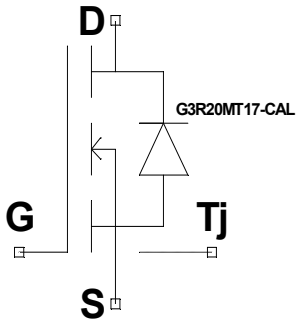
1) Encrypted SPICE Model (.lib)
2) Schematic Symbols (.asy)
3) SPICE Model Usage Instructions

The following points should be noted by the user while using these SPICE models:

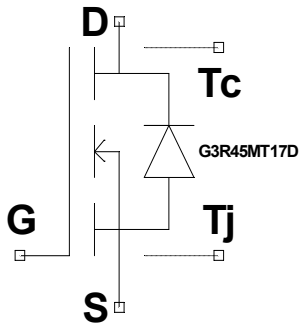
- The models are developed and optimized for usage in LTspice. It is the user's responsibility of verify the model before using the library on any other SPICE simulation tool.
- The models are designed to be accurate over operating temperature range specified on the product datasheet and include a provision of self-heating to observe the change in junction temperature of the device.
- These models provide a reasonable approximation for the MOSFET in third quadrant. It is optimized for operation in third-quadrant for V_{GS} = 20 V for G2R™ devices and V_{GS} = 15 V for G3R™ devices. The body diode threshold voltage is modeled at V_{GS} = -5 V. The variation in the body diode turn-on voltage with V_{GS} is not modeled.
- Parasitic inductances and resistances associated with the package (wire bonds and package pins) are included in the model.
- The avalanche capability of the device is not modeled.
- Bare chip models do not include any parasitic inductance (example: wire bond inductance) and they also do not include any heat dissipation (thermal) network. The user can model an external heat dissipation network at the T_j terminal.

1 – Model Description

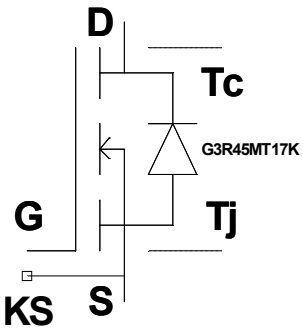
The terminals T_j and T_C are included in the model to analyze the self-heating of the device as a function of time. The terminal T_C represents the case temperature while T_j represents the junction temperature. These temperature connections work as voltage pins; therefore a potential difference of 1V refers to a temperature difference of 1°C. Either T_C or T_j must be connected to a voltage source to converge properly. T_j terminal can either be used to read junction temperature or apply a junction temperature. The voltage measured at T_j estimates the internal junction temperature of the device and it should be noted that the absolute maximum temperature at T_j should not exceed 175 °C under normal operating conditions. The remaining ports – Drain (D), Gate (G), Source (S) and Kelvin-Source (KS) are connected into the electrical circuit. A heat-sink (heat dissipation network) may be included / modeled as an external RC network.



Bare Chip



TO-247-3



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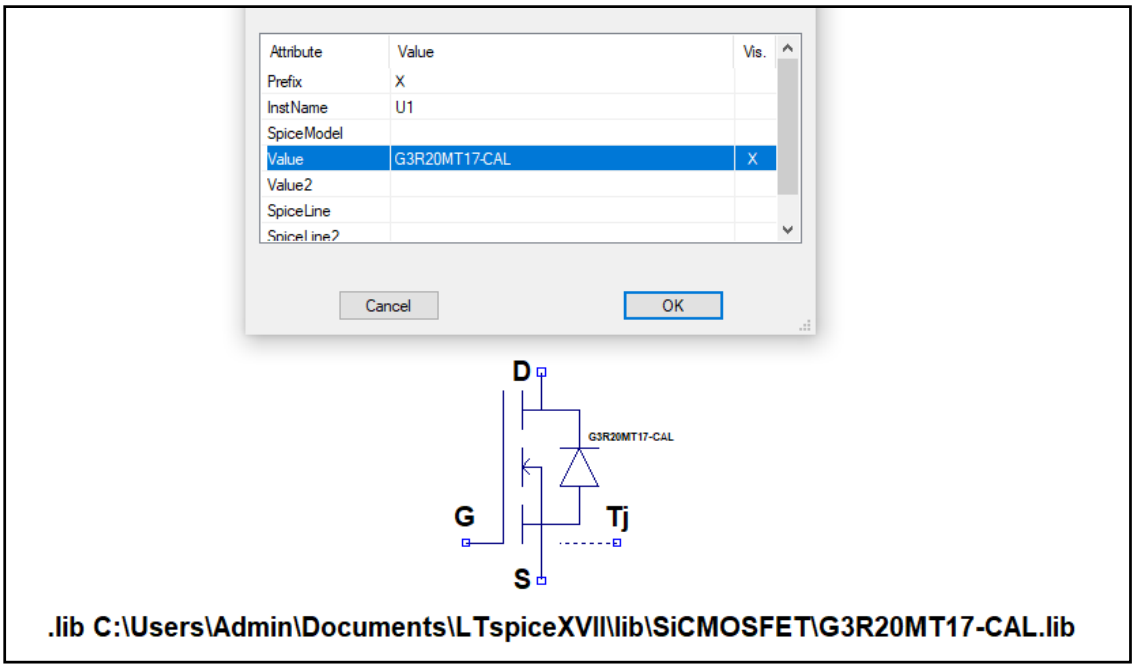
3 – Installation

These instructions are for LTSPICE users and provide guidance on installing GeneSiC Semiconductor's SPICE symbols and model libraries on the user's system.

1. After unzipping the package downloaded from the website, copy the contents (.asy files) of the "Schematic Symbols" folder containing SPICE symbols (.asy files) into your default LTSPICE symbols library directory.
   (Example Location: ***C:\Users\Admin\Documents\LTspiceXVII\lib\sym\SiCMOSFET***
2. Place the specific device model library file (.lib files) into your default LTSPICE directory / sub-circuit library folder. Remember this path as it will be useful to enter into LTSPICE directive later.
   (Example Location: ***C:\Users\Admin\Documents\LTspiceXVII\lib\SiCMOSFET***)
3. Open or restart LTSPICE to load the new symbols.

4 – Usage

1. Place the GeneSiC package symbol (Example: **L3_GeneSiC_MTseries_Bare-Chip.asy**) into the LTSPICE schematic using the Edit>Component selection dialog box.
2. Add a .lib SPICE directive which will link the relevant GeneSiC model library file to this schematic. Click Edit>SpiceDirective and a text box will appear.
   Enter ***.lib C:\Users\Admin\Documents\LTspiceXVII\lib\SiCMOSFET \G3R20MT17-CAL.lib***
3. Right Click on the MOSFET and edit the Value attribute, as shown in the figure below. Update the value of this attribute to GeneSiC part name (Example: ***G3R20MT17-CAL***)



Disclaimer

Models provided by GeneSiC Semiconductor are not warranted as fully representing all of the specifications and operating characteristics of the product to which the model relates. The model describes the characteristics of a typical product, and in all cases, the most recent revision of the product's datasheet is the recommended design guideline and the actual performance specification. Although SPICE models can be a useful tool in evaluating device performance, they cannot model the exact device performance under all conditions, nor are they intended to replace the design verification process. Therefore, GeneSiC Semiconductor does not assume any liability arising from their use and reserves the right to change models without prior notice.