SPI-Serial peripheral Interface is a standard protocol used for communication between two chips. (customized SPI)
It contains of 4 pins.

1) CSZ
2) SCLK
3) MOSI - Master Out Slave In
4) MISO - Master In Slave Out

CSZ : We can write or read during CSZ is low, which is chip select signal for protocol (active low)

SCLK : clock from Master to write in to slave and read from slave. Data can toggle should be settled on MISO/MOSI before fall edge of SCLK(sampling edge). We can toggle/change data at raise edge on MISO/MOSI.

MOSI(Master out slave in): Master writes data on this pin. Input pin to slave to read data from Master.

MISO(Master in slave out): Master reads data from this pin. Input pin to Master to read data from slave.

Regmap : consists of registers which are arranged in banks and pages(Hierarchy will be Bank consist of many pages and one page consist of many registers).Each register is of 1byte and is addressed from 00 to 7F.(In this design address has 7 bit, so maximum register address is 7F, we can use any of the register between this range).

MISO : There will be 16 clocks are needed for each read or write operation of SPI.
7 MSB bits are address(from 15 to 9) and 8th bit is read or write bit.
If it is 1 it is write operation then 7 to 0 bit represent data to be written in to register.
If 8th bit 0 then it Is read operation,7th ot 0th bit data is not valid(don’t care)
MISO: Always there should be zero on MISO for write operation. Initial 8 bits(15th to 8th bit) should be zero and from 7th to 0th bit should be read data.

	MSB															LSB
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	address							RB/W	Data(for write)							
MISO									Data(to read)							

Protocol timing diagram is as below.

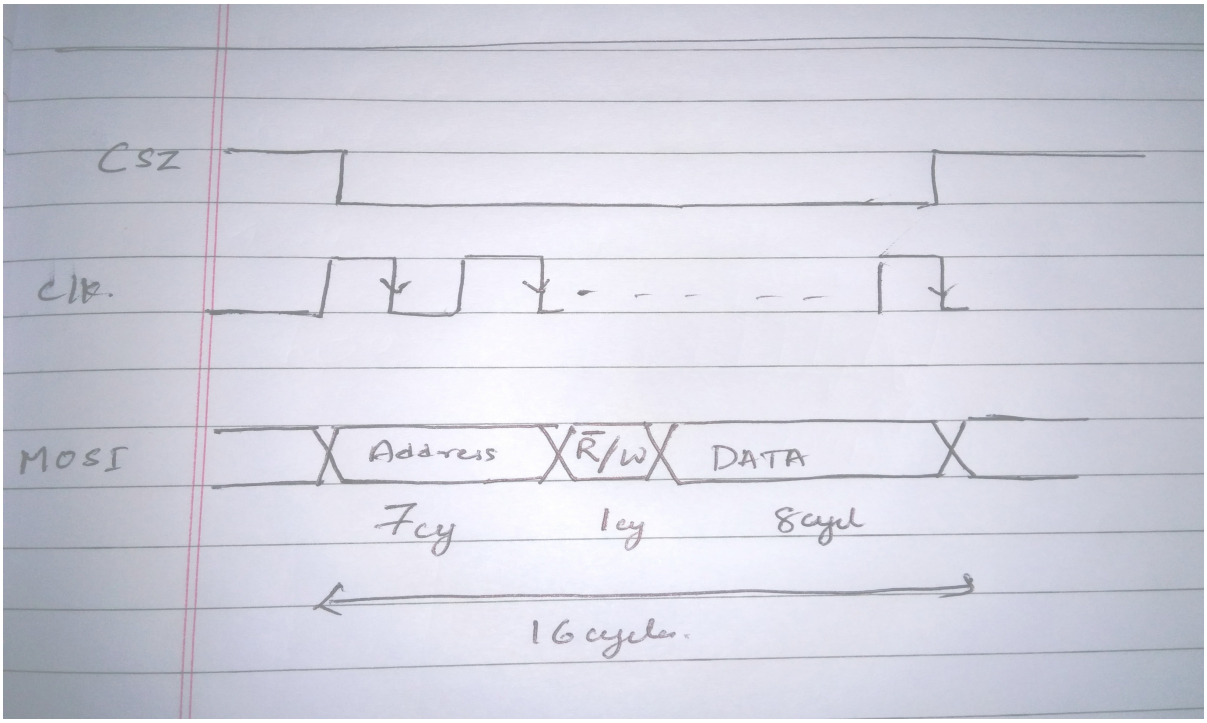

Fig 2 timing diagram of protocol

Digital block is shown in figure. Consists of 4 pins.

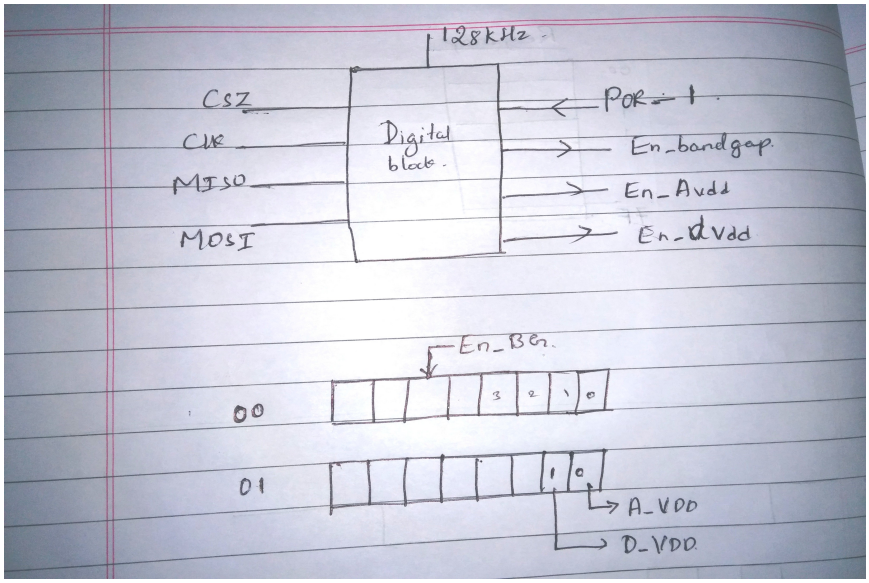

Fig 1 block diagram

POR - Should be one to enable operation.

en_bg : Output Signal to enable bandgap in analog block, Will be enable if 5th bit of reg address 7'h00 is high.
en_dvdd : Output Signal to enable LDO in analog block. Will be enable if 1st bit of reg address 7'h01 is high and en_bg is high.

en_avdd : Output Signal to enable LDO in analog block. Will be enable if 1st bit of reg address 7'h01 is high, en_bg is high and en_dvdd is high.

en_dvdd should go high only after en_bg is high and after 4 internal clock cycles.

en_avdd should go high only when en_bg is high and en_dvdd is high. en_avdd will be enabled after 4 internal clock cycles after en_dvdd enabling. frequency of internal clocks is 128Khz. Power up sequence is as shown in below digram.

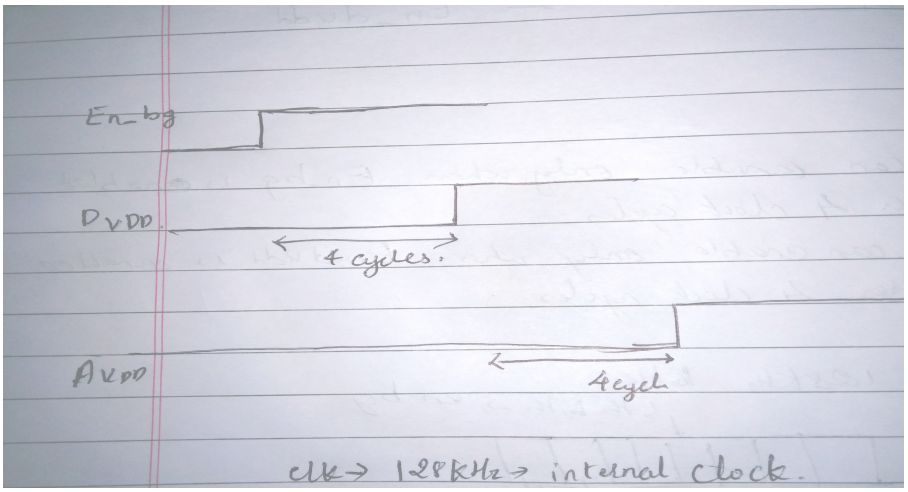

Fig 3 power up sequence

	7	6	5	4	3	2	1	0
7'h00					en_bg			
7'h01								
7'h02							en_dvdd	en_dvdd
7'h03								
.								
.								
.								
.								
7'h7F								

Fig 3 regmap