

**Idle Mode**

When the SM2..0 bits are written to 000, the SLEEP instruction makes the MCU enter Idle mode, stopping the CPU but allowing SPI, USART, Analog Comparator, ADC, Two-wire Serial Interface, Timer/Counters, Watchdog, and the interrupt system to continue operating. This sleep mode basically halts  $\text{clk}_{\text{CPU}}$  and  $\text{clk}_{\text{FLASH}}$ , while allowing the other clocks to run.

Idle mode enables the MCU to wake up from external triggered interrupts as well as internal ones like the Timer Overflow and USART Transmit Complete interrupts. If wake-up from the Analog Comparator interrupt is not required, the Analog Comparator can be powered down by setting the ACD bit in the Analog Comparator Control and Status Register – ACSR. This will reduce power consumption in Idle mode. If the ADC is enabled, a conversion starts automatically when this mode is entered.

**ADC Noise Reduction Mode**

When the SM2..0 bits are written to 001, the SLEEP instruction makes the MCU enter ADC Noise Reduction mode, stopping the CPU but allowing the ADC, the External Interrupts, the Two-wire Serial Interface address watch, Timer/Counter0 and the Watchdog to continue operating (if enabled). This sleep mode basically halts  $\text{clk}_{\text{I/O}}$ ,  $\text{clk}_{\text{CPU}}$ , and  $\text{clk}_{\text{FLASH}}$ , while allowing the other clocks to run.

This improves the noise environment for the ADC, enabling higher resolution measurements. If the ADC is enabled, a conversion starts automatically when this mode is entered. Apart from the ADC Conversion Complete interrupt, only an External Reset, a Watchdog Reset, a Brown-out Reset, a Two-wire Serial Interface address match interrupt, a Timer/Counter0 interrupt, an SPM/EEPROM ready interrupt, an External Level Interrupt on INT7:4, or an External Interrupt on INT3:0 can wake up the MCU from ADC Noise Reduction mode.

**Power-down Mode**

When the SM2..0 bits are written to 010, the SLEEP instruction makes the MCU enter Power-down mode. In this mode, the External Oscillator is stopped, while the External Interrupts, the Two-wire Serial Interface address watch, and the Watchdog continue operating (if enabled). Only an External Reset, a Watchdog Reset, a Brown-out Reset, a Two-wire Serial Interface address match interrupt, an External Level Interrupt on INT7:4, or an External Interrupt on INT3:0 can wake up the MCU. This sleep mode basically halts all generated clocks, allowing operation of asynchronous modules only.

Note that if a level triggered interrupt is used for wake-up from Power-down mode, the changed level must be held for some time to wake up the MCU. Refer to [“External Interrupts” on page 89](#) for details.

When waking up from Power-down mode, there is a delay from the wake-up condition occurs until the wake-up becomes effective. This allows the clock to restart and become stable after having been stopped. The wake-up period is defined by the same CKSEL fuses that define the Reset Time-out period, as described in [“Clock Sources” on page 36](#).

**Power-save Mode**

When the SM2..0 bits are written to 011, the SLEEP instruction makes the MCU enter Power-save mode. This mode is identical to Power-down, with one exception:

If Timer/Counter0 is clocked asynchronously, i.e., the AS0 bit in ASSR is set, Timer/Counter0 will run during sleep. The device can wake up from either Timer Overflow or Output Compare event from Timer/Counter0 if the corresponding Timer/Counter0 interrupt enable bits are set in TIMSK, and the global interrupt enable bit in SREG is set.

If the Asynchronous Timer is NOT clocked asynchronously, Power-down mode is recommended instead of Power-save mode because the contents of the registers in the asynchronous timer should be considered undefined after wake-up in Power-save mode if AS0 is 0.

This sleep mode basically halts all clocks except  $\text{clk}_{\text{ASY}}$ , allowing operation only of asynchronous modules, including Timer/Counter0 if clocked asynchronously.

## Standby Mode

When the SM2..0 bits are 110 and an External Crystal/Resonator clock option is selected, the SLEEP instruction makes the MCU enter Standby mode. This mode is identical to Power-down with the exception that the Oscillator is kept running. From Standby mode, the device wakes up in 6 clock cycles.

## Extended Standby Mode

When the SM2..0 bits are 111 and an external crystal/resonator clock option is selected, the SLEEP instruction makes the MCU enter Extended Standby mode. This mode is identical to Power-save mode with the exception that the Oscillator is kept running. From Extended Standby mode, the device wakes up in six clock cycles.

Table 18. Active Clock Domains and Wake Up Sources in the Different Sleep Modes

Sleep Mode	Active Clock Domains					Oscillators		Wake Up Sources					
	clk <sub>CPU</sub>	clk <sub>FLASH</sub>	clk <sub>IO</sub>	clk <sub>ADC</sub>	clk <sub>ASY</sub>	Main Clock Source Enabled	Timer Osc Enabled	INT7:0	TWI Address Match	Timer 0	SPM/EEPROM Ready	ADC	Other I/O
Idle			X	X	X	X	X <sup>(2)</sup>	X	X	X	X	X	X
ADC Noise Reduction				X	X	X	X <sup>(2)</sup>	X <sup>(3)</sup>	X	X	X	X	
Power-down								X <sup>(3)</sup>	X				
Power-save					X <sup>(2)</sup>		X <sup>(2)</sup>	X <sup>(3)</sup>	X	X <sup>(2)</sup>			
Standby <sup>(1)</sup>						X		X <sup>(3)</sup>	X				
Extended Standby <sup>(1)</sup>					X <sup>(2)</sup>	X	X <sup>(2)</sup>	X <sup>(3)</sup>	X	X <sup>(2)</sup>			

- Notes:
1. External Crystal or resonator selected as clock source
  2. If AS0 bit in ASSR is set
  3. Only INT3:0 or level interrupt INT7:4