When a current in the micro-ampere range is required, the self-biased reference described in the previous sub-section must employ quite high resistances (around $M\Omega$). This, in integrated implementation, corresponds to very large consumption of silicon area. This drawback can be overcome by using this very basic principle: the value of a resistance carrying a given current is reduced if the voltage across it is diminished. Thus, to save silicon area, a reduced voltage must be applied to the resistance defining the reference current. The circuit shown in Fig. 4.23 accomplishes this function. In fact, the voltage across the resistance R is not a V_{GS} but the difference between two V_{GS} (or the difference between two overdrive): the one going with M_1 minus that of M_2. Moreover, if we assume that the two transistors M_3 and M_4 are matched, they will carry the same current. If all transistors are in the saturation region we can write

$$I_1 = I_2 \tag{4.46}$$

$$\sqrt{\frac{2I_1L_1}{\mu C_{ox}W_1}} = \sqrt{\frac{2I_2L_2}{\mu C_{ox}W_2}} + RI_2 \tag{4.47}$$

Which is a system of two equations (one non linear) in the two variables, I_1 and I_2. Fig. 4.24 shows its possible graphic solution. It gives two results, one

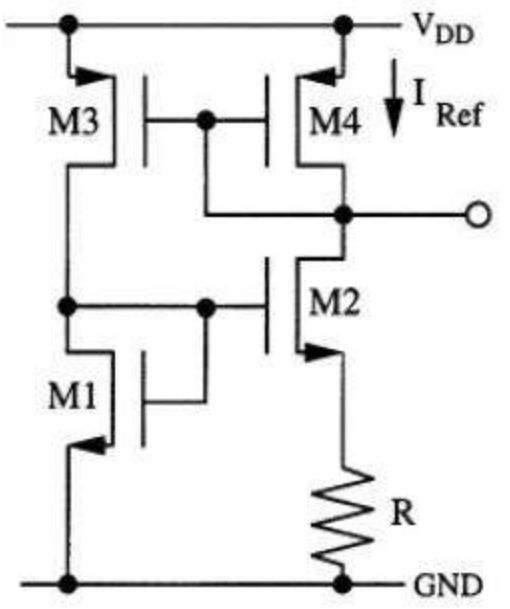


Fig. 4.23 - Self biased low current reference generator.

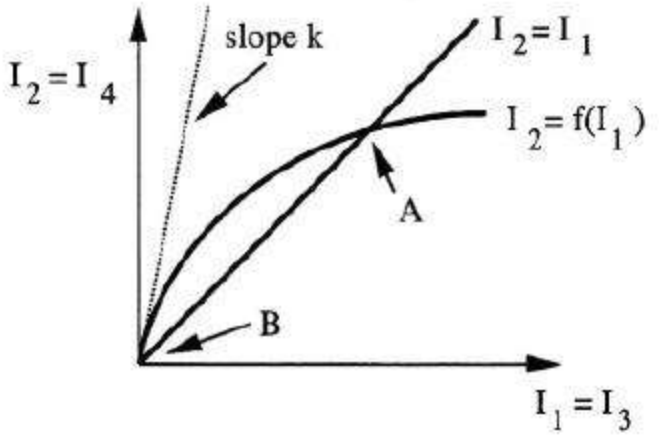


Fig. 4.24 - Graphic solution of the equations describing the circuit in Fig. 4.15.

of which, *B*, is trivial. Therefore, even for this circuit, it is necessary to use a start-up network to be sure that the current reference is driven to the proper operating point and is not stacked at zero current.

Of course the overdrive of M_1 must be suitably larger than the overdrive of M_2 to leave room for the voltage across *R*. This leads to the (obvious) condition $(W/L)_1 < (W/L)_2$. For modern CMOS technology the quantity $\mu_n C_{ox}$ is approximately $120\ \mu A/V^2$ (for n-channel devices); if the current to be generated is, for instance, $4\ \mu A$ and $(W/L)_1 = 3$, $(W/L)_2 = 30$, the overdrive voltage of M_1 becomes $149\ mV$ and that of M_2 becomes $47\ mV$. Therefore, the drop voltage across the resistance *R* is only $102\ mV$. The value of the resistor is consequently $25.5\ k\Omega$, approximately 6 to 10 times smaller (depending on the threshold value) than that required for the self-biased current reference studied in the subsection 4.2.2. Note that in the circuit considered here the supply independence is ensured by the high impedance elements M_2 and M_3.

The small signal equivalent circuit is similar to the one in Fig. 4.22. The only difference is that because of the diode connection M_1 is represented by a $1/g_{m1}$ resistance. (Fig. 4.25)

The current mirror $M_3 - M_4$ makes the signal currents in $1/g_{m1}$ and *R* equal $(i_{n2} = i_{n1})$. Therefore

$$v_{gs2} = \left[\frac{1}{g_{m1}} - R\right] i_{n1} \tag{4.48}$$

from which

$$[v_n^+ - v_n^-] = i_{n1}\left[\frac{1}{g_{m4}} + R + r_{ds2}\left(1 - \frac{g_{m2}}{g_{m1}}\right) + r_{ds2} g_{m2} R\right] \tag{4.49}$$

therefore

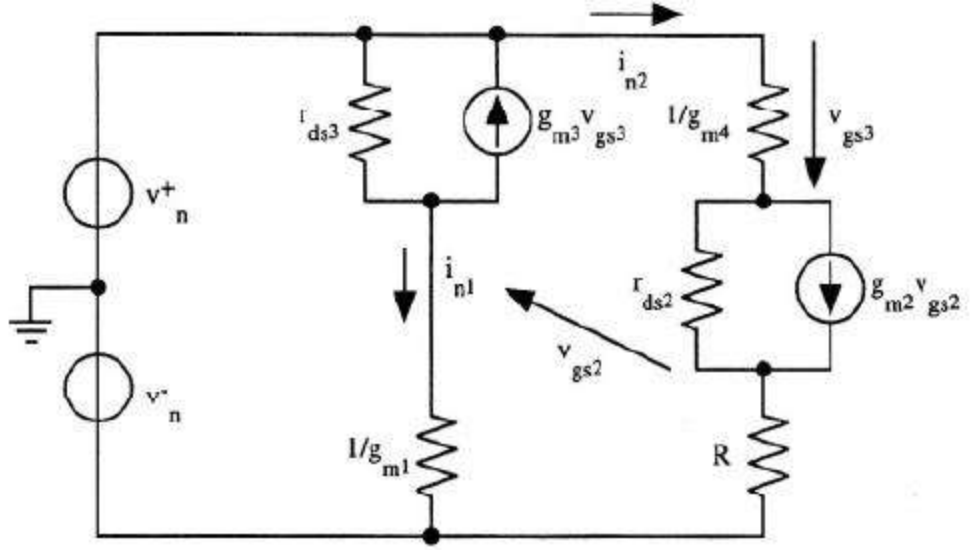


Fig. 4.25 - Small-signal equivalent circuit used to estimate the spur rejection in the self biased micro-current generator.

$$i_{n1} \cong \frac{[v_n^+ - v_n^-]}{r_{ds2} g_{m2} R} \tag{4.50}$$

The product $g_{m2}R$ (see equation (4.42)) equals the ratio between the drop voltage across R and the overdrive of M_2. Its value is not significantly lower than the one that we have in the normal self-biased current generator. Therefore, the micro-current version rejects spur with a similar extent as the scheme in Fig. 4.20 does.

Example 4.7

Determine, using Spice, the dependence on the supply voltage of the current in the self-biased micro generator shown in Fig. 4.23. Find the minimum operation value of V_{DD}. *Assume the following design parameters:* $(W/L)_1 = 3\mu/1\mu$; $(W/L)_1 = 30\mu/1\mu$; $(W/L)_3 = (W/L)_4 = 20\mu/2\mu$; $R = 25k\Omega$; $V_{DD} = 3\text{-}5$ V. *Analyse the circuit when the p-channel transistors are changed into* $(W/L)_3 = (W/L)_4 = 20\mu/8\mu$. *Moreover, repeat the simulations with* $R = 50\ k\Omega$. *Use the model parameters given in Appendix B.*

Solution:

The aspect ratios are the same used in the above section to estimate the drop voltage across the resistance R. If the process transconductance parameter of the technology used is the same used in the above section($120\ \mu A/V^2$*) the voltage across R is 102 mV. Therefore, being* $R = 50k\Omega$ *the expected current ranges around* $4\ \mu A$.

```
M1  2 2 Gnd Gnd MODN L=1u  W=3u
M2  1 2 3 Gnd   MODN L=1u  W=30u
M3  2 1 Vdd Vdd MODP L=2u W=20u
M4  1 1 Vdd Vdd MODP L=2u W=20u
R1  4 Gnd 25K
vdd Vdd Gnd 4.0
vx 3 4 0
Rs 1 Gnd 1000000K
.dc vdd 1 5 0.1
.print dc i(vx)
```

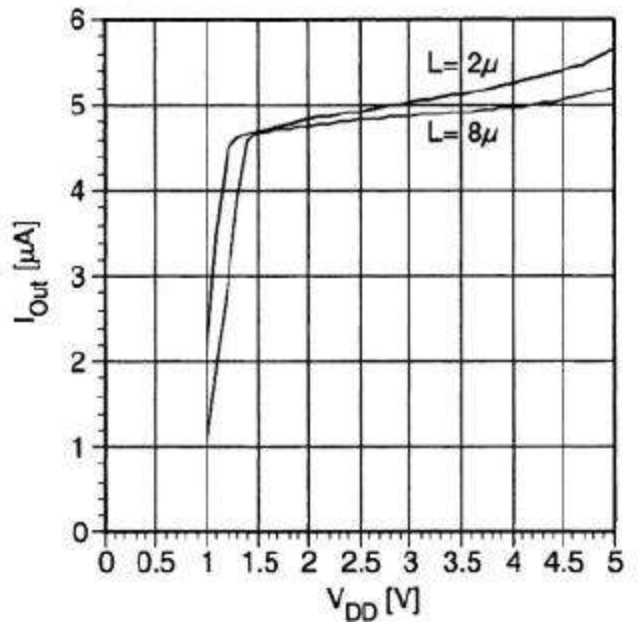
observe that, in addition to the expected elements, the Spice net-list includes the resistance R_s *(100 MΩ) connected between the node 1 and ground. Such a very high resistance forces an extremely low current (a few tens of pA) into the transistor* M_4 *thus avoiding the possible meta-stable condition* $I_3=I_4=0$.

The results of the simulation are summarized in the figure.

The generated current is slightly greater than expected (it ranges around $5\ \mu A$*). This difference comes from the approximations made in the hand calculations. Moreover the current dependence on the supply voltage is not so negligible. The reason is that the output resistance of the transistor used is far to be ideal. Therefore, increasing the supply voltage produces an increase in the current proportional to the* λ *factors. If the length of the p-channel transistors increases, the corresponding output resistance increases as well and the generated current is kept more independent of* V_{DD}.

From the simulation results we can estimate an equivalent output trans-resistance

$$r_{eq,\,out}(L = 2\mu) = \frac{\Delta V_{DD}}{\Delta I} = 3.5M\Omega \qquad r_{eq,\,out}(L = 8\mu) = 7.5M\Omega$$



The figure also shows the lower value of V_{DD} for proper operation of the circuit: it is necessary to have a supply voltage between 1 V and 1.5 V to start-up an output current. This voltage provides the V_{GS} and the saturation voltage of the transistors in each branch of the circuit.

The version that employs p-channel transistors with length 8μ requires a slightly higher V_{DD}: increasing the length also increases the output resistance but the ensuing reduction in the aspect ratio imposes a higher overdrive voltage.

Equation (4.47), remembering that $I_1 = I_2$, leads to the relationship $R = \alpha/\sqrt{I_1}$, where α is a suitable coefficient. Therefore, increasing the resistance by a factor 2 should decrease the current by a factor of 4. Simulation leads to a different result: the current drops only by a factor of 2.5. The reason, for this specific design, is twofold: equation (4.47) is approximated and, moreover, it holds for transistors in the saturation region. The use of condition (1.61) estimates for M_2 a transition point between saturation and weak inversion at $3.3\ \mu A$. Therefore, M_2 is likely in the weak inversion region and its V_{GS} becomes lower than the threshold voltage. Therefore, the voltage across R is higher than expected.