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Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS

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Abstract

This paper presents the opportunities and challenges for scaling A/D converters into ultra-deep-submicron CMOS technologies. With faster transistors and better matching, the trend is to migrate into higher sample rates with lower resolutions. Limited dynamic range at low supply voltages remains the utmost challenge for high-resolution Nyquist converters, and oversampling will become the dominant technique in this arena in the future. Linearity correction with digital calibration is also becoming prevalent as the efficiency of calibration circuitry improves.

Introduction

Explosive growth in wireless and wireline communications is the dominant driver for higher specifications of analog-to-digital converters (ADCs). New applications in wireless communications support multi-mode operation, utilize large portions of bandwidth, such as in the case of ultra-wideband and 60-GHz-band systems, or attempt to re-use the already licensed spectrum, thus requiring a high dynamic range for operation. Similarly, future wireline communication systems commonly extend the signal constellations to increase the data throughput, such as in the case of 10-Gb/s Ethernet or next-generation cable modems. These applications are driving the demand for high-resolution, high-speed, low power, and low cost integrated ADCs.

Technology scaling significantly lowers the cost of digital logic and memory, and there is a great incentive to implement high-volume baseband signal processing in the most advanced process technology available. Concurrently, there is an increased interest in using transistors with minimum channel length and minimum oxide thickness to implement analog functions, because the improved device transition frequency, f_T, allows for faster operation. However, scaling adversely affects most other parameters relevant to analog designs. To achieve a high linearity, high sampling speed, high dynamic range, with low supply voltages and low power dissipation in ultra-deep-submicron CMOS technology is a major challenge. In this paper we explore the challenges for ADC design associated with technology scaling. We will examine some circuit, architectural and system design techniques that will allow analog-to-digital converters to utilize transistors available in sub-100-nm technologies.

Technology Divergence with Scaling

Technology scaling doubles the density of digital logic every 2-3 years. Digital circuits have additionally benefited from scaling through increased operating frequencies and lower power consumption. Scaling to 90-nm CMOS technology and beyond is characterized by limited power. To minimize the dissipation, by balancing the switching and leakage power, digital systems choose the appropriate supply voltages and transistor types. Current foundry offerings are characterized by several thin-oxide devices, with different implant-controlled thresholds, and supply voltages that are scaled below the reliability-dictated levels. Furthermore, the same process usually offers thick-oxide I/O devices.

Analog functions can be implemented using either thin- or thick-oxide devices – the thick-oxide devices enjoy the benefit of a larger dynamic range (DR) and the thin-oxide devices harvest a higher operation frequency. This trend will continue in the future as predicted by ITRS (Fig. 1) [87]. Recent requirements to control the digital circuit leakage have slowed down the transistor threshold scaling, with a consequent reduction in supply voltage scaling. As a result, fast analog circuits can use 1V or higher supplies in the next few technology nodes. With continued scaling and the reduction of supply voltages in sub-1V range, the I/O devices will follow to sub-1.8V levels, and analog functions that require a high dynamic range would have to use additional process features or would have to be implemented on a separate chip.

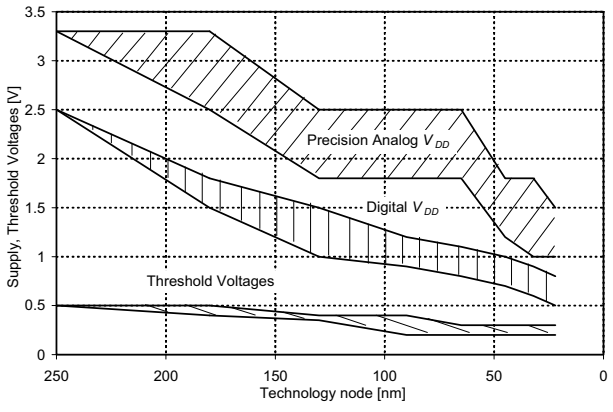


Fig. 1. Scaling of supply and threshold voltages.

Opportunities and Challenges in Scaling Analog Designs

As technology advances, there is an increased incentive for high-speed analog designs to exploit higher f_T of scaled transistors. A number of challenges presented by technology scaling however must be addressed.

Reduced Signal-to-Noise Ratio (SNR). The most prominent challenge for implementing precision analog circuitry in deeply scaled, "digital" processes is the reduction of supply voltages. It lowers the available voltage swings in analog circuits, fundamentally limiting the achievable SNR. To maintain the same dynamic range with a lower supply voltage in a noise-limited design, the circuit noise must also be proportionally reduced. For example, lowering the noise floor in switched-capacitor circuits requires an increase in the capacitor sizes to lower the kT/C noise, hence results in a penalty in power consumption.

Lower intrinsic gain. The intrinsic voltage gain ($g_m r_o$) of an MOS device is one important gauge of device performance for precision analog designs. As scaling continues, the intrinsic gain keeps decreasing due to a lower output resistance as a result of drain-induced barrier lowering (DIBL) and hot carrier impact ionization. In addition, gate leakage currents in very thin-oxide devices will set an upper bound on the attainable effective output resistance via circuit techniques (such as active cascode).

Device leakage. A fundamental advantage of MOS technology is the high quality switch naturally available. As scaling continues, the elevated drain-to-source leakage in an off-switch can adversely affect the switch performance. If the switch is driven by an amplifier, the leakage may lower the output resistance of the amplifier, hence limits its low-frequency gain. Charge storage on capacitive devices will become difficult with leaky transistors attached. In addition, the gate leakage current also violates the high-impedance "summing-node" assumption that underlines the operation of switched-capacitor circuits, especially at lower speeds. In a sense, the gate leakage current resembles the base current in a bipolar junction transistor.

Matching. Transistor matching properties are improved with a thinner oxide [95] [96]. However, devices with small geometries also experience larger mismatch due to higher order terms with either short W or L [97]. When the oxide thickness is reduced to a few atomic layers, quantum effects will dominate and matching will degrade.

Passives. Deeply-scaled CMOS processes target digital applications and frequently lack for high quality passives – inductors and capacitors. Sampled-data systems rely on linear, low-parasitic, high-density capacitors. Either double-poly or metal-insulator-metal (MIM) capacitor requires extra mask layers, hence adds cost. An alternative is the vertical, fringing metal capacitor [101]. These capacitors may benefit from reduced metal pitch and increased number of metal layers with technology scaling.

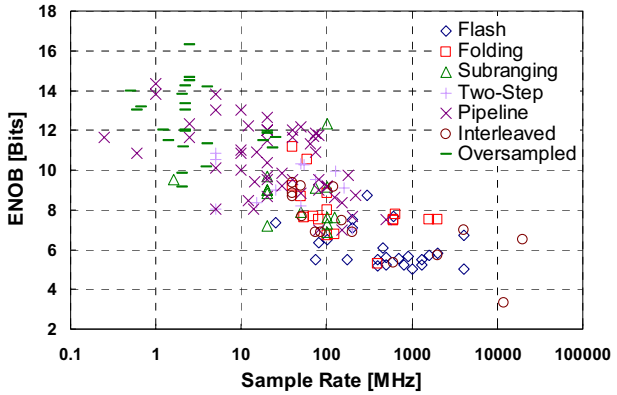


Fig. 2. ADC sample rate vs. ENOB from 1987 to 2005.

Scaling of ADC Architectures

The impact of technology scaling on the performance of various ADC architectures can be dichotomized according to the SNR specifications. While offering steadfast improvement of f_T, the accompanying reduction of supply voltages and the increased channel noise tend to shrink the dynamic range achievable by mixed-signal circuits in deeply scaled CMOS. For high-resolution converters, this inevitably leads to an increase of power consumption to maintain SNR. However, the accuracy of lower-resolution ADCs is limited by component mismatch, which results in a power and area scaling trend similar to that of the digital circuits for fixed conversion speeds (Table 1). The point of watershed at the current technology nodes seems to be between 8 and 10 bits.

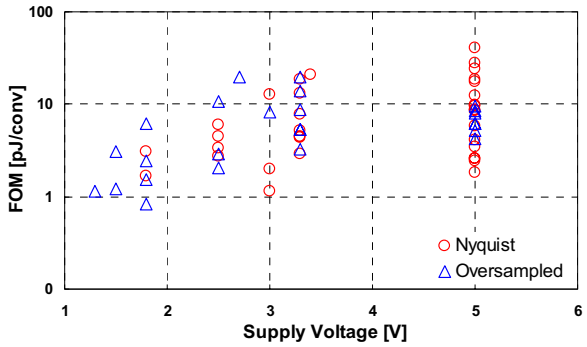
As scaling continues, there is a noticeable trend of a constant migration of the boundaries amongst the conventional A/D architectures (Fig. 2). While oversampled converters are encroaching into the regime used to be dominated by piepline ADCs [73], the later ones are reporting resolutions as low as 5-8 bits, which were only considered suitable for flash-type architectures [37].

A. Flash Converter

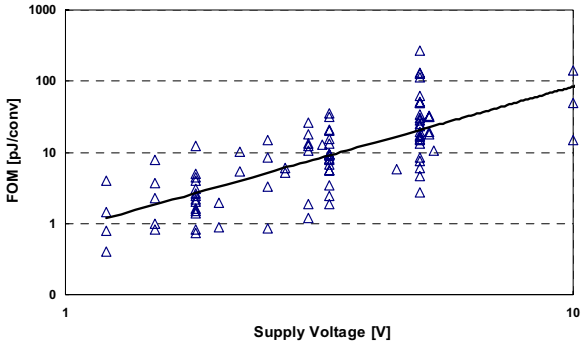
Flash converters are suitable for low-resolution (4-6 bits) applications that require high conversion rates (up to tens of gigahertz) and low latency. Although not a power-efficient architecture, the low latency feature makes it attractive in high-speed communication applications. Flash converters fall into the category of matching-limited scaling scenario.

Table 1. Scaling of Mixed-Signal Circuits

Scaling Parameter	SNR-Limited	Matching-Limited	Digital Circuits
Dynamic Range	$\propto \sqrt{C/kT}$	$\propto \sqrt{WL}$	Word length
Supply Voltage	$1/S$	$1/S$	$1/S$
Speed	1	1	S
Area	S^2	$1/S^2$	$1/S^2$
Power	S	$1/S^2$	$1/S^2$



(a)



(b)

Fig. 3. ADC scaling dichotomy, (a) SNR limited (≥ 12 bits) and (b) matching limited (≤ 10 bits). Data is taken from Fig. 2.

The major source of error in flash-type converters are the static and dynamic offsets sensed by the comparators, including offset errors originating from the comparators, the preamps, the reference ladders, and the relative timing skew of the strobe signals. Out of these, the dominant static offset often derives from the random threshold mismatch in the input devices of the preamps, which are used to suppress the large dynamic errors of small comparators and to mitigate kickback noise. As thin oxide improves the matching property of transistors [92] [96], smaller devices can be used in newer technology generations to achieve the same matching accuracy; this fact has been exploited by many recent works of flash-type converters to improve the figure-of-merit (FOM) or energy efficiency of the conversion

$$FOM = \frac{P}{2^{ENOB} \cdot f}, \qquad (1)$$

Where, f is the sample rate for a Nyquist ADC and twice the effective-resolution bandwidth in oversampled ones. This observation has been confirmed by Fig. 3b – the plot of FOM vs. supply voltage on a log-log scale shows a trend line with a slope of 2, which is predicted by column three of Table 1.

Because of the speed concerns, simple gain stages, such as the resistively-loaded differential pairs, are often used as the preamps in flash-type converters (Fig. 4).

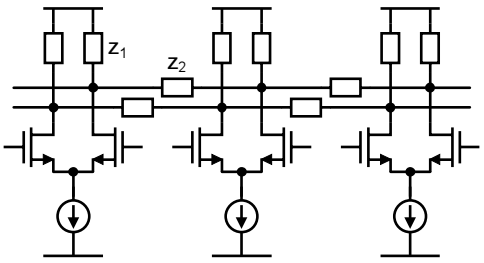
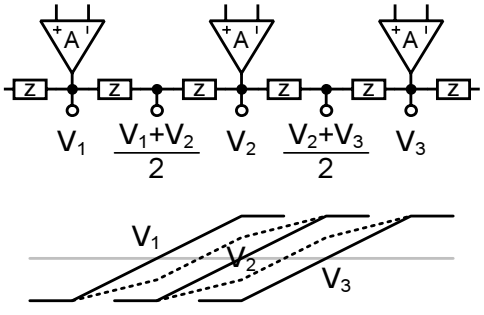


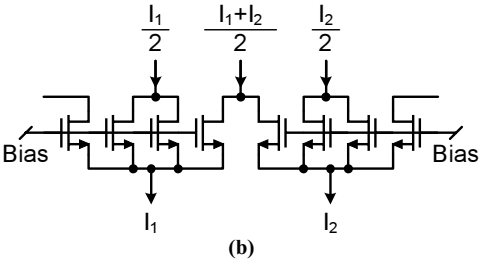
Fig. 4. Preamp with averaging network.

The simplicity of this circuit renders itself amenable to technology scaling and low supply-voltage operation. To further reduce the ADC power and input capacitance, resistive, capacitive [25] [20] [10], or current interpolation [17] can be performed to cut down the total number of preamps required (Fig. 5). The interpolation technique also leads to fewer points tapped off the reference ladder, resulting in a compact layout with less parasitics. Not only does a small layout improve the area and power efficiency, more importantly, it helps to keep the clock signal routing contained, which leads to a better dynamic performance of the converter.

Averaging (Fig. 4) is another common technique to improve the matching performance in preamps [9] [15] [4] [10]. Since the averaging effect improves in general with more amplifiers participating, a wider linear input range of the preamps and closely spaced reference voltages are beneficial. This is also in line with interpolation, where the active region overlap between adjacent differential pairs mitigates the interpolation error due to nonlinearity. Velocity saturation and lower supply voltages are driving flash converter designs converging toward this direction.



(a)



(b)

Fig. 5. Interpolation: (a) resistive/capacitive and (b) current.

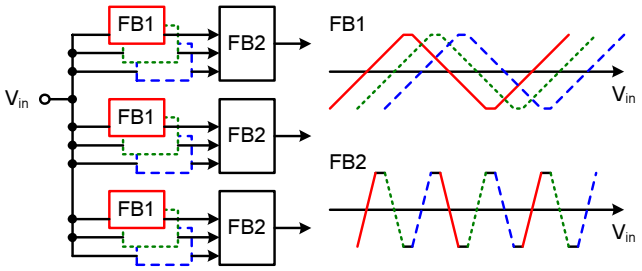


Fig. 6. Cascaded offset parallel folding.

B. Folding Converters

Interpolation reduces the number of preamps, but keeps the number of comparators the same. Signal folding has been developed to further improve the power efficiency of flash converters [16]-[19]. Compared to the flash architecture, the use of signal folding reduces the number of comparators by the folding factor F.[1] The combined hardware efficiency of folding, interpolation, and averaging has lead to CMOS realizations of flash converters with 1.6-GS/s sampling rate [11] or with resolutions of as high as 10-13 bits [13]-[15] at a reasonable power consumption.

The drawback of signal folding is that, if a large folding factor is developed in a single stage of folders, the bandwidth is greatly reduced due to large capacitive loads at the common output of many folding amplifiers; the maximum frequency seen at the folder output is given by

$$f_{\max} = \frac{\pi \cdot f_{in}}{\sin^{-1}(2/F)}, \qquad (2)$$

which can be many times higher than the maximum input frequency [16]. Furthermore, signal "rounding" problem at the folder output prevents further amplitude quantization, which has lead to the architecture of offset parallel folding with zero-crossing detection. This, however, leads to a large number of preamps used in the folders unless a significant amount of interpolation is also performed. Matching concern elevates for folders as, in addition to all other matching requirements, the current sources from different folding amplifiers also need to cancel each other precisely.

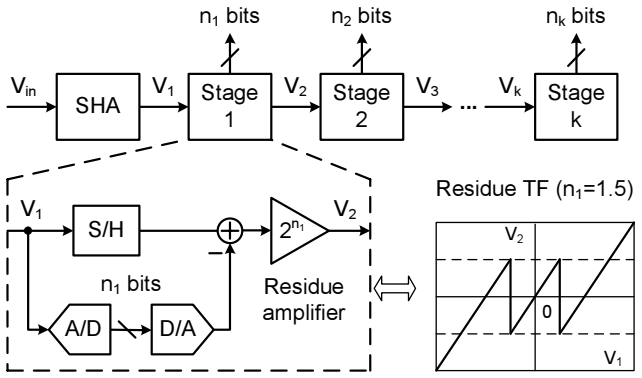


Fig. 7. 1.5-b/s pipeline ADC block diagram.

[1] Note that F coarse comparators are also required to resolve which fold the input signal resides in.

The above observation has lead to the design strategy to develop large folding factors successively by cascading folders with small folding factors [14] [15]. Pre-amplification is also increasingly necessitated by the folders to avoid active region overlap in adjacent folding amplifiers as the supply voltage is reduced, which also provides opportunities for averaging, interpolation, and pipelining.

C. Subranging Converter

The subranging architecture extends the resolution of flash ADCs by arranging the conversion in a coarse-fine two-step fashion. A sample-and-hold amplifier (SHA) and a switch matrix are usually required. In this architecture, latency is traded for low complexity and area/power efficiency. The achievable resolution in CMOS technology with this architecture is usually around 8-10 bits. If over/under-range protection is used, the offset requirements for the coarse converter can be greatly relaxed; but the fine one shares similar matching concerns as the flash architecture. Averaging and interpolation can be applied as well to reduce the number of preamps and their sizes. A balanced design can often achieve an FOM close to that of the pipeline converters [20] [22] [23].

D. Multi-Stage and Pipeline Converter

Taking the subranging concept to the extreme, a multi-stage ADC resolves the analog input in a cascade of low-resolution stages by passing the conversion residue to the trailing stages. Residue gain is usually provisioned to suppress the noise and nonlinearity contribution of lower ranked stages. The pipeline ADC is a typical multi-stage converter, which inserts SHAs in the residue amplifier to facilitate concurrent operation of all stages to improve throughput at the cost of increased latency. Similar to a subranging converter, over/under-range protection is necessary in a pipeline ADC and is often termed "digital error-correction" (DEC). A commonly used 1.5-bit/stage architecture is illustrated in Fig. 7.

Since the comparator offset specs are substantially relaxed due to a low stage resolution and the DEC, comparator design in pipeline ADCs is far simpler than that of the flash ones, and usually does not impose limitation on the overall conversion speed or precision. It is how fast and how accurate the residue signals can be produced and sampled that determines the performance of a pipeline converter, especially for the first stage that demands the highest precision. Negative feedback is conventionally employed to stabilize the voltage gain and to broaden the amplifier bandwidth. It is expected that technology advancement will keep pushing the nondominant poles of these amplifiers to higher frequencies, hence offer the potential of a higher conversion speed.

Nonetheless, the above statement is true only when a close-to-minimum channel length is used. At these dimensions, the accompanying short-channel effects pose serious challenges to realizing high open-loop gain, low noise, and low power consumption simultaneously at

significantly reduced supply voltages. The tradeoff between speed, dynamic range, and precision will eventually place a fundamental limit on the resolution of pipeline converters attainable in ultra-deep-submicron CMOS technologies (Fig. 3a).

One such fundamental limit is the dynamic range. The sampling process inherent in switched-capacitor circuits introduces kT/C noise at each pipeline stage when a residue voltage is captured. The sampled noise usually comprises two major contributions – the channel noise of the switches and the amplifier noise. As the switch resistance is only weakly affected by technology scaling [97], it is expected that amplifier will become the dominant noise source in pipeline ADCs in deeply scaled technologies. Based on this observation, efforts were directed to search the optimum stage resolution n and scaling factor γ to minimize the total conversion power [53] [55]. It has been recently pointed out that, for a uniform n and γ, the total ADC power is expressed as

$$P = SNR \cdot kT \cdot f_s \cdot \left(\frac{V_{gs} - V_{Th}}{V_{DD}} \right) \cdot g(n, \gamma, \eta), \qquad (3)$$

where f_s is the sample rate, V_{gs}-V_{Th} is the overdrive voltage of the amplifier input transistors, and $\eta \in [0,1]$ is the speed factor that models the parasitic loading effect depending on the conversion speed [36]. The evaluation of the function $g(.)$ reveals that a choice of 2-3-bit/stage resolution yields the optimum architecture for high-speed pipeline converters.

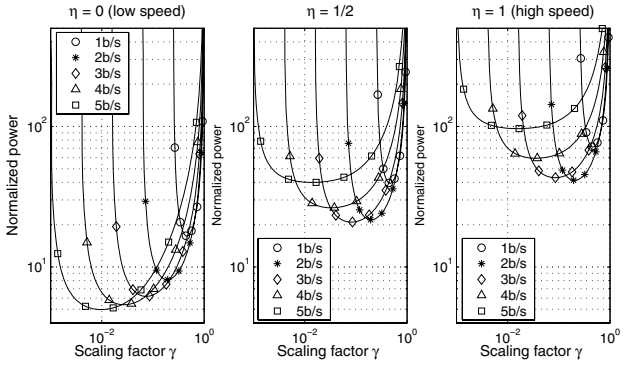


Fig. 8. Optimizing the stage resolution and scaling factor of a pipeline ADC at different sample rate.

E. Oversampled Converter

As mentioned before, technology scaling is commensurate with high sample rate but not high resolution. One technique to trade speed for dynamic range is oversampling – circuit and quantization noises are spread out and later suppressed by a digital decimation filter. Noise shaping is often facilitated to push quantization noise (and part of the circuit noise) further out of the interested signal band. The noise shaper often takes the form of a sigma-delta modulator.

Although oversampling plus noise shaping enables the use of smaller capacitors, other design constraints of the modulator such as linearity share similar concerns as the Nyquist converters.[2] Specifically, the signal swing at the amplifier output is increased due to the lag of the modulator feedback loop in response to a change in the input signal; a high oversampling ratio also stresses the amplifiers for settling speed. However, the decimation filter, being a digital circuit, greatly benefits from technology scaling. It is expected that oversampled ADCs will outperform pipeline converters for high-SNR applications in the near future.

F. Interleaved Converter

Interleaving was originally introduced to improve the power efficiency of a single-path converter as the sample rate is pushed close to the limit set by the fabrication technology [71]. Although the conversion speed of interleaved ADC arrays always surpass their single-path counterparts, the inherent problems of path mismatch and sample clock skew amongst the parallel paths substantially limit the attainable resolution of this converter. A single frontend SHA helps to mitigate the clock skew limitation but often has to be implemented in a different technology due to its high clock rate. Therefore, interleaved ADCs are suitable for 6-8-bit applications that require extremely high speed. Calibration is often engaged to improve the path matching condition. In spite of these difficulties, an interleaved pipeline converter clocked at 20 GS/s has recently been demonstrated [62].

G. Linearity Enhancement with Digital Techniques

It has long been noticed that conversion nonlinearity resulted from component mismatch (such as capacitor ratio errors) can be remedied by recording the error in a memory and successively removed by trimming or digital post processing [59] [91]. It is especially suitable to Nyquist A/D architectures that use an algorithmic approach (non flash-type). A genre of the techniques, a.k.a. digital calibration, were later proliferated to treat amplifier offset and gain errors, switch-induced errors in algorithmic and multi-stage ADCs, and the path mismatch problem in interleaved ADCs [49-52] [54-56] [58] [66] [67] [90]. The recent flurry of research activities in this direction is most likely motivated by Moore's law, which makes the digital calibration circuitry increasingly smaller and more power-efficient [27] [31-33] [35] [38-40] [46] [62] [63] [87] [89].

Just as the oversampling technique trades speed for SNR, the calibration technique can trade digital complexity for precision. Therefore it presents a major opportunity for the design of high-performance ADCs in ultra-deep-submicron CMOS. The combination of oversampling, noise shaping, calibration, and higher device f_T may constitute a viable approach for future high-DR, high-accuracy, and high-speed A/D converters. Hitherto, calibration works on ΣΔ converters have been reported [76] [84]. The concept of digital trimming was also recently reported in a folding ADC [11].

[2] Strictly speaking, only the front stage is subject to these constraints while the input-referred noise and nonlinearity of later stages are much attenuated by the front stage.

Nonetheless, digital treatment on error parameters that are supply voltage and temperature dependent poses serious challenges on the adaptation speed of the calibration algorithm used. This may limit the types of errors that can be reliably treated. The use of simple analog building blocks in the critical paths of high-precision converters also invites common-mode rejection-ratio (CMRR) and power-supply rejection-ratio (PSRR) issues that are typically not included in the calibration loop.

Scaling of Building Blocks

Technology scaling affects the design choices for various ADC building blocks. Amplifiers, sample-and-hold (S/H) circuits and comparators are common building blocks for many A/D architectures.

A. Operational Amplifier

In frontend S/H amplifiers or multi-stage ADCs, precision op amps are almost invariably employed to relay the input signal (or the residue signal) to the trailing conversion circuits. Negative feedback is usually engaged to establish signal transfer fidelity. Operating on the edge of the performance envelope, op amps exhibit intense tradeoffs amongst the dynamic range, linearity, settling speed, stability, and power consumption. As a result, the conversion accuracy and speed are often dictated by the performance of these amplifiers. While technology advancement offers an attractive reward of wider bandwidth, hence a higher sampling rate, with high f_T devices, concerns for matching, low intrinsic gain, hot carrier effect, and sensitivity to process variations often direct a seasoned designer away from using transistors of minimum channel lengths in high-performance op amps.

Nonetheless, resorting to long-channel devices has only a limited capability to recover the needed open-loop gain to achieve a 10-bit or higher conversion accuracy. Multi-stage amplifiers and gain-boosted single-stage amplifiers are becoming popular choices at low supply voltages. Although the necessity for frequency compensation renders a multi-stage amplifier less power-efficient, it may become the only viable op-amp architecture at a supply voltage of less than 1V. CMOS gain boosting (a.k.a. active cascode) exploits the fact that when the load is purely capacitive, the DC gain of an op amp can be increased by enhancing the cascoding effect using negative feedback [92]-[94]. The technique is effective in boosting the output resistance R_o with negligible effect on the effective G_m. Recently, it was demonstrated that further gain is attainable through a recursive gain-boosting technique [36]. The ultimate limit of this approach would be the direct current path to ground at the drains of the cascode devices due to hot carrier induced substrate current and the effective gate resistance due to oxide tunneling current.

In addition to various short-channel effects, the most prominent challenge presented by technology scaling is probably the reduced supply voltage. It has become increasingly difficult to maintain the dynamic range of an op amp while keeping its power consumption low. Recent designs all exploited the differential topology to improve SNR and noise immunity. Stressed by the ever-decreasing supply voltage, pseudo-differential op amps have also been explored more frequently [36] [42] [43]. However, with this architecture, care must be exercised to regulate the common-mode biasing in a multi-stage ADC to avoid unnecessary accumulation of offset voltages. Switched op amp is another approach to achieve high output swing and to save power (it can also function as the sampling switch). While the slow turn-on following a complete op-amp turn-off lead to low conversion speeds in earlier works, a recent attempt demonstrated an 8-bit, 200-MS/s pipeline ADC with partially switched op amps [30].

B. Sample-and-Hold

Inherent to the A/D conversion process is a sample-and-hold (S/H) circuit that resides in the frontend of a converter (and also between stages in a multi-stage converter). In addition to suffering from additive circuit noise and signal distortion just as the rest of the converter does, the S/H also requires a precision time base to define the exact acquisition time of the input signal. The dynamic performance degradation of an ADC can often be attributed to the deficiency of the S/H circuit (and the associated buffer amplifier).

In CMOS technology, switched capacitors are the preferred implementation of the S/H circuits (Fig. 9). The performance of these samplers can be gauged by the small-signal bandwidth when the switches are on and the ratio of the gate capacitance of the switch to that of the sampling capacitor. Technology scaling reduces the associated capacitance while keeping the switch on-resistance nearly constant [97]; not only does this improve the tracking bandwidth of the S/H, it also alleviates the charge injection problem during the turn-off of the sampling switch, which typically results in distortion as the dynamics of the switch-off is quite signal-dependent (even with bottom-plate sampling). In other words, the increase of f_T through technology scaling improves the linearity of the sampling switch. A rule-of-thumb is to use minimum channel length for switches when no critical matching/leakage requirement is concerned.

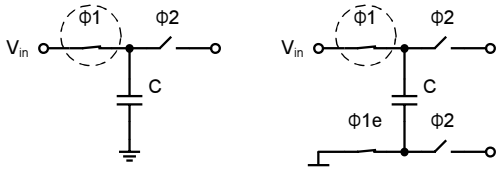


Fig. 9. Top- (left) and bottom- (right) plate sampling.

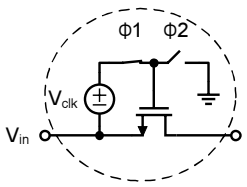


Fig. 10. Concept of clock bootstrapping.

A prominent drawback of a simple S/H is the on-resistance variation of the input switch that introduces distortion. Technology scales the supply voltage faster than the threshold voltage, which results in a larger on-resistance variation in a switch. As a result, the bandwidth of the switch becomes increasingly signal dependent. Clock bootstrapping was introduced to keep the switch gate-source voltage constant [28] [44] [48] [55] [78] [83]. Care must be exercised to ensure that the reliability of the circuit is not compromised.

In most high-performance sampled-data acquisition interfaces, the sampling clock is derived directly or indirectly (e.g., through phase-locking) from an off-chip low-phase noise crystal oscillator. This setup often renders the on-chip clock buffer the dominant source of aperture jitter. The improvement of the rise/fall time of digital gates over each generation of technology desensitizes the clock buffer jitter performance to circuit and supply noises.

C. Preamp and Comparator

The offset in preamps and comparators constitutes the major source of error in flash-type converters. Simple differential structure with thin oxide devices will keep dominating the preamp architecture in newer technologies. Dynamic performance is crucial at high sample rates with high input frequencies. Circuit techniques addressing these issues [12] [20] will continue to be explored.

Summary

Sustained scaling of high-performance CMOS ADCs in the ultra-deep-submicron regime and the prospect for future performance attainable through technology scaling are analyzed and projected.

Acknowledgments

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Flash ADC

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Folding ADC

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