Scaling Guidelines for CMOS Linear Analog design

Timothée Levi:
Address: IMS Laboratory, 351 Cours de la Libération, 33405 Talence Cedex
Phone: +33 5 4000 6540
Fax: +33 5 5637 1545
Email: timothee.levi@ims-bordeaux.fr

Noëlle Lewis, IMS Laboratory, University of Bordeaux 1, Talence, France
Jean Tomas, IMS Laboratory, University of Bordeaux 1, Talence, France
Pascal Fouillat, IMS Laboratory, University of Bordeaux 1, Talence, France

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Timothée Levi, Noëlle Lewis, Jean Tomas, Pascal Fouillat
IMS laboratory
CNRS / ENSEIRB, University Bordeaux 1
Talence, France
timothee.levi@ims-bordeaux.fr

***Abstract*— This paper proposes scaling guidelines for CMOS analog design during a technology migration. The scaling rules aim to be easy to apply and are based on the simplest MOS transistor model. The principle is to transpose one circuit topology from one technology to another, while keeping the main figures of merit, and the issue is to quickly calculate the new transistor dimensions. Furthermore, when the target technology has smaller minimum length, we expect to obtain a decrease of area. The proposed guidelines are applied to linear examples: OTAs. The results are compared on four CMOS processes whose minimum length are 0.8 µm, 0.35 µm, 0.25 µm and 0.12 µm.**

I. INTRODUCTION

Nowadays analog design flow is much less automated than digital counterpart. Efforts must be done towards developing methods and tools that could accelerate the analog design cycle. The main idea is to reuse already design blocks. The resizing of the design is an essential tool for the reuse of analog circuits.

The main goals of a resizing methodology are to keep performances of the original design but also to reduce area and power consumption during a technology migration.

In this work we present resizing guidelines of MOS analog designs during a technology migration.

The paper is organized as follows. First we summarize the state of art of the resizing. Then we explain our scaling rules. We apply it on a linear circuit: an OTA.

II. STATE OF ART

Recently, several works have been proposed in the reuse of analog blocks, and including resizing. The work of C. Galup-Montoro and M.C. Schneider [1], [2] proposed an analytical approach of MOS transistor resizing and several strategies depending on the type of the original circuit. In this work, the used model of MOS transistor is the ACM model [3] and application circuits are OTAs.

This method was extended in [4], adding experimental results from a complete Miller OTA, exploring additional performance aspects of analog circuits. And it was also extended in [5], using a tuning procedure based on an optimization loop [6].

The main drawback of these works is the increase of chip area in the OTA examples.

Some EDA companies [7] have recently started to offer tools and services aimed at design reuse and technology migration. [7] and [8] based their approaches on an optimization loop and intensive SPICE simulations in order to check and suitably modify circuit parameters to obtain the specified performances.

III. GENERAL APPROACH

The proposed resizing guidelines could be summarized in three steps:

Step 1: Definition of the figure(s) of merit to be preserved

Step 2: Calculation of the technological scaling factors

Step 3: Decision on some strategic aspects and computation of the new transistor sizes

The last computation step relies on MOS transistor model equations. In the present work, the Level 1 MOS transistor model is carried out and gives correct estimations. Naturally, it is possible to use more accurate equations like those of BSIM3V3 to determine the scaling rules and then the new sizes of transistors.

The scaling factors [9] are defined in Table 1, considering a migration from a technology 1 to a technology 2.

The first four factors are calculated from known technological parameters (Step 2).

The goal is to evaluate the factors K_L and K_W.

TABLE I. DEFINITION OF THE SCALING FACTORS

Parameters	Scaling factors
Supply voltage : V_{DD}	$K_V = V_{DD2} / V_{DD1}$
Oxide capacitance : C_{OX}	$K_{OX} = Cox_2 / Cox_1$
Mobility : μ_0	$K_\mu = \mu_{02} / \mu_{01}$
Effective gate voltage : $V_{EG}=V_{GS}-V_T$	$K_{EG} = V_{EG2} / V_{EG1}$
Length of the transistor : L	$K_L = L_2 / L_1$
Width of the transistor : W	$K_W = W_2 / W_1$

Here is the main equation, derived from Level 1 MOS transistor model, which is carried out in the next paragraphs:

- the drain current in the saturation region

$$I_D = \frac{\mu_0 C_{ox} W}{2L} V_{EG}^{\ 2} \qquad (1)$$

IV. APPLICATION EXAMPLES

Applications of these guidelines are proposed on a linear application: an OTA where all the transistors are in saturation mode, for a technology migration from CMOS 0.8 µm to CMOS 0.35 µm, to CMOS 0.25 µm and to CMOS 0.12 µm.

A. Resizing procedure

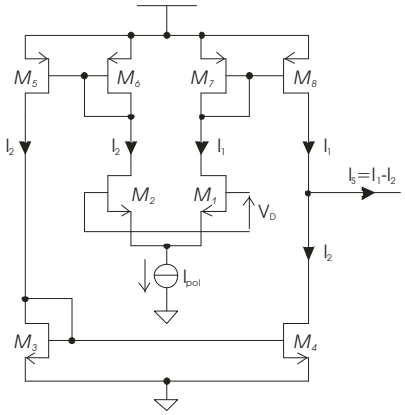

Figure 1. Schematic of the OTA

Fig. 1 describes the classical circuit topology.

The original circuit has been designed in CMOS 0.8 µm technology with a supply voltage of 5 V and first scaled in CMOS 0.35 µm technology with a 3.3 V supply voltage, then in 0.25 µm technology with a 2.5 V supply voltage, and finally in 0.12 µm technology with a 1.2 V supply voltage. In this OTA, all the transistors are in saturation mode.

Step 1: the figure of merit to be kept is the transconductance OTA gain.

Step 2: K_V, K_{OX}, K_μ are deduced from technological information.

Step 3: A simple way to conserve the transconductance OTA gain is to keep the same current drain, then from (1) and Table I:

$$\frac{\mu_{01} C_{OX1} W_1}{2L_1} V_{EG1}^{\ 2} = \frac{\mu_{02} C_{OX2} W_2}{2L_2} V_{EG2}^{\ 2} \qquad (2)$$

$$W_2 = \frac{\mu_{01} C_{OX1} W_2 2L_2}{\mu_{02} C_{OX2} 2L_1} \frac{V_{EG1}^{\ 2}}{V_{EG2}^{\ 2}} \qquad (3)$$

$$W_2 = \frac{K_L}{K_\mu K_{ox} K_{EG}^{\ 2}} W_1 \qquad (4)$$

$$K_W = \frac{K_L}{K_\mu K_{OX} K_{EG}^{\ 2}} \qquad (5)$$

At this step, K_L and K_{EG} are indeterminate.

We decide to keep also the same value for V_{EG} ($V_{EG1}=V_{EG2}$), checking after if this decision is compatible with the decreasing V_{DD} values. Furthermore, we reduce the transistor length L in the same proportion of decreasing of the minimum length of the technology, so: $K_L = L_{MIN2} / L_{MIN1}$.

Then we determine K_W value using equation (5).

As the scaling factors are determined, the new transistor sizes could be calculated.

TABLE II. SIZES OF THE TRANSISTORS

Transistors W/L	0.8 µm 5 V	0.35 µm 5 V	0.25 µm 2.5 V	0.12 µm 1.2 V
M_1 (µm)	20/10	8.75/4.4	3.6/3.15	0.8/1.5
M_2 (µm)	20/10	8.75/4.4	3.6/3.15	0.8/1.5
M_3 (µm)	40/10	17.5/4.4	7.25/3.15	1.55/1.5
M_4 (µm)	40/10	17.5/4.4	7.25/3.15	1.55/1.5
M_5 (µm)	40/10	19.75/4.4	6.45/3.15	2.45/1.5
M_6 (µm)	40/10	19.75/4.4	6.45/3.15	2.45/1.5
M_7 (µm)	40/10	19.75/4.4	6.45/3.15	2.45/1.5
M_8 (µm)	40/10	19.75/4.4	6.43/3.15	2.45/1.5

B. Characterization of resized OTAs

To determine the DC performance of the methodology we compare the DC transconductance gain G_0 (the slope of DC transfer characteristic in linear region (figure 2)).

To obtain the DC voltage gain, the Gain-Bandwidth product and the phase margin, an output capacitance has been added. Its value is fixed at 50 pF.

All of the simulations are made with Cadence Environment with Spectre simulator. The transistor's model is the BSIM3V3 model where the channel length modulation and the short channel effect are included.

TABLE III. RESULTS OF THE SIMULATIONS

Technology (µm) Supply Voltage (V)	0.8 5	0.35 5	0.35 3.3	0.25 2.5	0.12 1.2
G_0 (µA.V^{-1})	38	39	38	39	38
DC voltage Gain (dB)	54	54	54	54	49
Gain-Bandwidth product (MHz)	6.5	6.5	6.5	6.5	6.1
Phase Margin	88°	89°	89°	89°	89°
Power Consumption (µW)	302	302	198	150	72
Area (µm^2)	2800	580	580	150	22

Table IV describes the results of the simulations of the OTA, with the resizing methodology. We observe a small variation of the gains and the gain-bandwidth product but there is a huge decrease of the area (80 %) and the consumption (34%), then a reduction of the chip cost.

In technology 0.12 µm, we notice a decrease of the DC gain voltage. We decide to consider this result as an initial guess for an optimization post-procedure. Then with the optimization algorithm of Cadence environment, we determine the new sizes of transistors (Table IV) and then the new performances which are given in Table V.

TABLE IV. COMPARAISON OF THE TRANSISTORS SIZES IN 0.12 UM / 1.2 V PROCESS

Transistors W/L	Initial guess	after optimization
M_1 (µm)	0.8/1.5	1.05/2.65
M_2 (µm)	0.8/1.5	1.05/2.65
M_3 (µm)	1.55/1.5	2.65/1.1
M_4 (µm)	1.55/1.5	2.65/1.1
M_5 (µm)	2.45/1.5	2.75/1.35
M_6 (µm)	2.45/1.5	2.75/1.35
M_7 (µm)	2.45/1.5	2.75/1.35
M_8 (µm)	2.45/1.5	2.75/1.35

TABLE V. COMPARAISON OF OTA PERFORMANCES IN 0.12 UM / 1.2 V PROCESS

Technology (µm) Supply Voltage (V)	Initial guess	after optimization
G_0 (µA.V^{-1})	38	38
DC voltage Gain (dB)	49	54
Gain-Bandwidth product (MHz)	6.1	6.5
Phase Margin	89	89
Power Consumption (µW)	72	72
Area (µm^2)	22	29

C. MonteCarlo Simulations

The MonteCarlo simulations determine the behaviour of a design with parameters variation. It can change uniformly the parameters (change of wafer): it is the MonteCarlo simulation with process. It can change the parameters for each component (on the same wafer): it is the MonteCarlo simulation with mismatch. Then these simulations permit the verification of the robustness of the design.

The next figures 2, 3, 4 describe the behavior of the OTA's DC gain in a closed loop with MonteCarlo simulations with mismatch and process. The MonteCarlo simulation of the DC gain voltage in technology 0.25 µm is not included in this work because the MonteCarlo transistor models in this technology are not available.

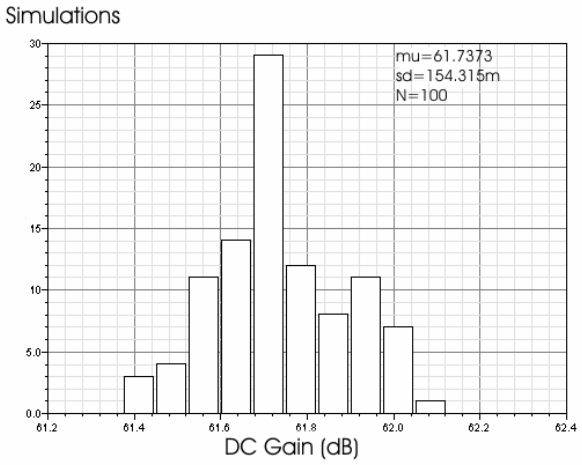

Figure 2. MonteCarlo simulation of the DC voltage gain of the OTA in technology 0.8 µm with 5 V

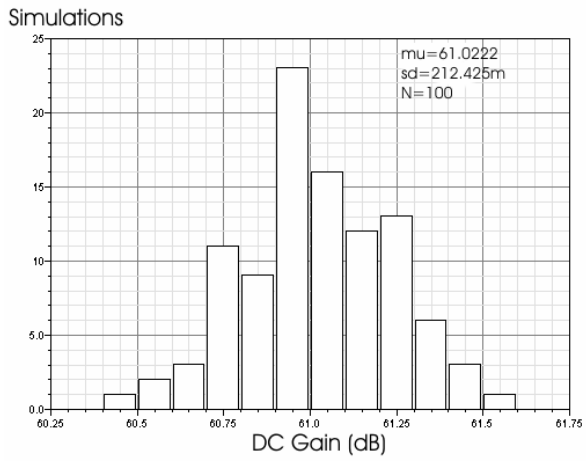

Figure 3. MonteCarlo simulation of the DC voltage gain of the OTA in technology 0.35 µm with 3.3 V

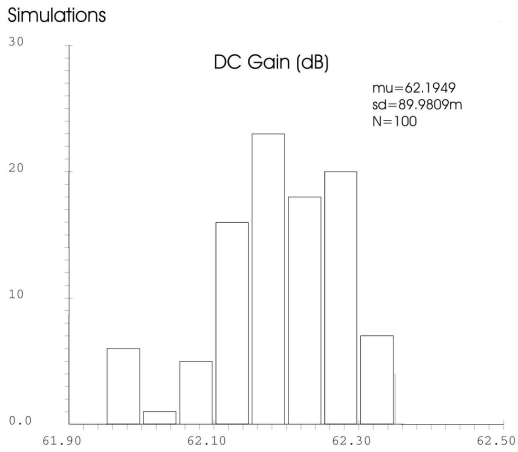

Figure 4. MonteCarlo simulation of the DC voltage gain of the OTA in technology 0.12 µm with 1.2 V and with the optimization tool

The gain mean-value is maintained as the standard deviation ($\simeq$0.15 dB) during the technology migration.

For 0.8 µm 5 V, 0.35 µm 3.3 V and 0.12 µm 1.2 V, all values of the simulated voltage gain are included between 98 and 102 % of the initial value, proving the robustness of the design along this resizing.

Simulation results describe that the methodology keeps the chosen figure of merit: G_0. But it also maintains other performances as AC figures of merit (DC voltage gain and gain-bandwidth product) except for a few technologies where the optimization tool is needed. It conserves the robustness of the design and reduces the cost with the decrease of area (80 % between 0.8 µm and 0.35 µm, 75 % between 0.35 µm and 0.25 µm and 85 % between 0.25 µm and 0.12 µm) and the power consumption (a K_V ratio depending of the decrease of the supply voltage).

V. CONCLUSION

The work presented here gives guidelines for resizing during a technology migration. It was applied on a linear circuit (OTA) to compare with others resizing works. The presented guidelines decompose the resizing process into three steps. This work clearly highlights which parameters are deduced from technological information and which ones are determined thanks to different strategic decisions.

Calculation and simulations were checked against the original design. The results of this technological migration support the success of this redesign technique. Indeed our goals were to conserve performances of the initial circuit, and to reduce area. Furthermore the gain in area for the OTA is nearly 80 %. This gain generates a huge decrease of the chip cost.

Those guidelines could represent a useful technique for determining at a "first step" of a general resizing methodology with an optimization tool.

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