

Shreyas Jayantilal Patel

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My immediate aim is to gain work experience and learn the current trends of ASIC & FPGA verification and design and expand my horizon while working as an ASIC design/verification engineer and work with full capacity and dedication for the concerned organization.

ACADEMIA

Pursuing Master of technology in VLSI Design (3rd Semester)
VIT University, Chennai

Bachelor of Engineering in Electronics & Telecommunication
Atmiya Insitute of Technology and Science, Rajkot.

XIIth
Vasani Forward School, Rajkot

Xth
Nirmala Convert School, Wankaner

Sr. No.	Course	Discipline / Specialization	Board / University	Percentage (%)	Year of Passing
1.	M.Tech	VLSI Design	VIT University	8.6 (CGPA)	2014
2.	B.E.	Electronics and Telecommunicaton	Saurashtra University	68.33	2011
3.	H.S.C	Science stream	Gujarat State Board	60.00	2007
4.	S.S.C	S.S.C	Gujarat State Board	65.86	2005

ACADEMIC PROJECTS

- **PG Project :**

Title : Optimize Design Platform for High Speed Digital Filter Using Folding Technique.

Duration : Jul'12 – May'13

Description : Main aim of project to minization number of register used in DSP filter and also reduce the time-to-market pressure for RTL design engineer .

- **UG Project :**

Title : Weighing Scale Automation using RFID.

Duration : Aug'10 – Apr'11

Description : Main aim of project to transfer the weighted data by loadcell (Instrument to measure the weight of any object almost used in shop) to lcd which placed at receiver side using RFID

TECHNICAL SKILLS

1.	VLSI Tools	Tanner EDA, Cadence EDA, Xilinx ISE, Modelsim
2.	Programming Languages	Verilog, C
3.	Assembly Languages	Micro controller 8051 and Microprocessor 8085

ACHIEVEMENTS

1. Secured 1st rank in Group Discussion Competition Dextrous'10, Rajkot
2. Secured "B" grade for Communicative English-LAB, Rajkot.

TRAINING

1. Took part in Industrial automation training at "NCVT Institute Private Limited" at Rajkot.
2. Attended training session by "Videocon Industries Limited" at Bharuch.

EXTRA-CURRICULAR ACTIVITIES

1. Student member of IEEE for the year 2013-14.

STRENGTH

1. Hard work
2. Proactive
3. Adaptive

HOBBIES

Playing Volleyball, Social Service.

PERSONAL VITAE

Date of Birth : 3th April, 1990.
Address (Per.) : Sarita App, B/No-101, University Road, Rajkot -360005.
Dist:- Rajkot State:- Gujarat
Alternative email ID : patel.shreyas2012@vit.ac.in
Languages Known : English, Hindi and Gujarati (Read, Write and Speak)

DECLARATION

I hereby declare that the information furnished above is true to the best of my knowledge and understanding.

Place: Rajkot

Your Truly
(Patel Shreyas Jayantilal)