

## References

- [1] Amit Berman and Idit Keidar, "Low-Overhead Error Detection for Networks-on-Chip", ICCD 2009, IEEE Conference on Computer Design, 2009
- [2] Isarel Cidon, "Zooming in on Network-on-Chip Architectures", SIROCCO 2009, Piran, Slovenia, May 25-27, 2009
- [3] Marcello and Miltos D. Grammatikakis, "Design of Cost-Efficient Interconnect Processing Unit", CRC Press, United States of America, 2009, Chapter 2.
- [4] David Atienza, Federico Angiolini and Srinivasan Muralia, "Network-on-Chip design and synthesis outlook", INTEGRATION, the VLSI journal 41 (2008) 340–359.
- [5] Yuan-Long Jeang, Win-Hsien Huang and Wei-Feng Fang, "A Binary Tree Architecture for Application Specific Network On Chip (ASNOC) Design", The 2004 IEEE Asia-Pacific Conference on Circuits and Systems, December 6-9, 2004.
- [6] Axel Jantsch and Hannu Tenhunen, "Network on Chip", Kluwer Academic Publishers, United States of America, 2003, Chapter 5.
- [7] Ahmed Hemani, Axel Jantsch and Shashi Kumar, "Network on a Chip: An architecture for billion transistor era"
- [8] <http://www.design-reuse.com/articles/10496/a-comparison-of-network-on-chip-and-busses.html>
- [9] [http://en.wikipedia.org/wiki/OSI\\_model](http://en.wikipedia.org/wiki/OSI_model)
- [10] <http://www.imit.kth.se/info/FOFU/NOC/>