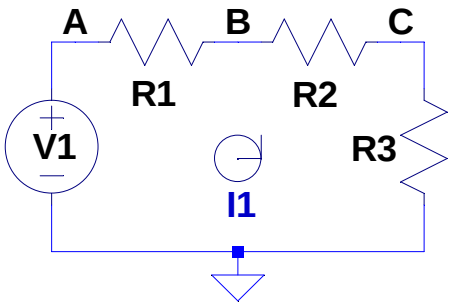
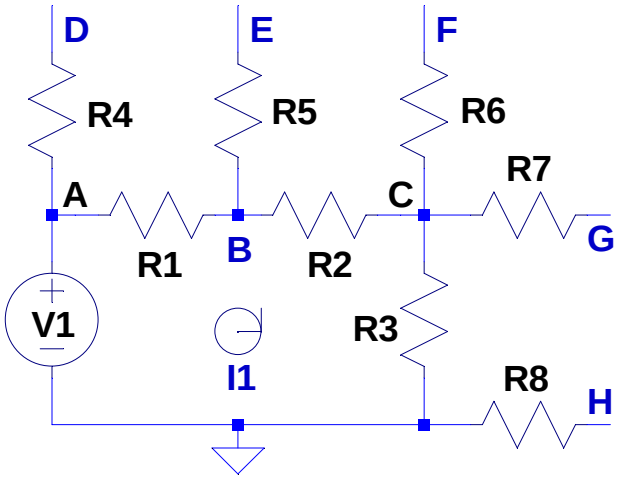
FIGURE 1



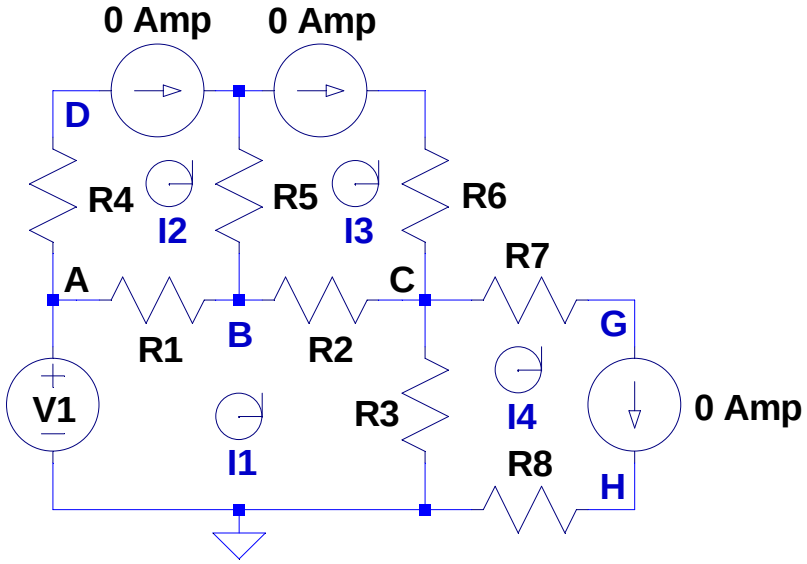
A single loop circuit

FIGURE 2



Possible redundant elements added
R4, R5, R6, R7 and R8

FIGURE 3



Possible redundant loops added
I2 = I3 = I4 = 0

--- C:\Users\TOSHIBA\Desktop\temp\RedundantLoops_01.asc ---