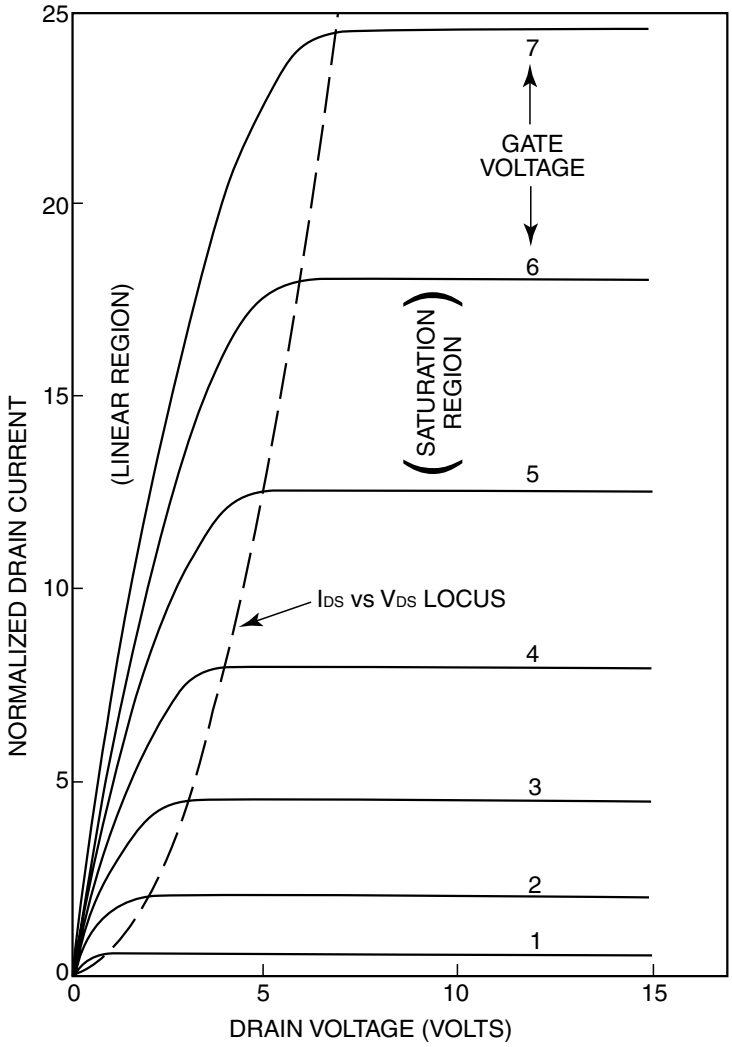

FIGURE 1.59 Current-voltage characteristics of a power MOSFET.

Breakdown Voltage

This is the drain voltage at which the reverse-biased body-drift diode breaks down and a significant current starts to flow between the source and drain by the avalanche multiplication process, while the gate and source are shorted together. Breakdown voltage, BV_{DSS}, is normally measured at a drain current of 250 μA. For drain voltages below BV_{DSS} and with no bias on the gate, no channel is formed under the gate at the surface and the drain voltage is entirely supported by the reverse-biased body-drift *pn* junction. There are two related phenomena which can occur in poorly designed and processed devices. These are punch-through and reach-through.

Punch-through is observed when the depletion region on the source side of the body-drift *pn*-junction reaches the source region at drain voltages below the rated avalanche voltage of the device. This provides a current path between source and drain and causes a soft breakdown characteristic as shown in Fig. 1.60. The leakage current flowing between source and drain is denoted by I_{DSS}. Careful selection and optimization of the doping profile used in the fabrication of a power MOSFET is therefore very important. Figure 1.61 shows a typical diffusion profile for a power MOSFET. The surface concentration of the body diffusion and the channel length (distance between the two *pn*-junctions formed by the source diffusion and the channel diffusion) will determine whether punch-through will occur or not. There are trade-offs to be made between on-resistance R_{dson} which requires shorter channel lengths and punch-through avoidance which requires longer channel lengths. An approximate equation giving the depletion region width as a function of silicon

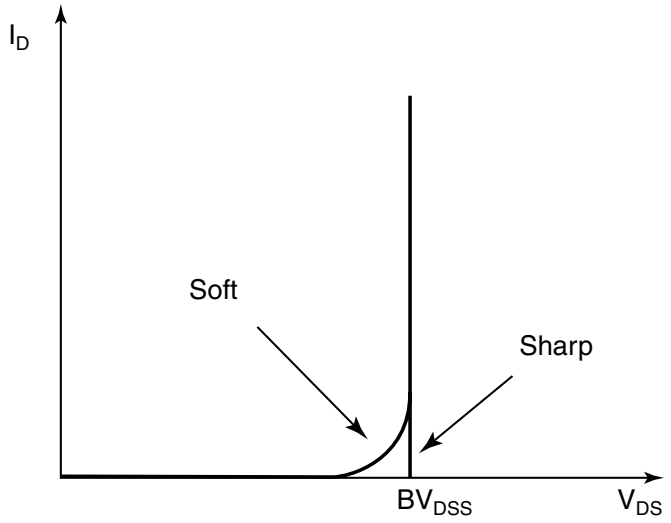

FIGURE 1.60 Breakdown characteristics of a power MOSFET showing the ideal (sharp) and nonideal (soft) behaviors.

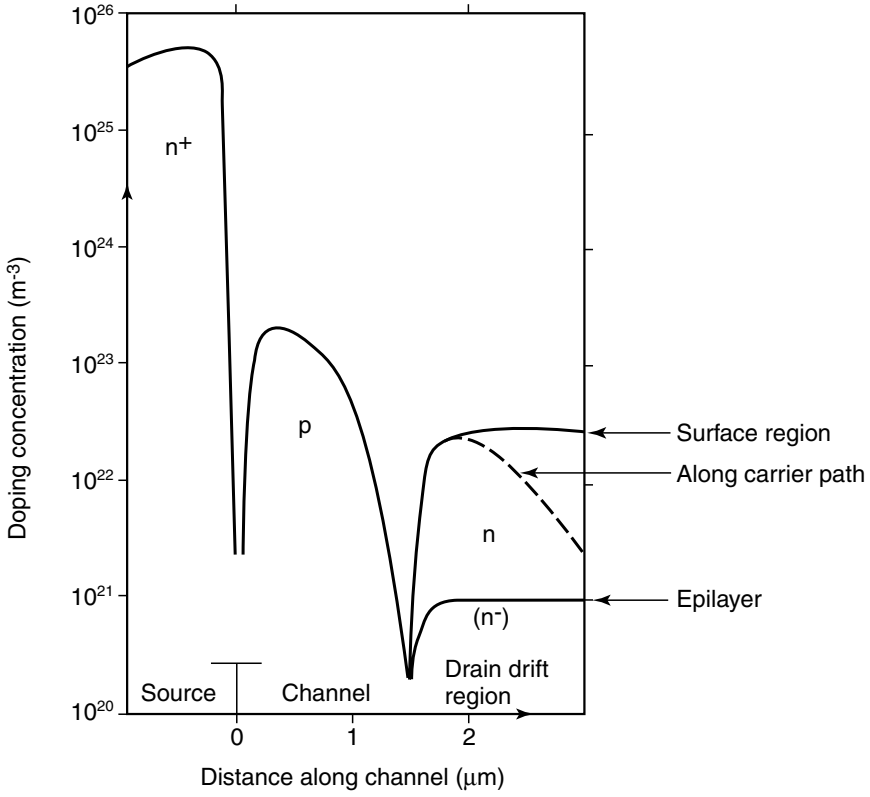

FIGURE 1.61 Typical doping profile of a power MOSFET, in a direction parallel to the device surface. Threshold voltage is determined by the peak carrier concentration in the channel region.

background doping is given by:

$$W \approx \sqrt{\frac{4\epsilon_s KT}{q^2 N_A} \ln\left[\frac{N_A}{n_i}\right]} \tag{1.1}$$

where ϵ_s is semiconductor permittivity, K is Boltzmann's constant, T is temperature in K, q is electronic charge, N_A is background doping, and n_i is the intrinsic carrier density.

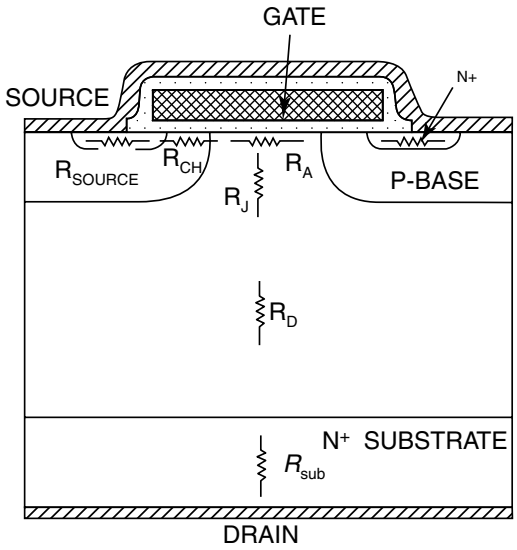

FIGURE 1.62 The origin of the internal resistances in a power MOSFET.

Also, higher channel implant dose is beneficial from the punch-through point of view since depletion width will be smaller, but the R_{dson} will suffer through reduced carrier mobility. The design of the doping profile involves choosing channel and source implant doses, diffusion times and temperatures that give a designed threshold voltage while simultaneously minimizing R_{dson} and I_{DSS}. Optimizing these performance parameters with manufacturability in mind is one of the challenges of power MOSFET design.

The reach-through phenomenon, on the other hand, occurs when the depletion region on the drift side of the body-drift *pn*-junction reaches the epilayer-substrate interface before avalanching takes place in the epi. Once the depletion edge enters the high carrier concentration substrate, a further increase in drain voltage will cause the electric field to quickly reach the critical value of 2×10^5 V/cm at which avalanching begins.

Other factors that affect the breakdown voltage of power MOSFETs for a given epitaxial layer include termination design, cell spacing (poly line width) and curvature of the body diode depletion region in the epi which is a function of diffusion depth. Power MOSFETs are designed such that avalanche breakdown occurs in the active area first.

On-Resistance

The on-state resistance of a power MOSFET is made up of several components as shown in Fig. 1.62.

$$R_{dson} = R_{\text{source}} + R_{ch} + R_A + R_J + R_D + R_{\text{sub}} + R_{wcml} \tag{1.2}$$

where

R_{source} = source diffusion resistance
R_{ch} = channel resistance
R_A = accumulation resistance
R_J = the "JFET" component-resistance of the region between the two body regions
R_D = drift region resistance
R_{sub} = the substrate resistance; wafers with resistivities of up to 20 mΩ-cm are used for high-voltage devices and less than 5 mΩ-cm for low-voltage devices
R_{wcml} = sum of bond wire resistance, contact resistance between the source and drain metallization and the silicon, metallization resistance, and leadframe contributions; these are normally negligible in high-voltage devices but can become significant in low-voltage devices