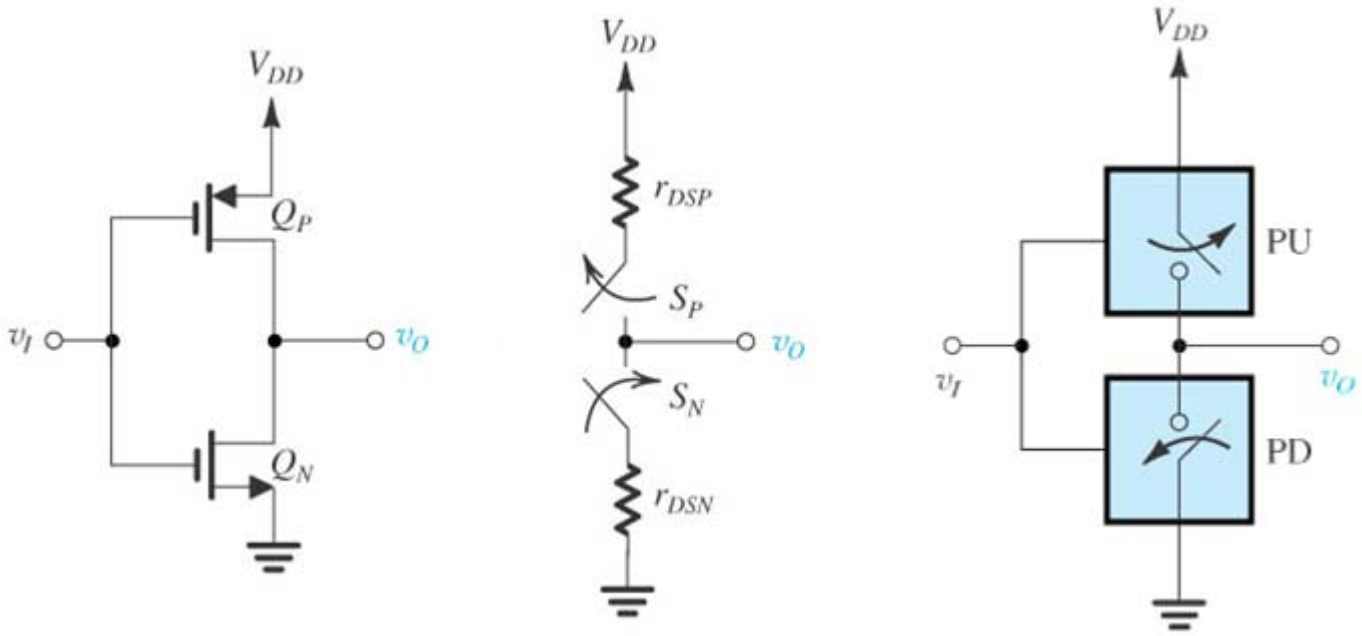
Digital CMOS Logic Circuits

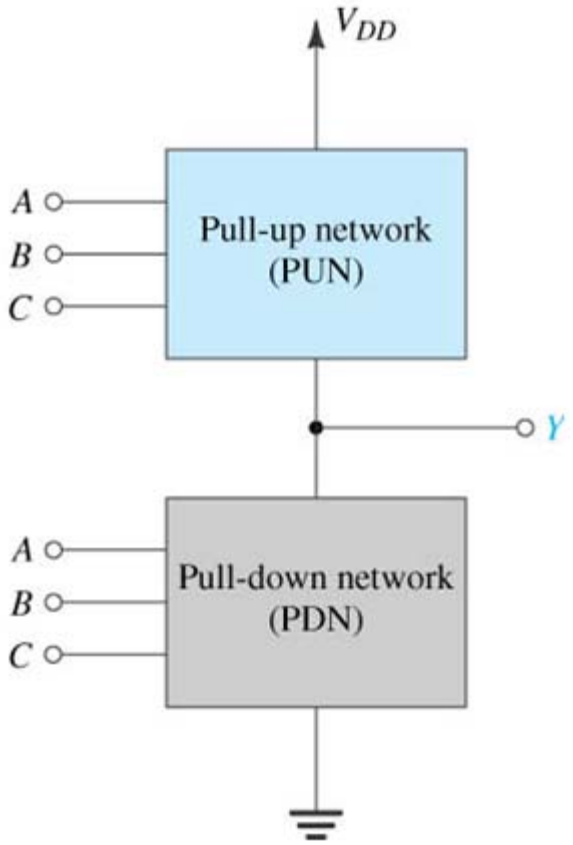
Sedra & Smith, Chapter 10



Inverter Circuit

CMOS Logic Gate Circuit

Similar structure to inverter:

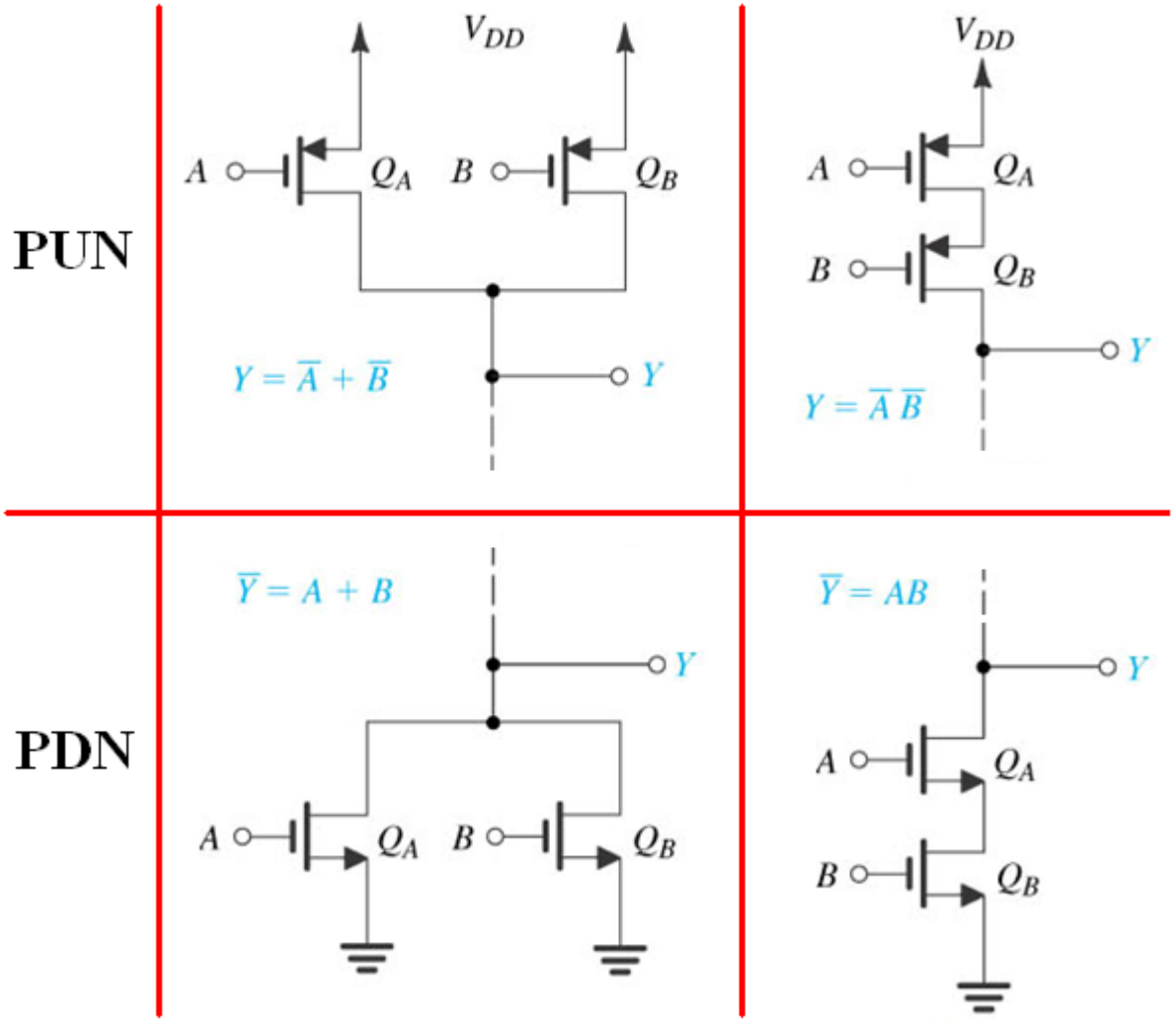


Network of PMOS transistors

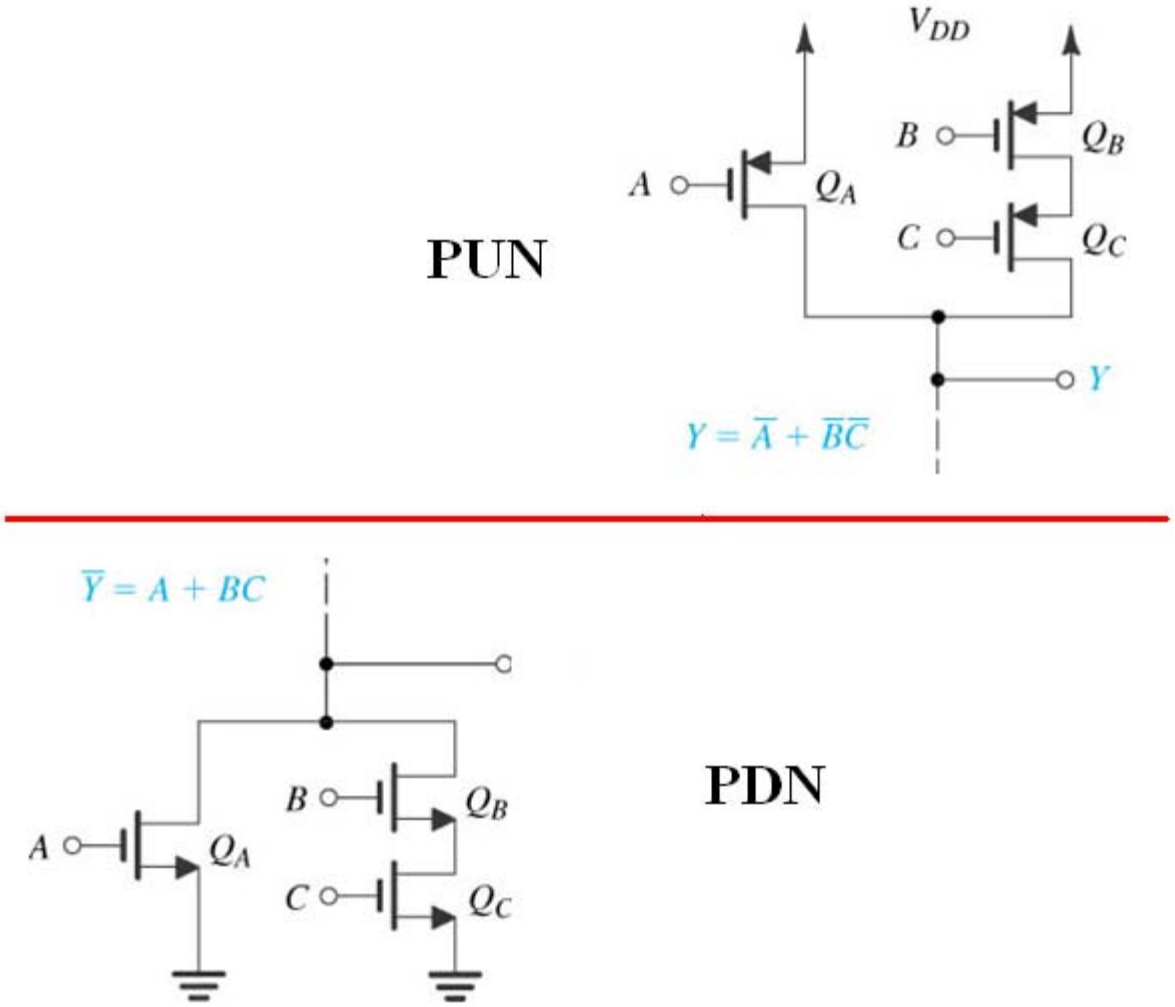
Network of NMOS transistors

PUN & PDN Basic Structure

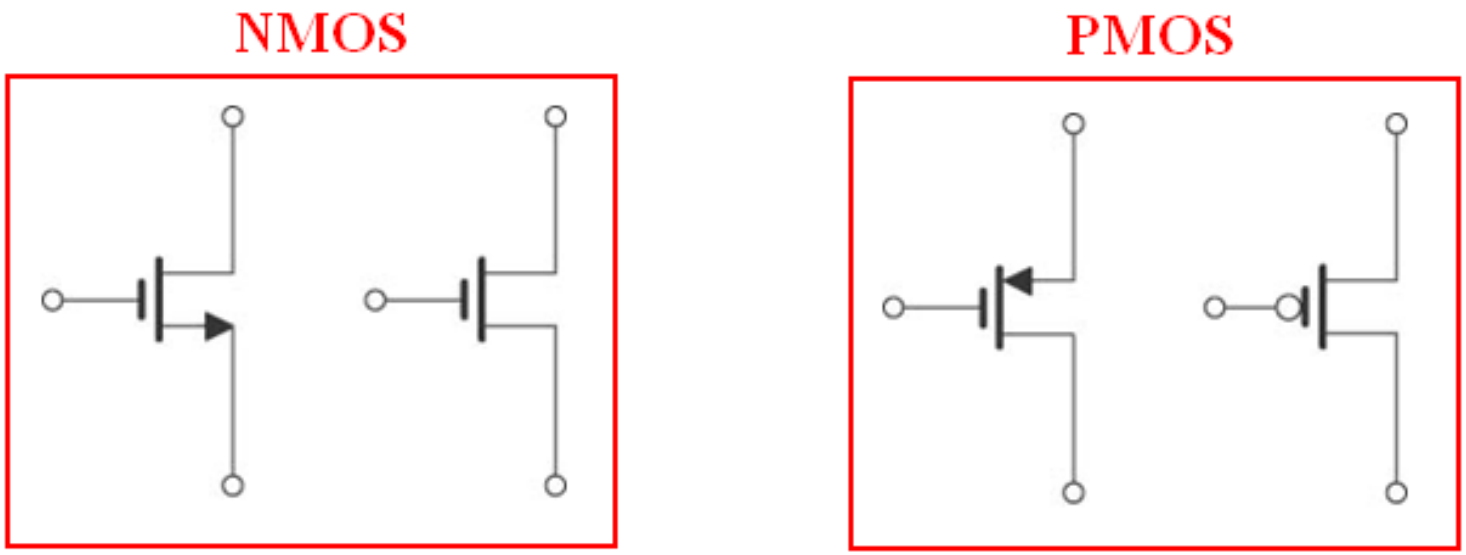
Parallel → OR Series → AND



Combinations of Basic Structures



Alternative (Digital) Symbols



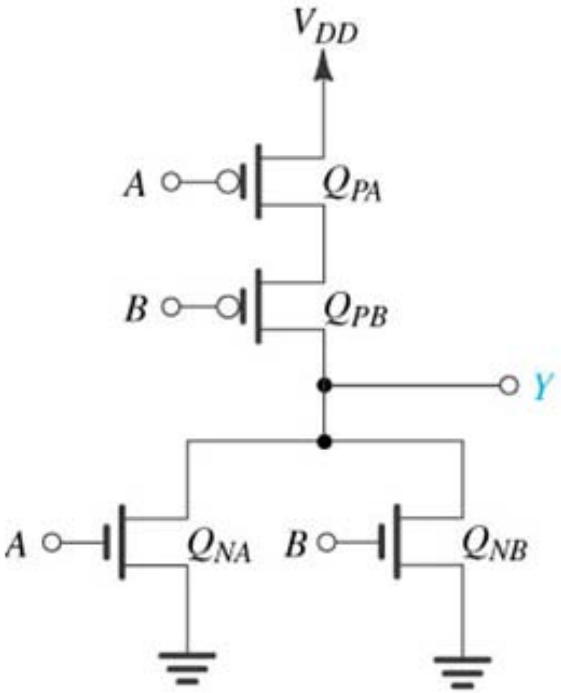
PMOS Active Low: Transistor is conducting (activated) when input is low.

2-input NOR

$$Y = \overline{A + B} = \bar{A}\bar{B}$$

$Y = \bar{A}\bar{B}$ Y is high (PUN conducting) when A AND B are Low.

$\bar{Y} = A + B$ Y is low (PDN conducting) when A OR B is High.

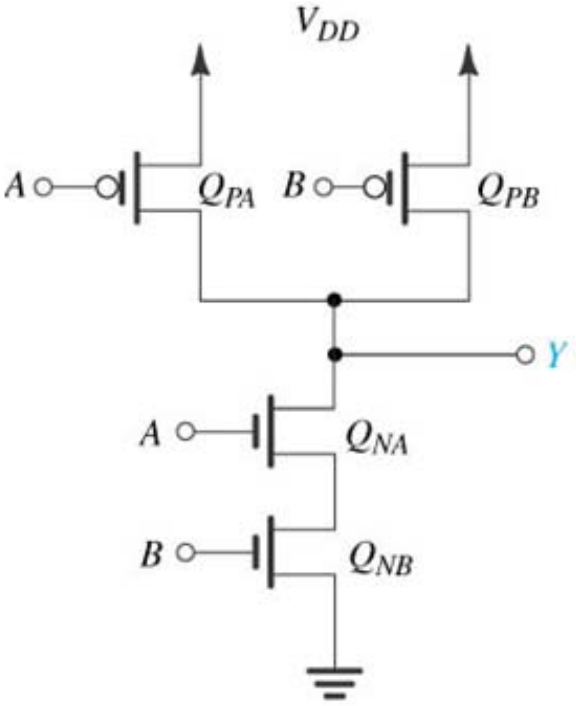


2-input NAND

$$Y = \overline{AB} = \bar{A} + \bar{B}$$

$Y = \bar{A} + \bar{B}$ Y is high (PUN conducting) when A OR B are Low.

$\bar{Y} = AB$ Y is low (PDN conducting) when A AND B are High.



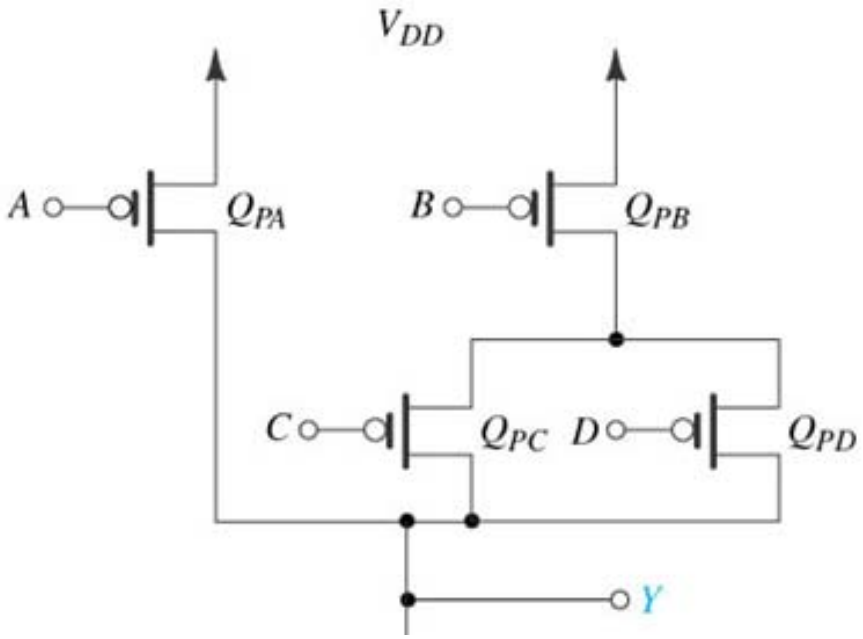
A Complex Gate

$$Y = \overline{A(B + CD)}$$

For PUN expression must be of Y in terms of the variables complements:

By DeMorgan's Law:

$$Y = \overline{A(B + CD)} = \bar{A} + \overline{(B + CD)} = \bar{A} + \bar{B}\overline{CD}$$
$$= \bar{A} + \bar{B}(\bar{C} + \bar{D})$$

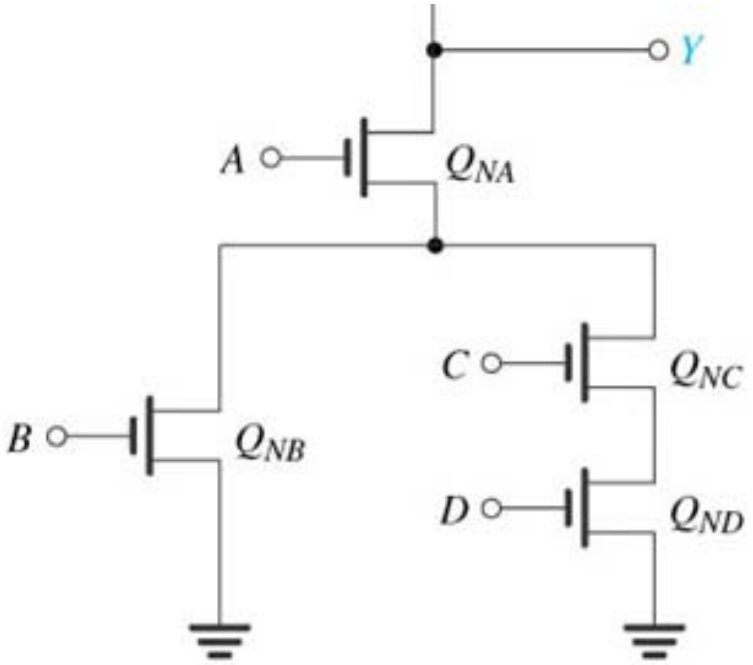


A Complex Gate

$$Y = \overline{A(B + CD)}$$

For PDN expression must be of $\bar{Y}$ in terms of the variables:

$$\bar{Y} = A(B + CD)$$

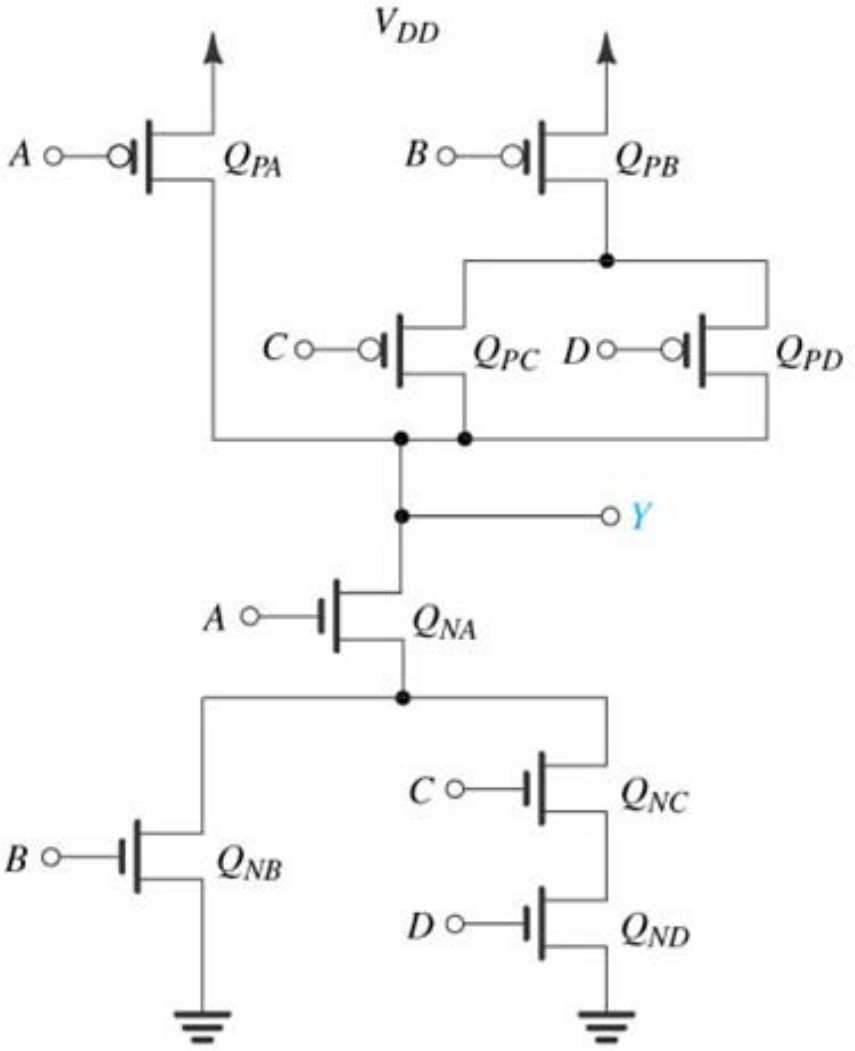


Complete Complex Gate

$$Y = \overline{A(B + CD)}$$

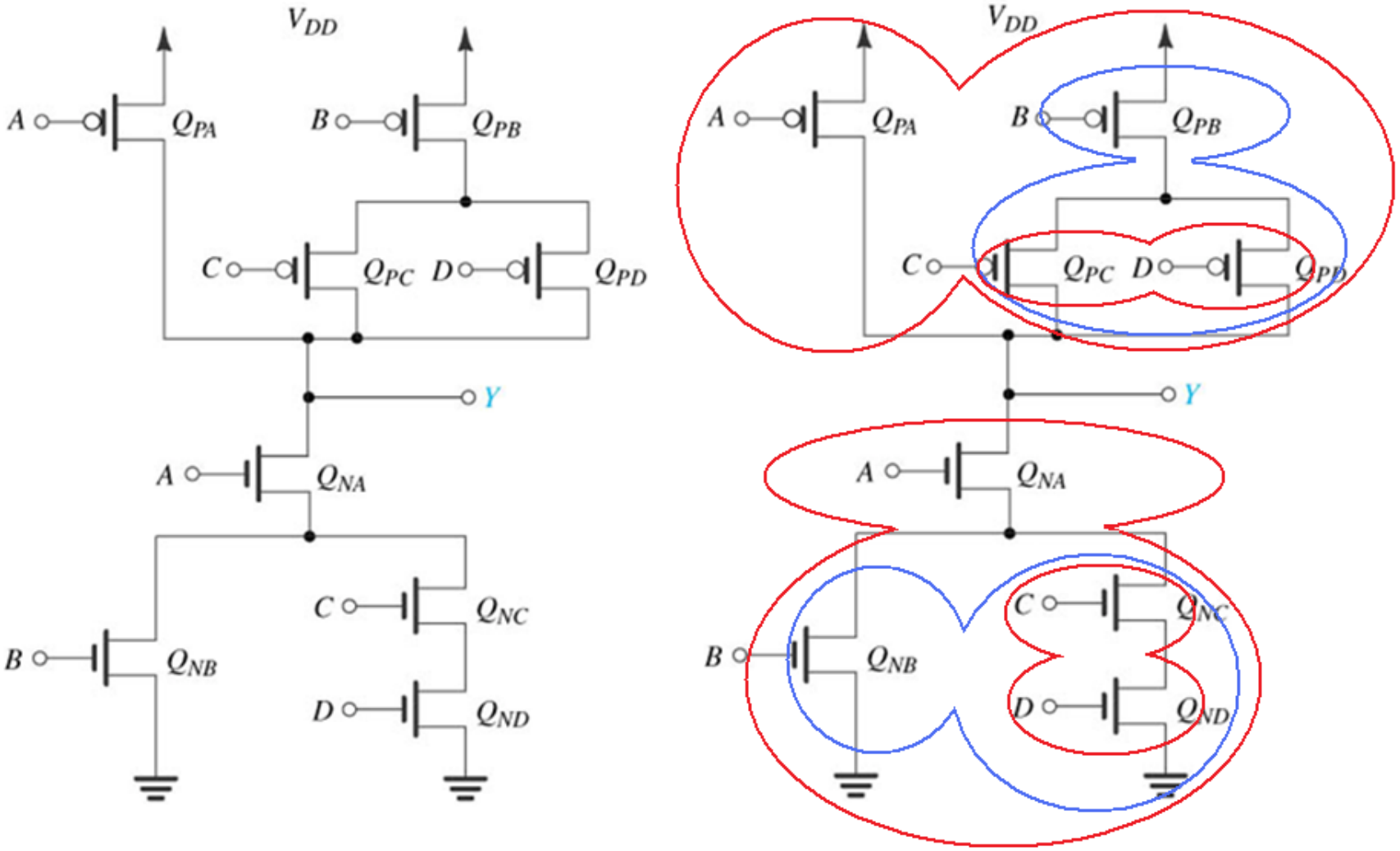
$$Y = \overline{A(B + CD)} = \bar{A} + \bar{B}(\bar{C} + \bar{D})$$

$$\bar{Y} = A(B + CD)$$



Note: Two transistors per variable.

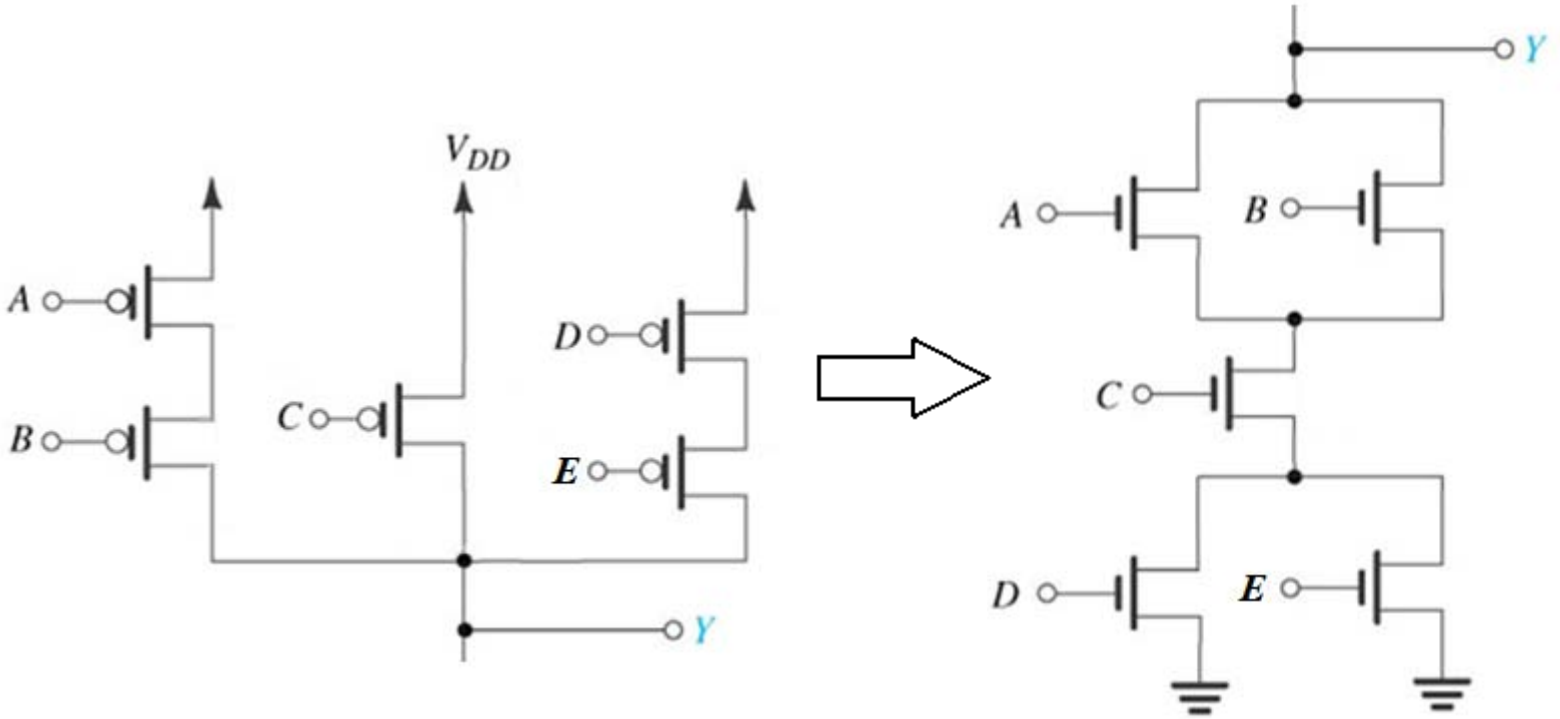
PUN/PDN Duality



Design by Duality

$$Y = \overline{A + B} + \overline{C(D + E)}$$

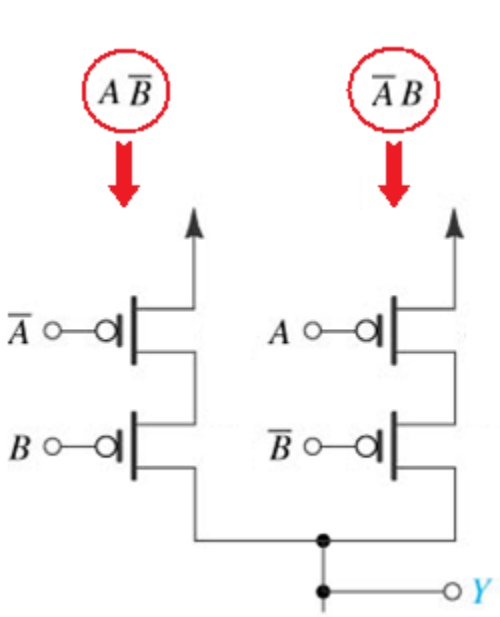
$$Y = \overline{A + B} + \overline{C(D + E)} = \bar{A}\bar{B} + \bar{C} + \overline{D + E} = \bar{A}\bar{B} + \bar{C} + \bar{D}\bar{E}$$

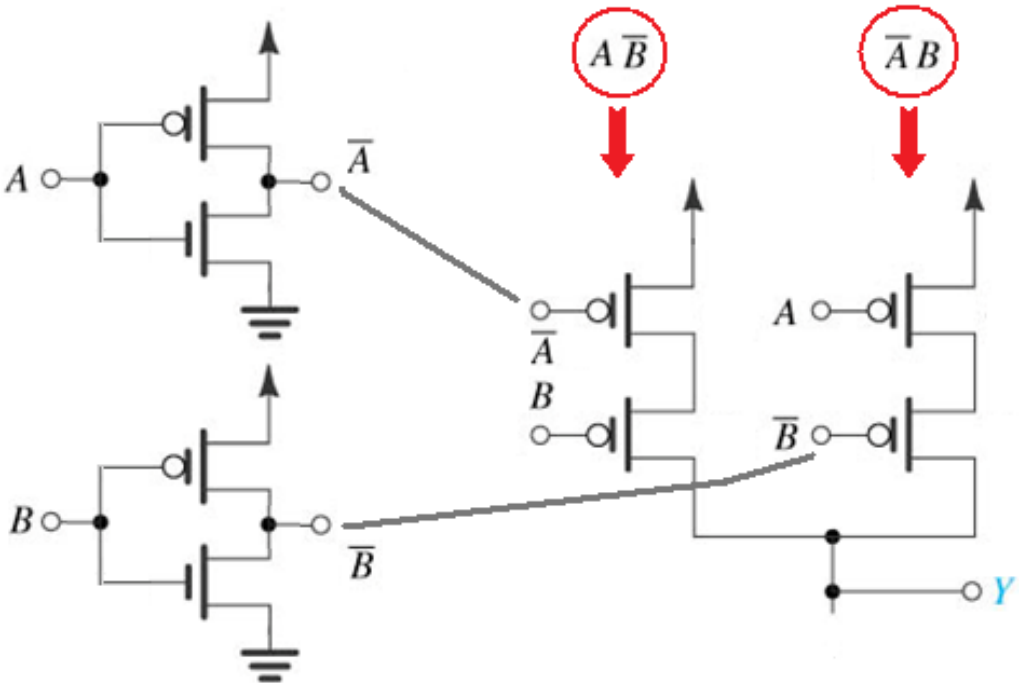


XOR PUN

$$Y = A\bar{B} + \bar{A}B$$

PUN

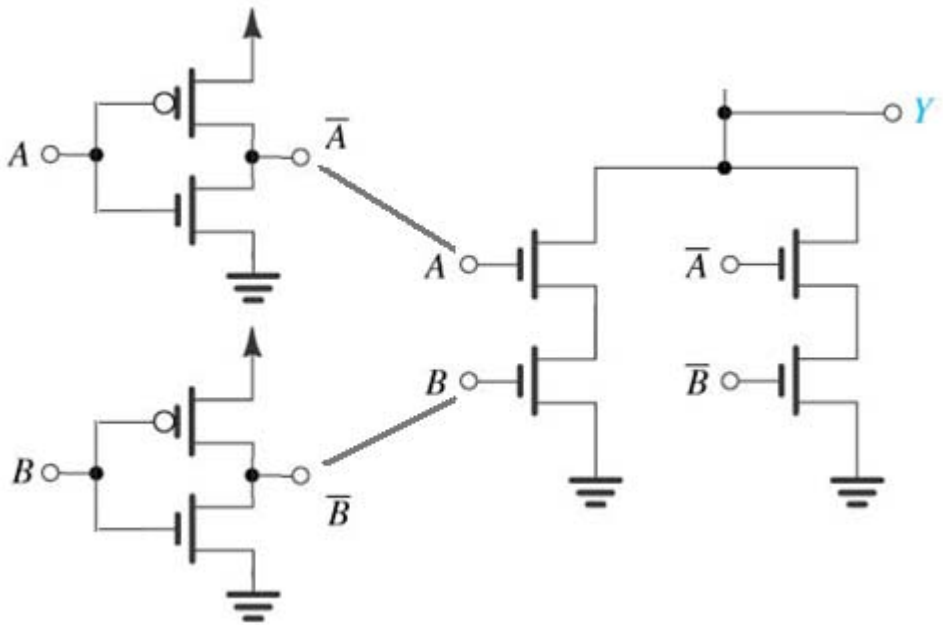




$$Y = \bar{\bar{A}}\bar{B} + \bar{A}\bar{\bar{B}}$$

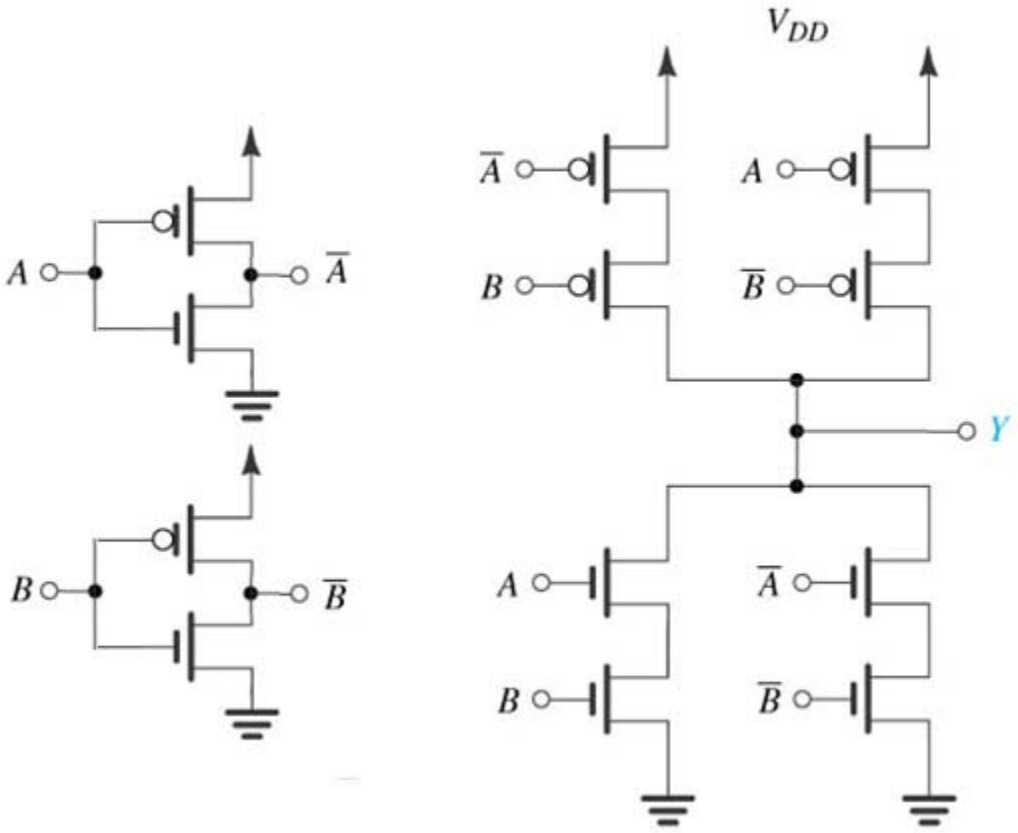
XOR PDN

$$\bar{Y} = \overline{A\bar{B} + \bar{A}B} = \overline{(A\bar{B})}\,\overline{(\bar{A}B)} = (\bar{A} + B)(A + \bar{B})$$
$$= A\bar{A} + AB + \bar{A}\bar{B} + B\bar{B} = AB + \bar{A}\bar{B}$$



Complete XOR

$$Y = A\bar{B} + \bar{A}B$$



Number of transistors is 12!

Transistor Sizing

$$I_{PUN} = I_{PDN} = I_{Inverter}$$

Define: $n = \frac{W_n}{L_n} \approx 1.5\ to\ 2$ and $p = \frac{W_p}{L_p} = n\frac{\mu_n}{\mu_p}$ recall $\frac{\mu_n}{\mu_p} \approx 2\ to\ 3$

$$r_{DS} \propto \frac{L}{W} \qquad R_{series} = r_{DS1} + r_{DS1} + \cdots = b\left(\frac{L}{W}\right)_1 + b\left(\frac{L}{W}\right)_2 + \cdots = b\left(\frac{L}{W}\right)_{eq}$$

$$\left(\frac{W}{L}\right)_{series,eq} = \frac{1}{\frac{1}{(W/L)_1} + \frac{1}{(W/L)_2} + \cdots}$$

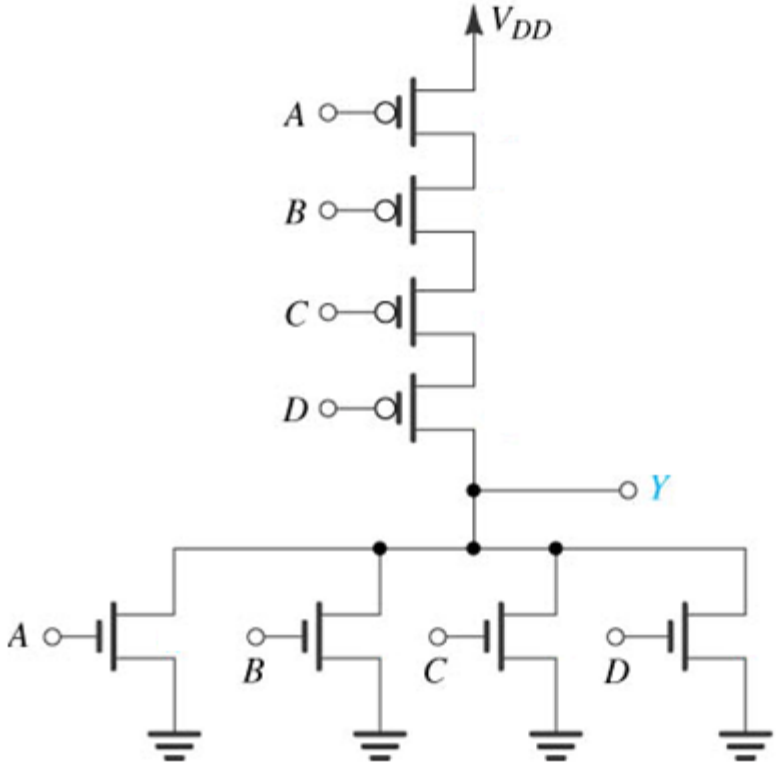
Similarly $\left(\frac{W}{L}\right)_{parallel,eq} = (W/L)_1 + (W/L)_2 + \cdots$

If $\frac{W}{L} = 4$ then for two transistors $\left(\frac{W}{L}\right)_{series} = 2$ and $\left(\frac{W}{L}\right)_{parallel} = 8$

Transistor Sizing Example-1

$$\left(\frac{W}{L}\right)_{series} = \frac{1}{4\frac{1}{(W/L)}} = \frac{1}{4}\left(\frac{W}{L}\right)$$

$$\left(\frac{W}{L}\right)_{parallel} = 4\left(\frac{W}{L}\right)$$



Design	
4p	
4p	
4p	
4p	
n	*n* *n* *n*

Design with worst case in mind.

Transistor Sizing Example-2

Let $n = 1.5, p = 5, L = 0.25\mu m.$

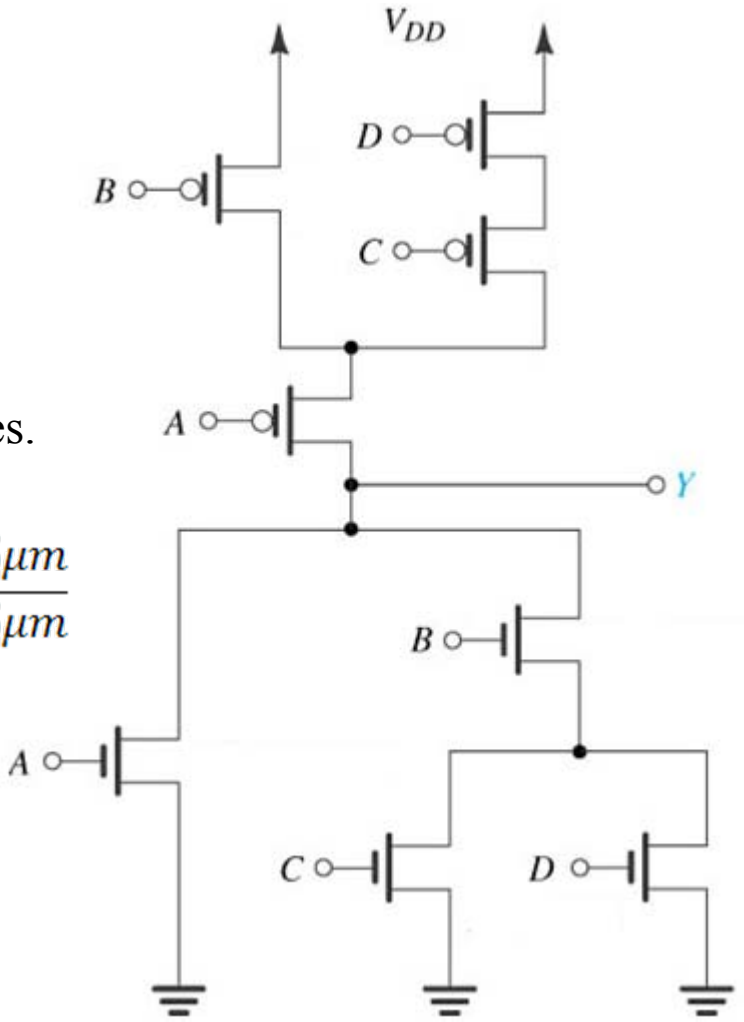
Calculate *W/L* for all transistors.

PDN worst case:

Q_{NB} and (Q_{NC} or Q_{ND}) ON. → 2 transistors in series.

$$\left(\frac{W}{L}\right)_{Q_{NB}} = \left(\frac{W}{L}\right)_{Q_{NC}} = \left(\frac{W}{L}\right)_{Q_{ND}} = 2n = 3 = \frac{0.75\mu m}{0.25\mu m}$$

$$\left(\frac{W}{L}\right)_{Q_{NA}} = n = 1.5 = \frac{0.375\mu m}{0.25\mu m}$$



Transistor Sizing Example-2

PUN worst case:

Q_{PA} and Q_{PC} and Q_{PD} ON. → 3 transistors in series.

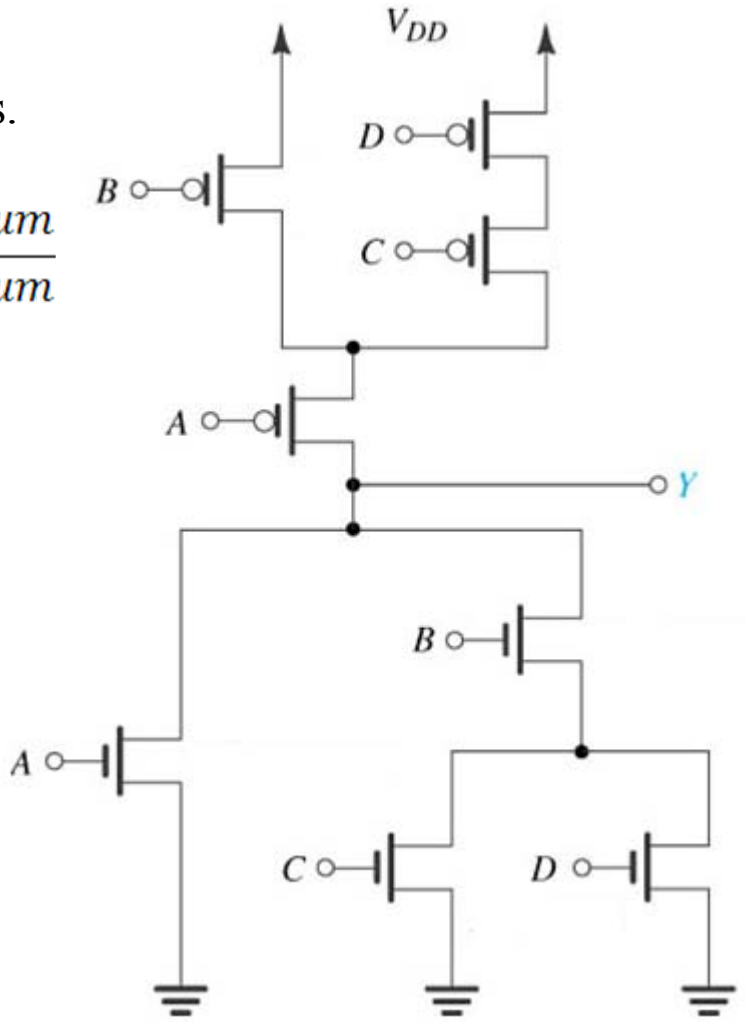
$$\left(\frac{W}{L}\right)_{Q_{PA}} = \left(\frac{W}{L}\right)_{Q_{PC}} = \left(\frac{W}{L}\right)_{Q_{PD}} = 3p = 15 = \frac{3.75\mu m}{0.25\mu m}$$

Q_{PA} and Q_{PB} ON. → 2 transistors in series.
Q_{PA} fixed:

$$\left(\frac{W}{L}\right)_{Q_P} = \frac{1}{\frac{1}{(W/L)_{Q_{PA}}} + \frac{1}{(W/L)_{Q_{PB}}}}$$

$$p = \frac{1}{\frac{1}{3p} + \frac{1}{xp}} = \frac{3p}{1 + \frac{3}{x}} \rightarrow 1 + \frac{3}{x} = 3 \rightarrow x = 1.5$$

$$\left(\frac{W}{L}\right)_{Q_{PB}} = 1.5p = 7.5 = \frac{1.875\mu m}{0.25\mu m}$$



Fan-in & Fan-out VS. Propagation Delay

Fan-in ↑

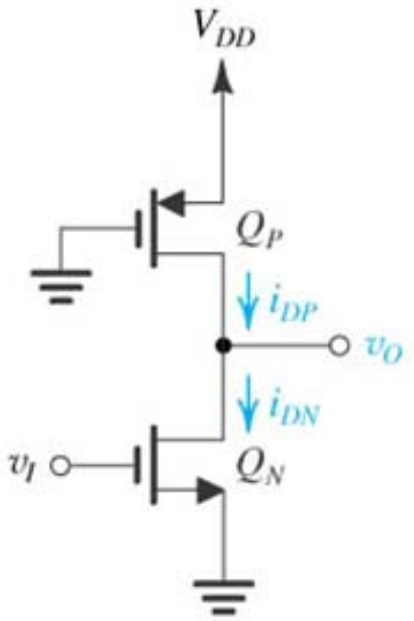
additional input → 2 extra transistors
- → chip area ↑
- → C_{EQ} ↑ → t_P ↑

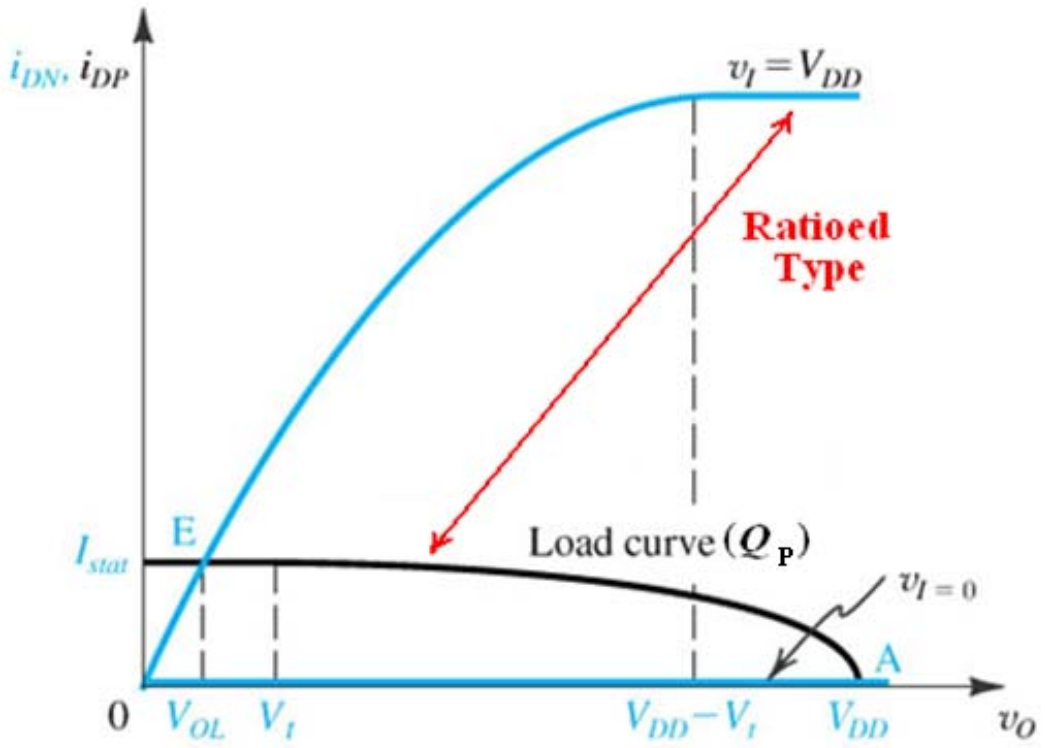
Fan-out ↑

additional output → C_{load} ↑ → C_{EQ} ↑ → t_P ↑

Also more complex circuits for both cases.

Pseudo-NMOS Inverter





Advantages:
- One gate per input.
-Less loading capacitance.
- Smaller Area.

Pseudo-NMOS Logic Static Characteristics

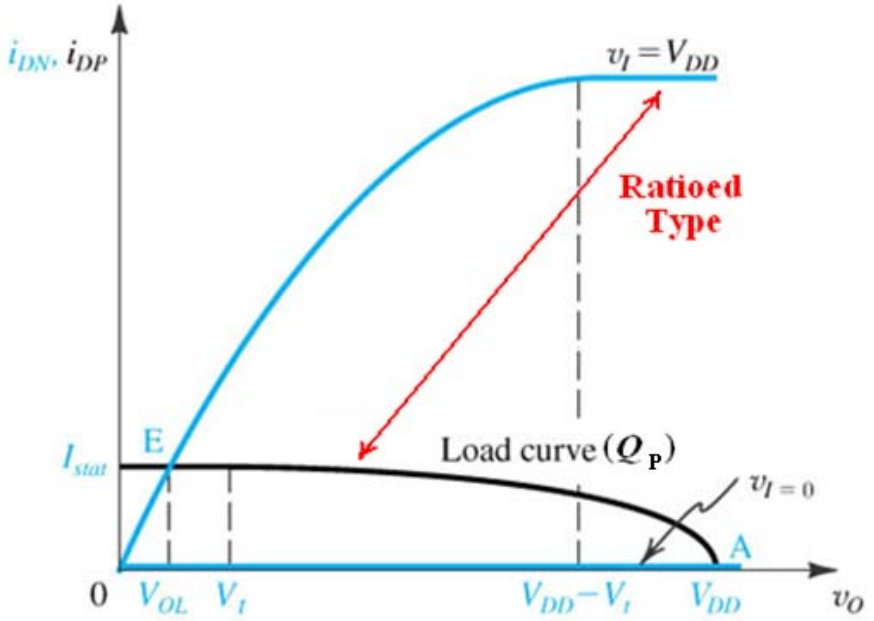
Point E

Q_P saturation:

$$i_{DP} = \frac{1}{2} k_p (V_{DD} - V_t)^2$$

Q_N triode:

$$i_{DN} = k_n \left[(v_I - V_t) v_O - \frac{1}{2} v_O^2 \right]$$



Point A

Q_P triode:

$$i_{DP} = k_p \left[(V_{DD} - V_t)(V_{DD} - v_O) - \frac{1}{2} (V_{DD} - v_O)^2 \right]$$

Q_N saturation (cutoff):

$$i_{DN} = \frac{1}{2} k_n (v_I - V_t)^2$$

Ratioed Type

$$k_n = k_n' \left(\frac{W}{L} \right)_n \qquad k_n = k_p' \left(\frac{W}{L} \right)_p \qquad r \equiv \frac{k_n}{k_p}$$

Pseudo-NMOS Logic V_{OH} and V_{OL}

For v_I=0 (point A)

Q_P triode, Q_N cutoff

$$i_P = 0, v_{DSP} = 0$$

$$v_O = V_{OH} = V_{DD}$$

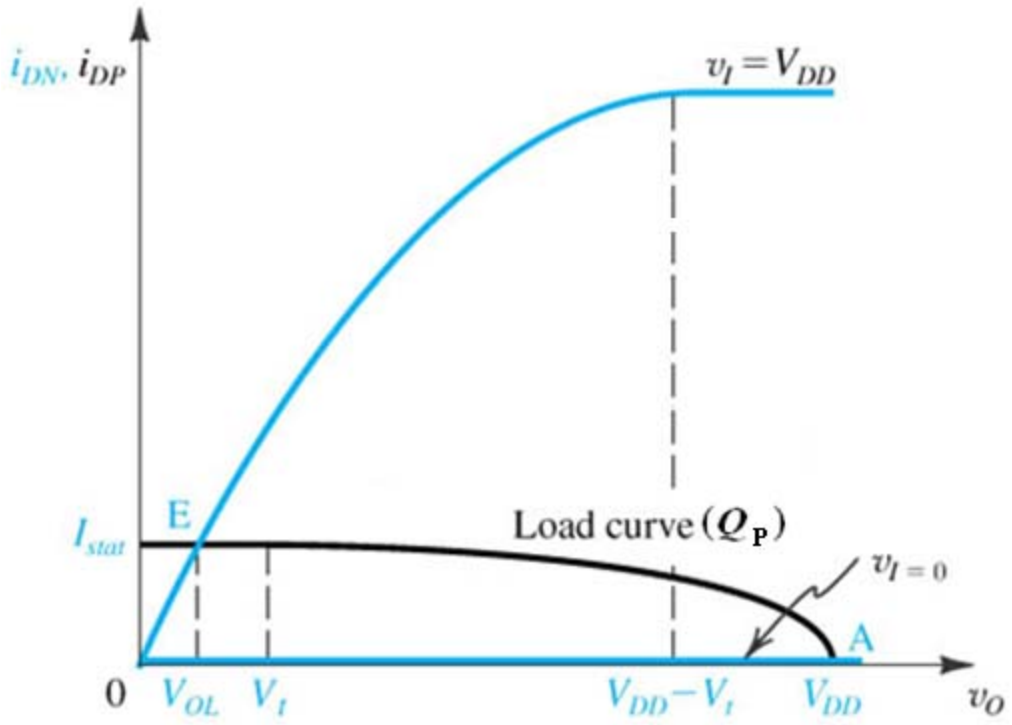
For v_I=V_{DD} (point E)

Q_P saturation, Q_N triode

$$v_O = V_{OL} \neq 0$$

Gate conducts (static) current I_{stat} !

$$P_D = I_{stat} \times V_{DD}$$



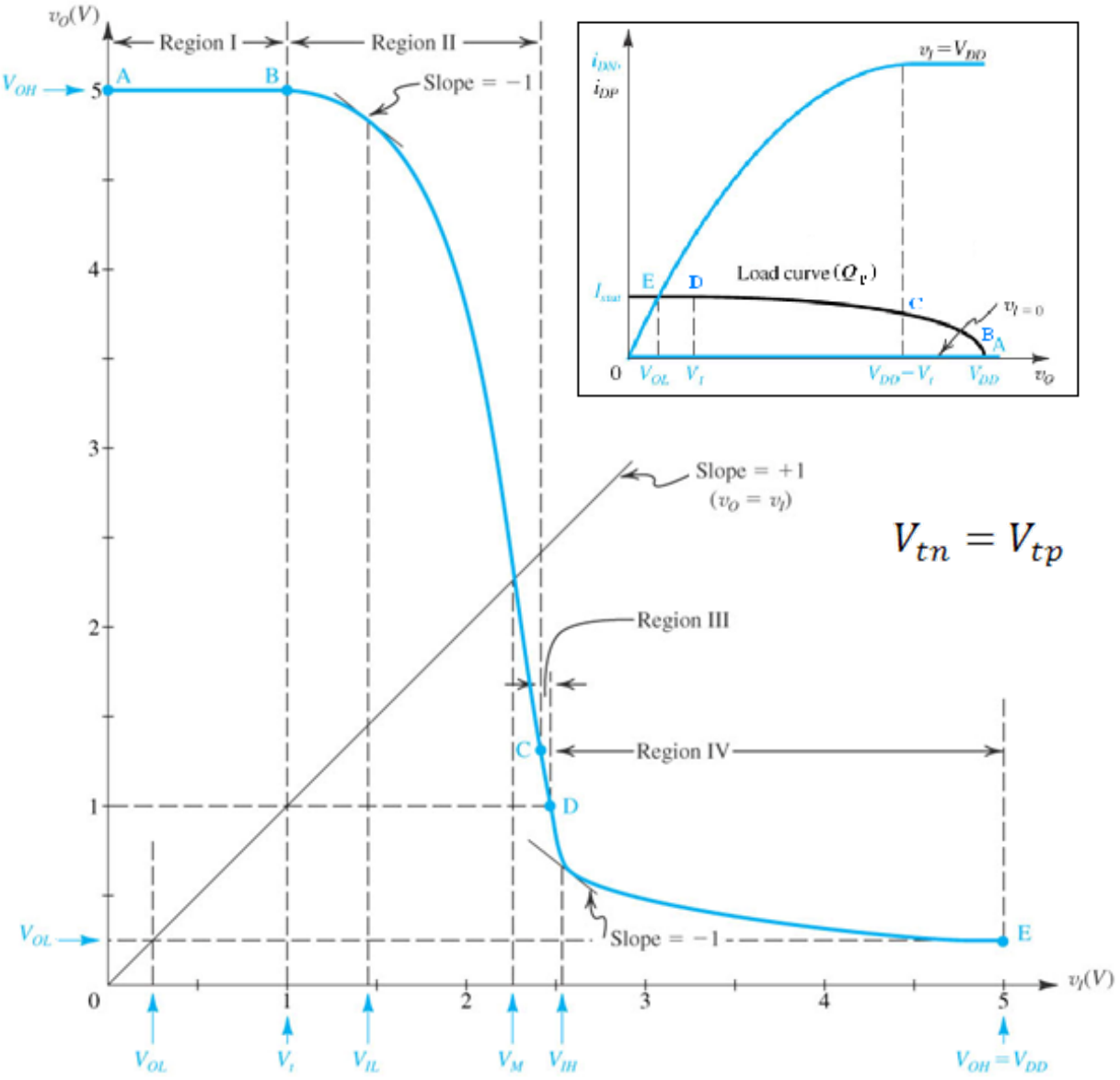
Pseudo-NMOS Logic VTC

Region I (AB)
Q_P triode, Q_N cutoff

Region II (BC)
Q_P triode, Q_N saturation

Region III (CD)
Q_P triode, Q_N triode

Region IV(DE)
Q_P saturation, Q_N triode



Pseudo-NMOS Logic VTC Regions I & II

Region I $v_I < V_t$

Q_P triode, Q_N cutoff

$$v_O = V_{OH} = V_{DD}$$

Region II $v_O \geq v_I - V_t$

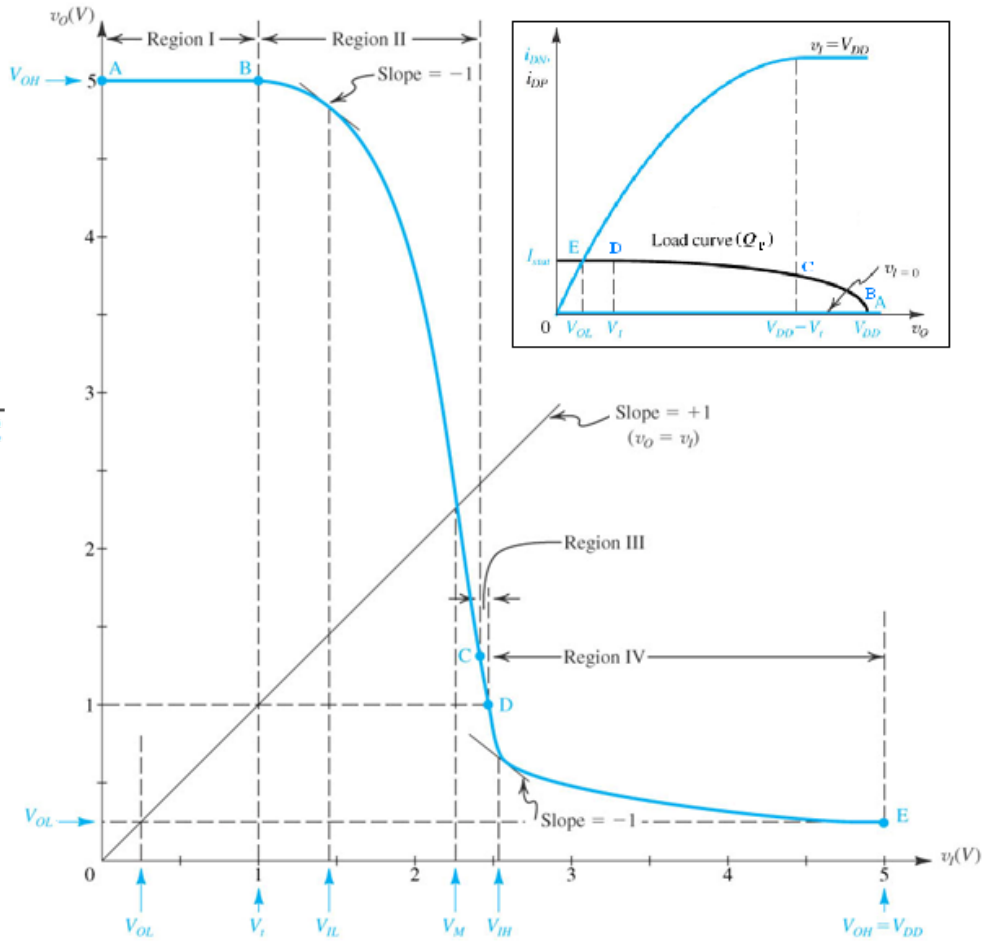
Q_P triode, Q_N saturation

$$v_O = V_t + \sqrt{(V_{DD} - V_t)^2 - r(v_I - V_t)^2}$$

Setting $\frac{dv_O}{dv_I} = -1 \text{ and } v_I = V_{IL}$

$$V_{IL} = V_t + \frac{V_{DD} - V_t}{\sqrt{r(r+1)}}$$

$$V_M|_{v_O = v_I} = V_t + \frac{V_{DD} - V_t}{\sqrt{r+1}}$$



Pseudo-NMOS Logic VTC Regions III & IV

Region III
Q_P triode, Q_N triode
Not significant.

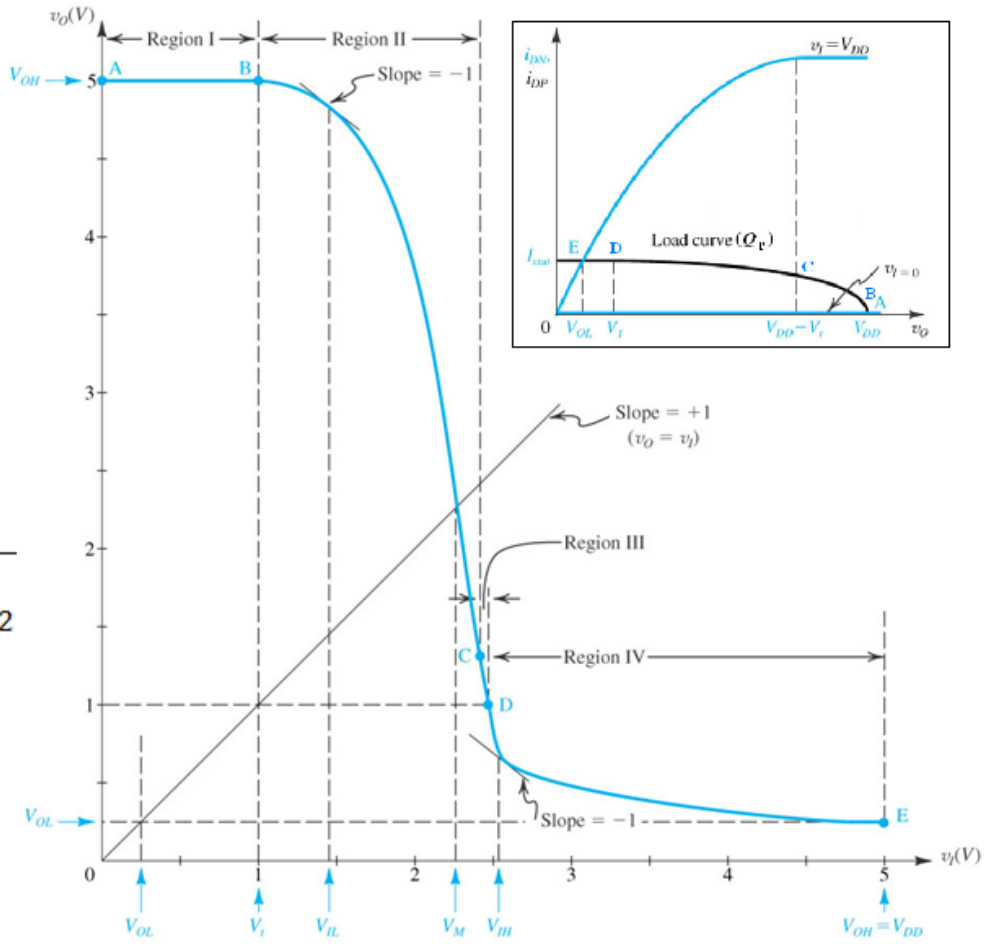
Point C: Set $v_O = v_I - V_t$ in region II
v_O formula.
Point D: $v_O = V_t$

Region IV
Q_P saturation, Q_N triode

$$v_O = v_I - V_t - \sqrt{(v_I - V_t)^2 - \frac{1}{r}(V_{DD} - V_t)^2}$$

Setting $\frac{dv_O}{dv_I} = -1 \text{ and } v_I = V_{IH}$

$$V_{IH} = V_t + \frac{2}{\sqrt{3r}}(V_{DD} - V_t)$$



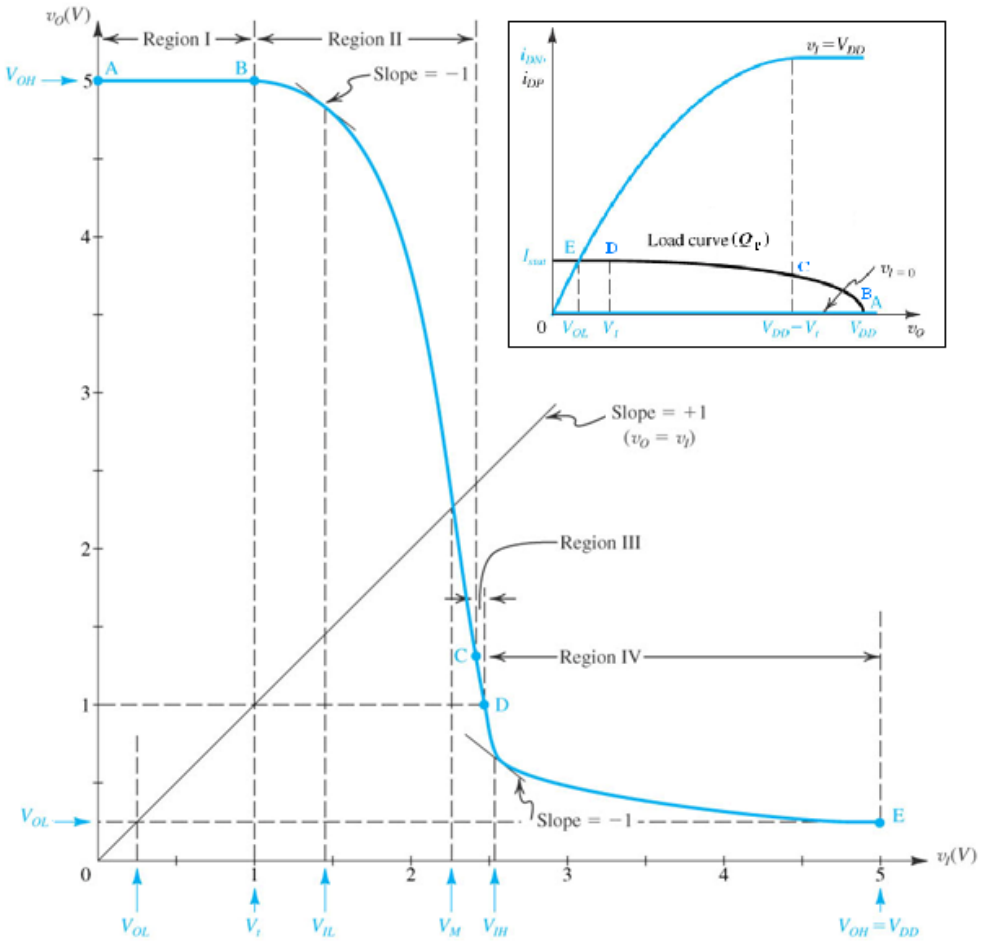
Pseudo-NMOS Logic V_{OL} & I_{stat}

Set $v_I = V_{DD}$ in region IV v_O formula:

$$V_{OL} = (V_{DD} - V_t)\left(1 - \sqrt{1 - \frac{1}{r}}\right)$$

Static current is Q_P current in saturation

$$I_{stat} = \frac{1}{2} k_p (V_{DD} - V_t)^2$$

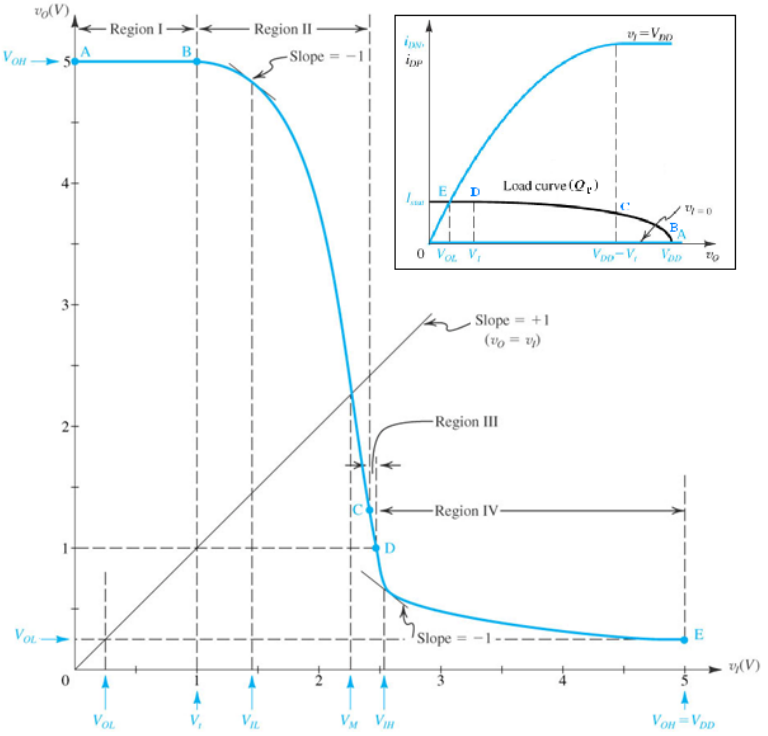


Noise Margins for Pseudo-NMOS Logic

$$NML = V_t - (V_{DD} - V_t)\left(1 - \sqrt{1 - \frac{1}{r} - \frac{1}{\sqrt{r(r+1)}}}\right)$$

$$NMH = (V_{DD} - V_t)\left(1 - \frac{2}{\sqrt{3r}}\right)$$

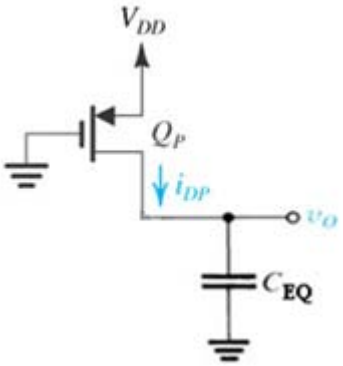
By controlling the ratio $r=k_n/k_p$ we can adjust the noise margins and V_{OL}.



Pseudo-NMOS Dynamic Operation

t_{PLH}

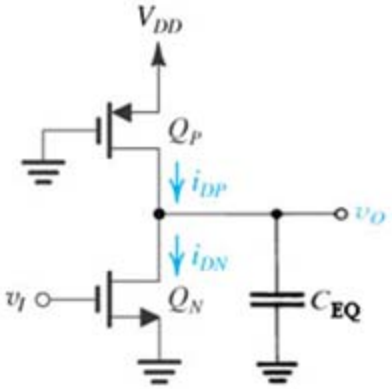
Similar to CMOS.



$$t_{PLH} = \frac{1.7C_{EQ}}{k_p V_{DD}}$$

t_{PHL}

Not so similar to CMOS.



Must subtract i_{DP} from i_{DN}.

$$t_{PHL} = \frac{1.7C_{EQ}}{k_n\left(1 - \frac{0.46}{r}\right)V_{DD}}$$

If r is large the formulas will look identical but:

$$r \equiv \frac{k_n}{k_p}$$

So t_{PLH} will be r times t_{PHL}. → Asymmetrical delay.

Pseudo-NMOS Logic Design Considerations

Design of either P or N MOSFET ratio *r* and *W/L* is chosen. The design of the counterpart is determined by the ratio *r*.

Ratio $r \uparrow$

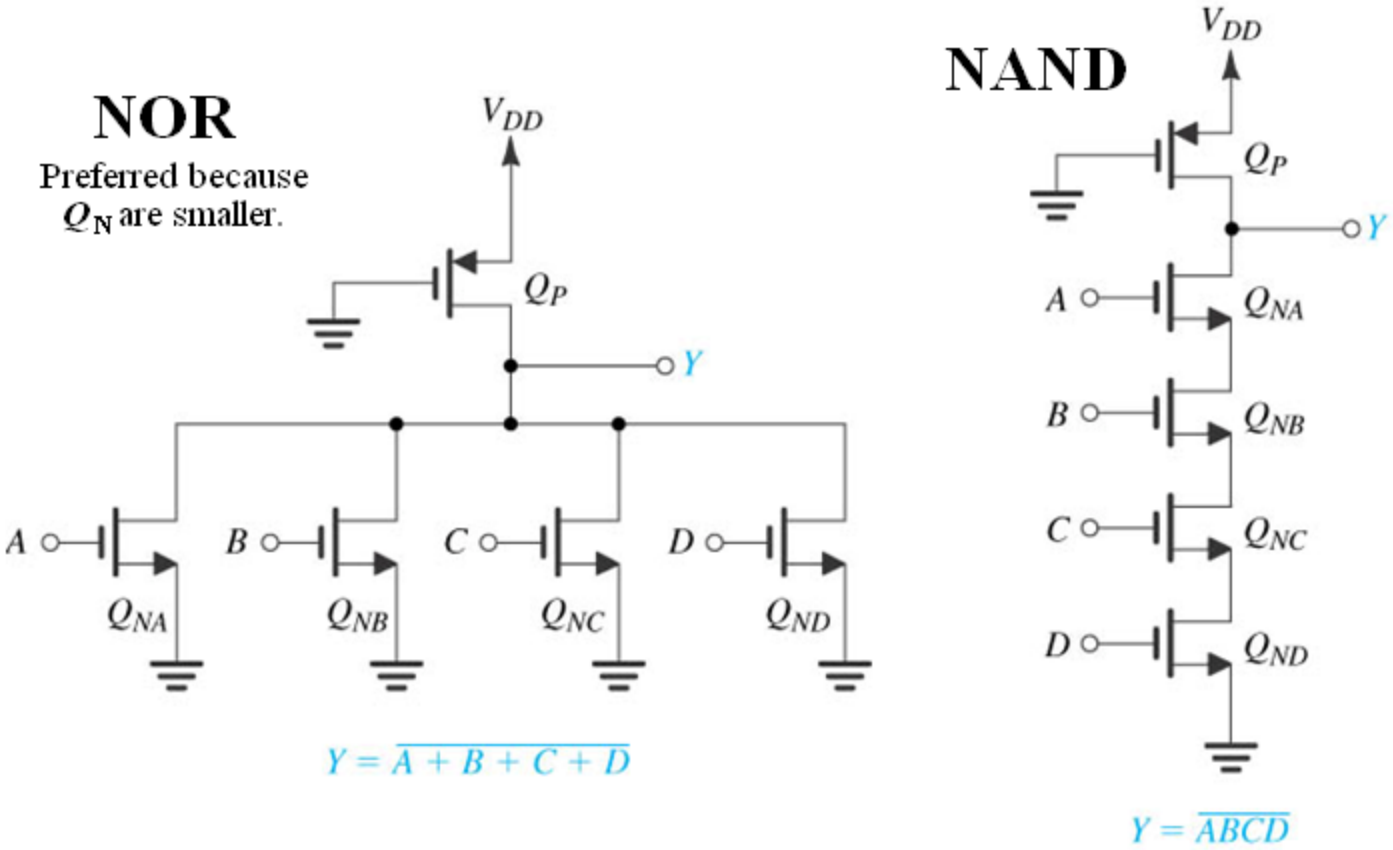
- $V_{OL} \downarrow$
- *NML* & *NMH* $\uparrow$
- Asymmetry of $t_P \uparrow$
- $(W/L)_P$ (size) $\uparrow$

$W/L \downarrow$

- $C \downarrow$
- Size $\downarrow$
- $I_{Stat} \downarrow$
- $P_D \downarrow$
- $t_P \uparrow$

Pseudo-NMOS Logic Circuit

PDN same as for CMOS.



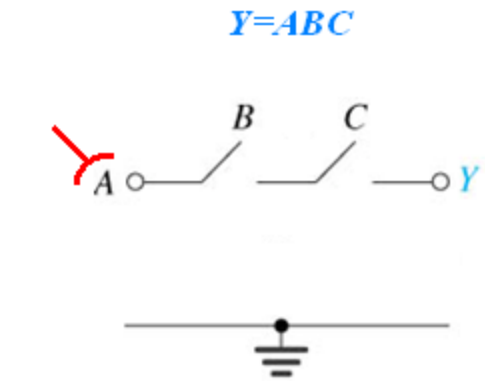
Less transistors than CMOS.

Most used in RAMs, memory decoders, and when output is mostly high.

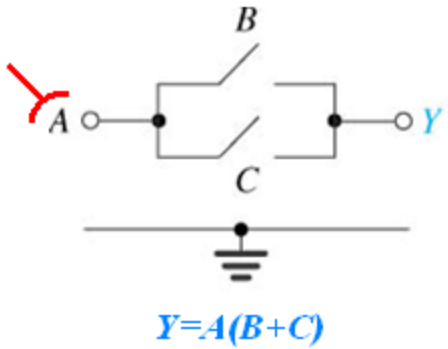
Pass-Transistor Logic (PTL)

Transmission-Gate Logic

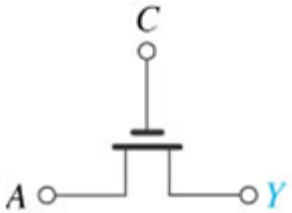
Use logic variables to connect another input variable to output.



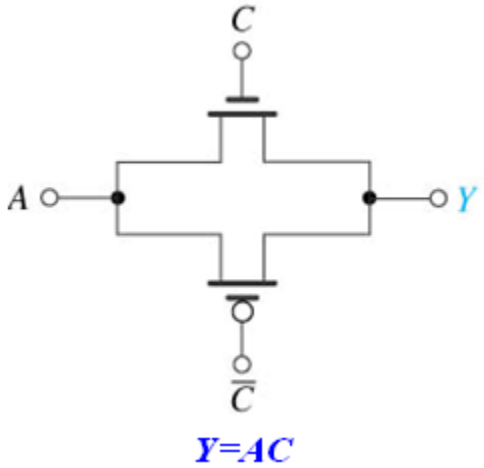
Used with CMOS gates.



PTL Switch Types



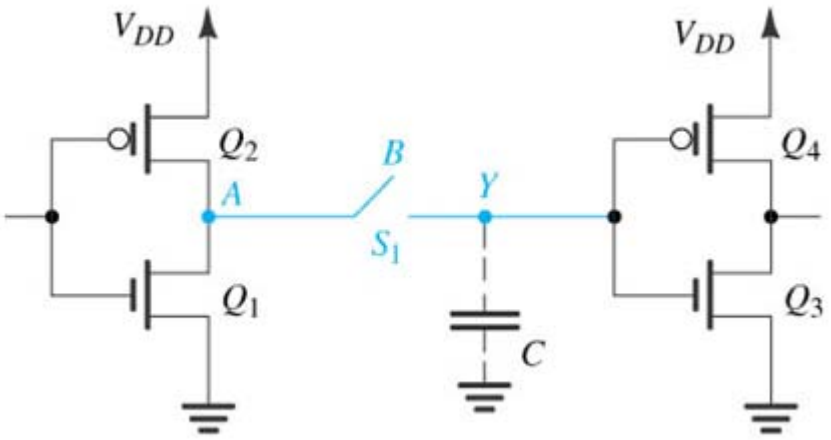
Single NMOS Transistor



Two complimentary CMOS Transistors.
CMOS Transmission Gate

PTL Needs Path to V_{DD}/Ground

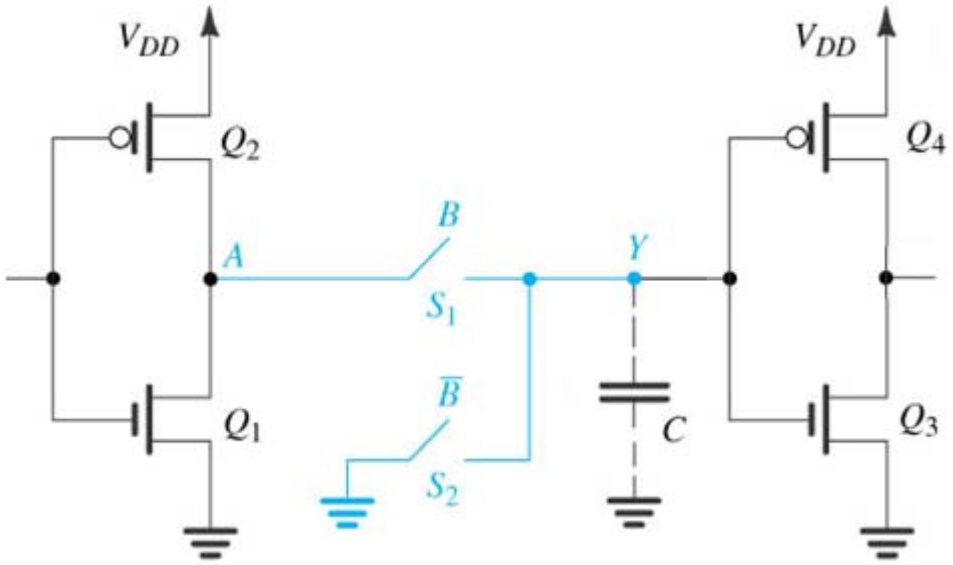
Y=AB



B	S_1		*A*	*Y*
High	Closed	*Y=A*	Low	Low
			High	High
Low	Open	*Y=?*	Was Low	Low
			Was High	Slow Discharge!

Not a static combinational logic circuit!

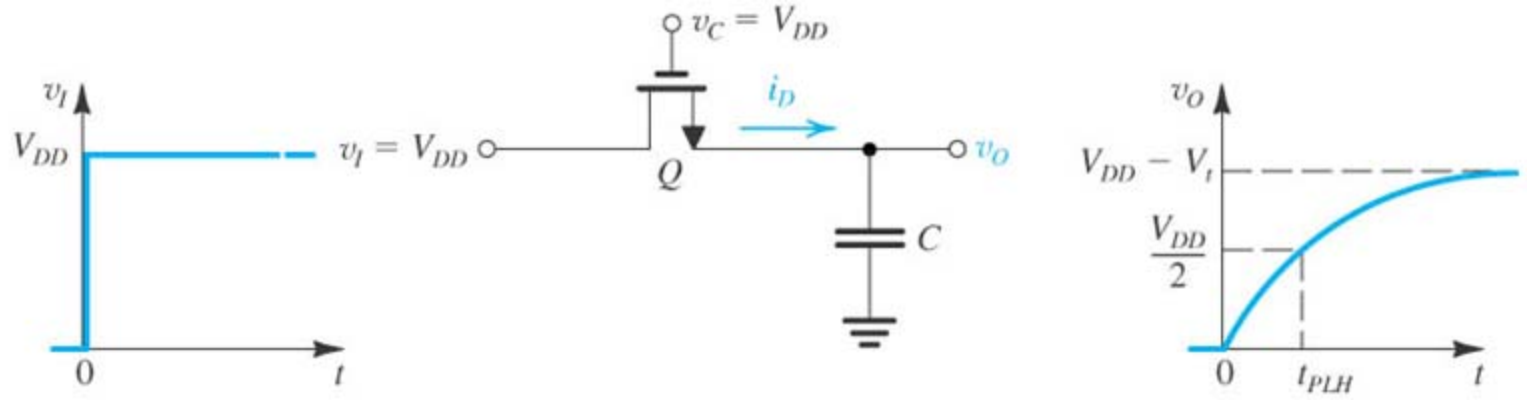
PTL Path to V_{DD}/Ground Solved



S_2 low resistance path to ground.

Every node must always have a low resistance path to V_{DD} or ground.

Single NMOS & Body Effect



When v_I goes high Q will be in saturation.

$$i_D = \frac{1}{2} k_n (V_{DD} - v_O - V_t)^2$$

Body Effect: $$V_t = V_{t0} + \gamma \left(\sqrt{v_O - 2\emptyset_f} - \sqrt{2\emptyset_f} \right)$$

Body connected to source at v_O.

1- As $v_O \uparrow \longrightarrow V_t \uparrow$ and $i_D \downarrow \longrightarrow$ Charging will be slowed.

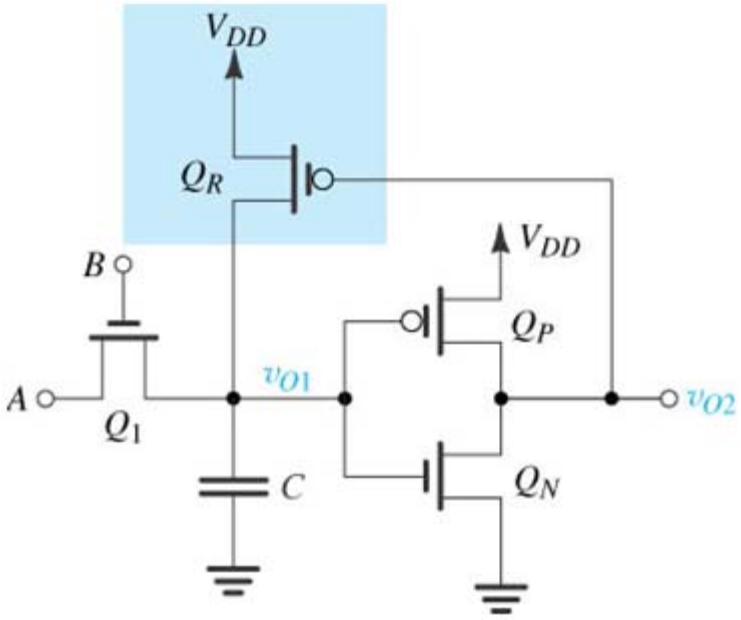
2- When $v_O = V_{DD} - V_t$ the current $i_D = 0 \longrightarrow V_{OH} = V_{DD} - V_t$ (poor 1).

3- Because $V_{OH} = V_{DD} - V_t$ load Q_P will conduct $\longrightarrow P_D \neq 0$.

Restoration of V_{DD}

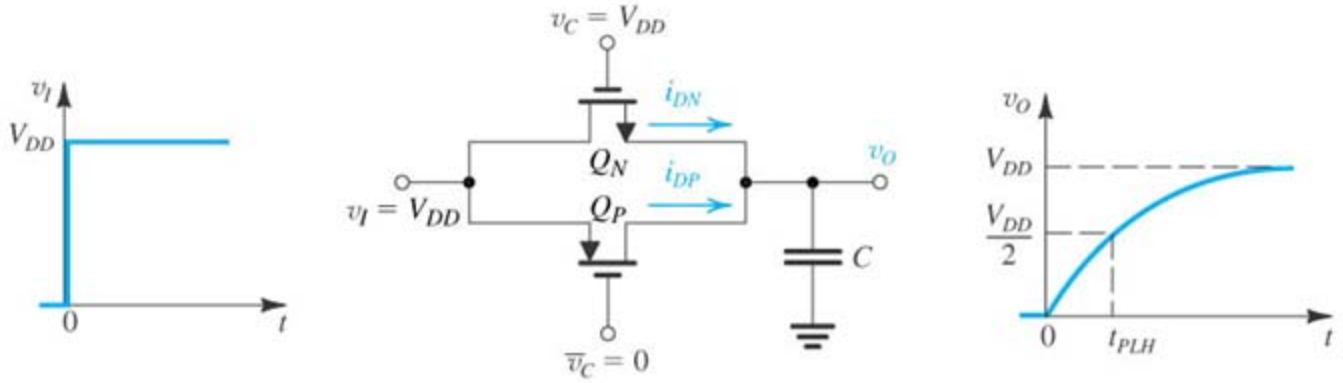
v_{O1}	v_{O1}	Q_R
Low	High	Off
Poor High	Low	On

When Q_R is on it will charge C up to V_{DD} (good High).
Warning: Positive feedback!



Or use special transistors with small V_t preferably V_t =0V.

CMOS Transmission Gates



Switch=On

$V_{DSN}=V_{DD}$ & $V_{GSN}=V_{DD}$ Q_N in saturation.

$$i_{DN} = \frac{1}{2}k_n(V_{DD} - v_O - V_{tn})^2 \qquad \& \qquad V_{tn} = V_{t0} + \gamma\left(\sqrt{v_O - 2\emptyset_f} - \sqrt{2\emptyset_f}\right)$$

i_{DN} is going down again!

What about Q_P ?

$V_{DSP}=-V_{DD}$ & $V_{GSP}=-V_{DD}$ Q_P also in saturation.

$$i_{DP} = \frac{1}{2}k_p(V_{DD} - |V_{tp}|)^2$$

No body effect. Why?

Q_P will continue to conduct after $v_O=|V_{tp}|$ until $v_O=V_{DD}= V_{OH}$.

Transmission Gate Vs. Single Transistor

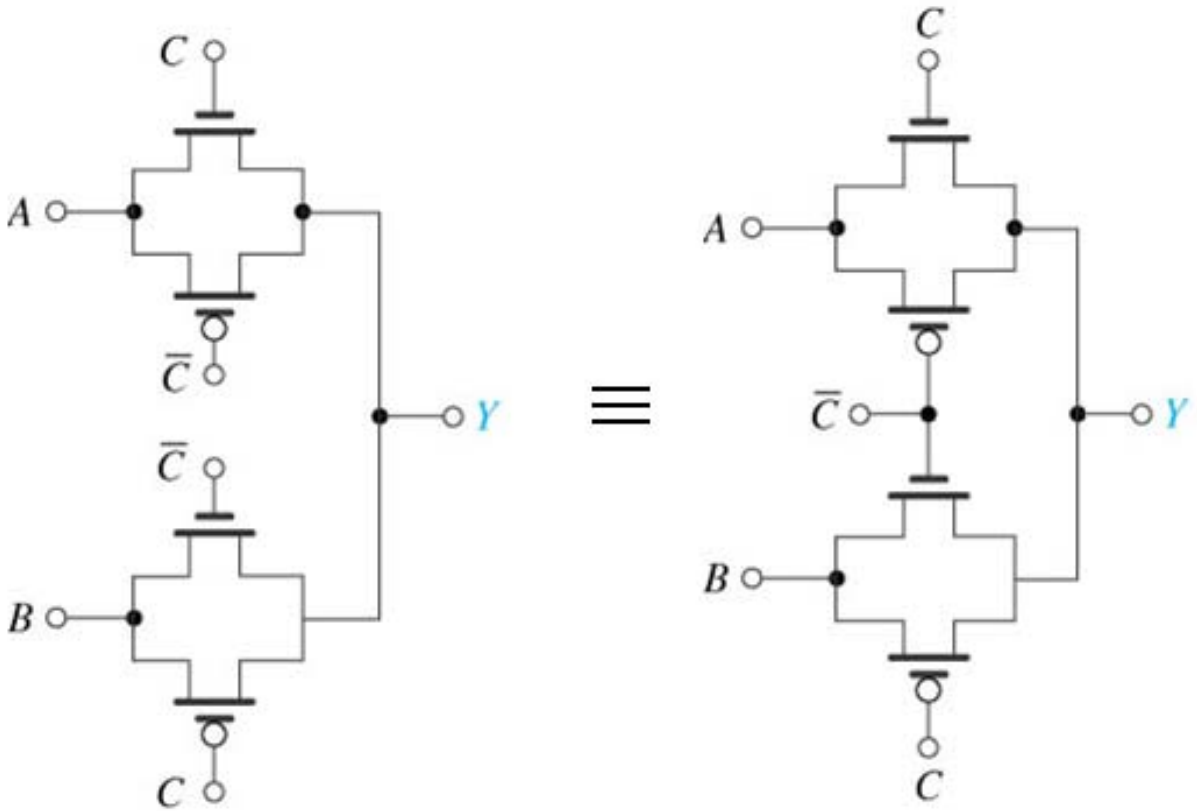
Pros:

-Improved t_p because two transistors conduct giving higher current.
-Good V_{OH}.

Cons:

-Increased capacitance *C* because of two transistors.
- More complex circuit.
- More area.

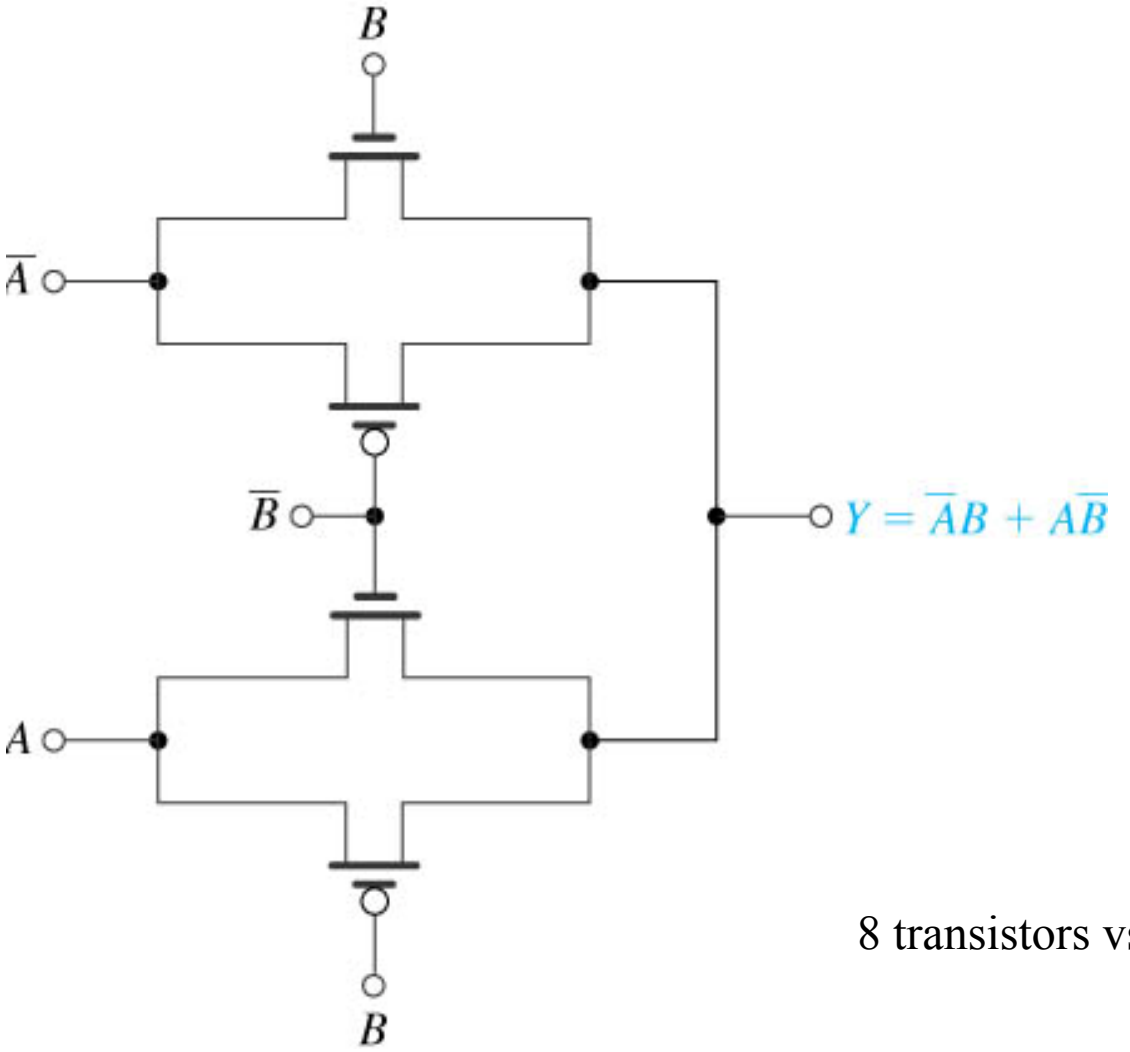
PTL Example 1



$$Y = CA + \overline{C}B$$

2 to 1 MUX

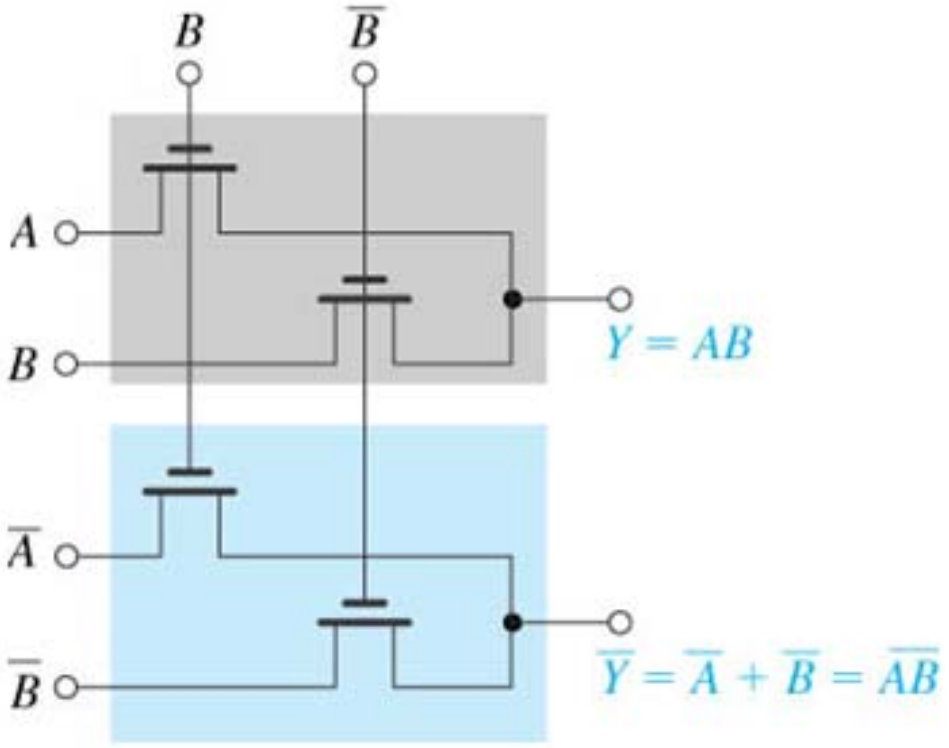
PTL Example 2



XOR

8 transistors vs. 12 for CMOS.

Complementary PTL Example



AND

NAND

Use small V_t or V_t =0V.

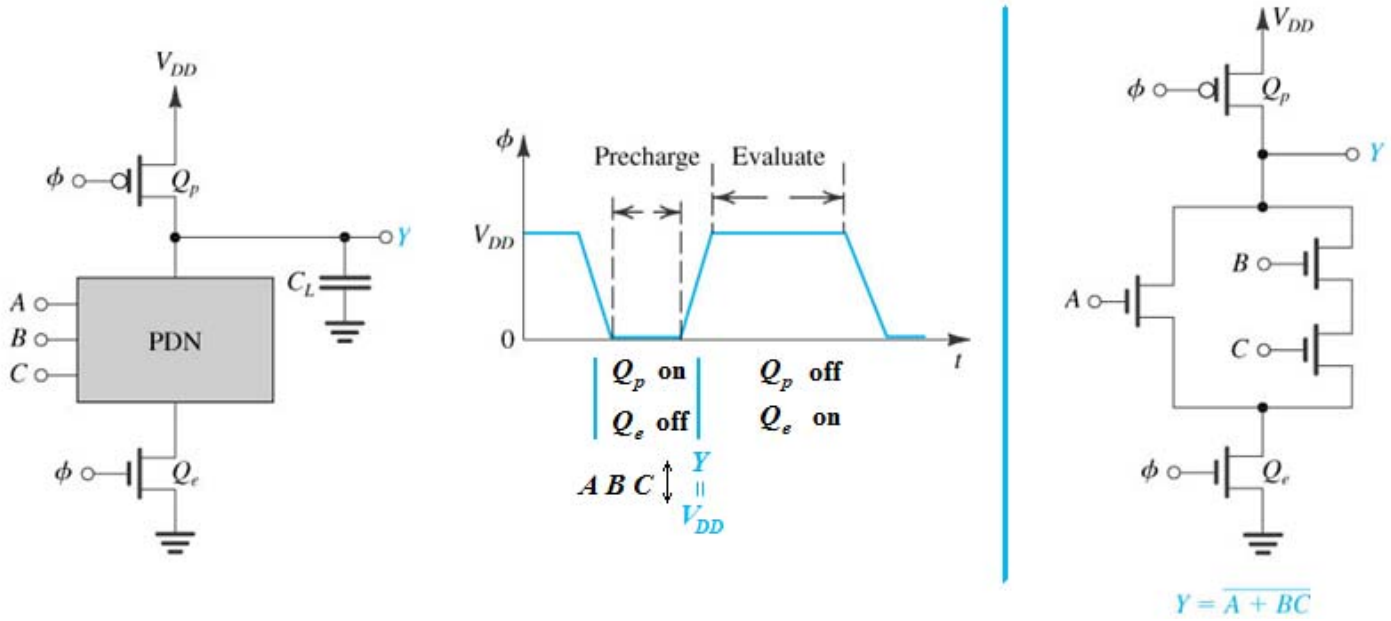
Dynamic Logic Circuits

Basic principle: Storage of voltages on capacitors.
Capacitors lose charge over time. Need refresh (clock).

Why dynamic logic?

1- Small number of transistors.
2- Static power dissipation is zero.

Dynamic Logic Operation Principle



Precharge: Q_p on, Q_e off → C_L charged to V_{DD}=Y =V_{OH}.
Inputs settle.

Evaluate: Q_p off, Q_e on

- *F(A,B,C) high* → PDN off → *Y high*, t_{PLH}=0
- *F(A,B,C) low* → PDN on → *Y low*, V_{OL}=0, $t_{PHL}\neq 0$

Q_p *W/L* to fully charge C_L during $T_{Precharge}$

Dynamic Logic Characteristics 1

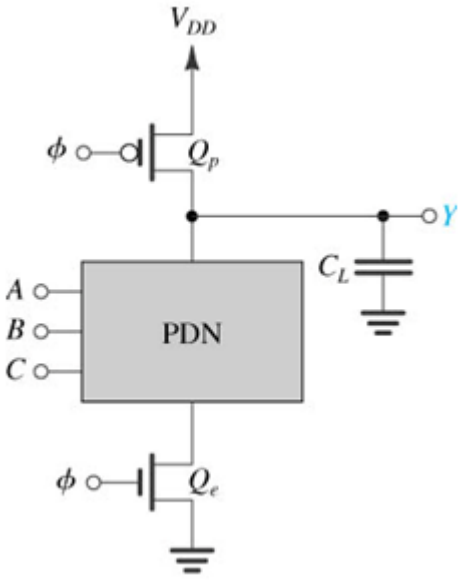
$$V_{IL} \approx V_{IH} \approx V_{tn}$$

Noise Margins: $NML = V_{tn}$ $NMH = V_{DD} - V_{tn}$

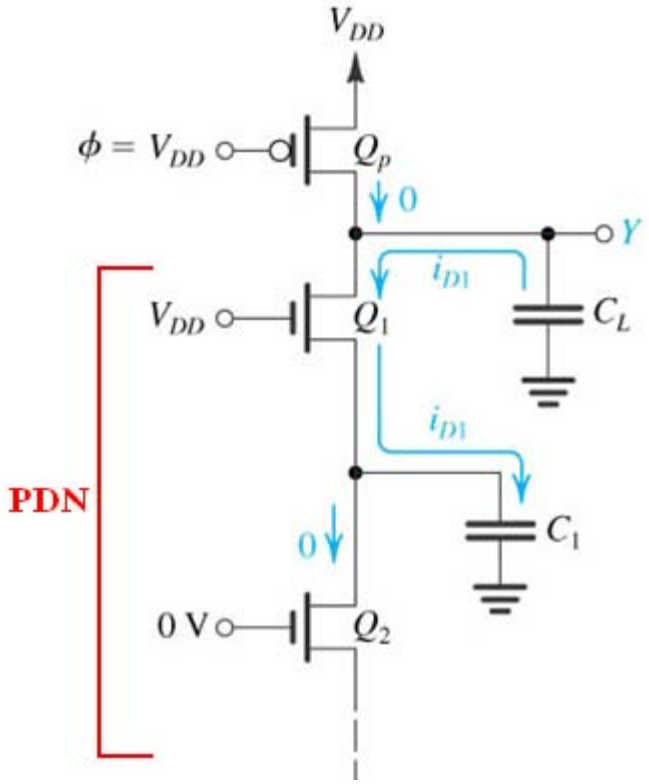
$NML \neq NMH$ NML small

C_L will discharge into the load gate.

Clock cycle must be small to limit discharge.



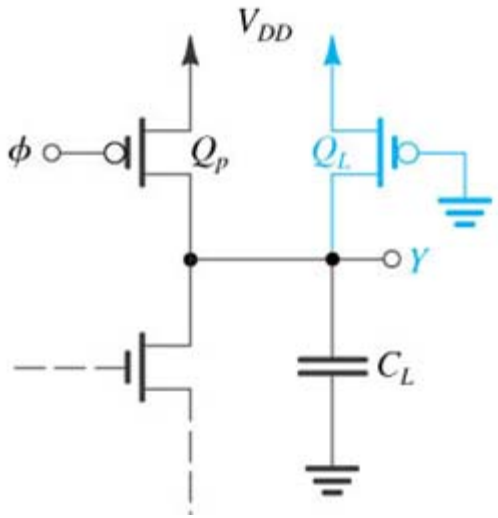
Dynamic Logic Characteristics 2



Charge Sharing

Evaluation phase

If Q_1 on and Q_2 off. C_L loses some charge to $C_1 \rightarrow v_O$ decay.



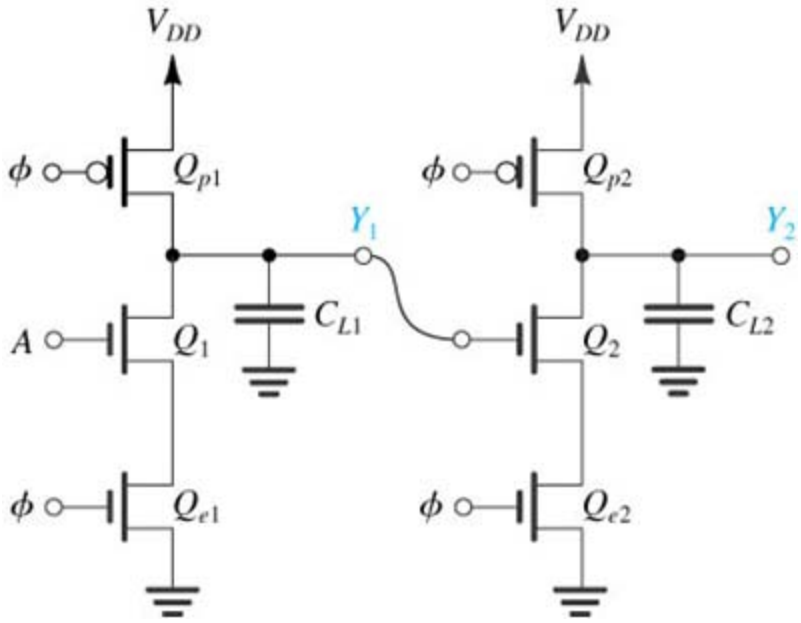
Solution

Dynamic Logic Characteristics 3

Dynamic Logic Circuits in Cascade

Evaluation phase
In theory: A high $\rightarrow$ Y_1 low $\rightarrow$ Y_2 high
In reality: Y_1 at V_{DD} and discharging
Q_2 will stay on until Y_1 drops to V_t
In the mean time Y_2 is discharging!
$v_O < V_{DD}$ (Poor One)

It doesn't work properly!



Domino CMOS Logic Circuits

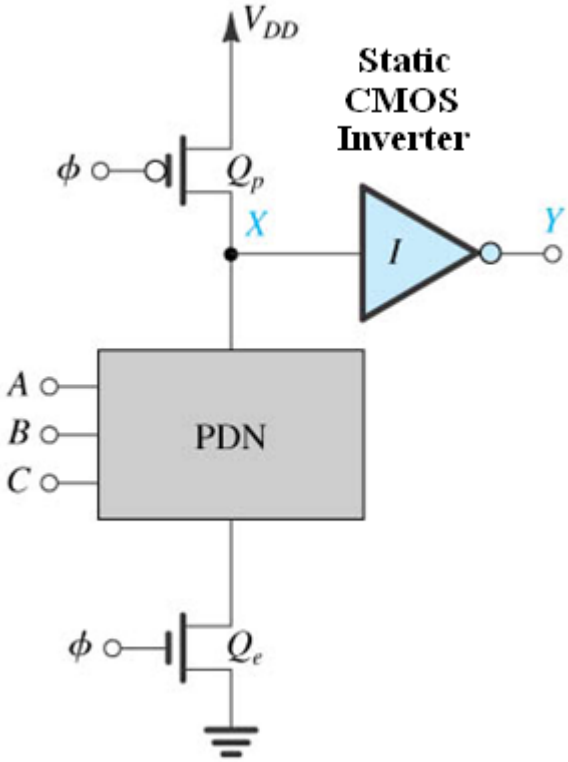
(Dynamic Logic Circuits In Cascade)

Precharge Phase: Y low

Evaluation Phase:

- X *high* $\rightarrow$ Y *low*, $t_{PHL}=0$
- X *low* $\rightarrow$ Y *high*, $t_{PLH}\neq 0$

Will it work?



Domino CMOS Logic Circuits 2

Precharge Phase:

X_1 high(V_{DD}) $\rightarrow$ Y_1 low(0V)
X_2 high(V_{DD}) $\rightarrow$ Y_2 low(0V)

Evaluation Phase:

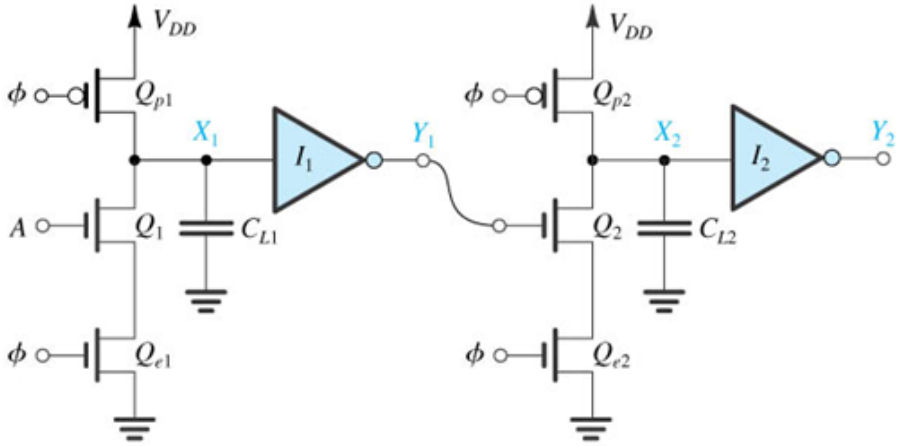
A high, $\phi \uparrow$

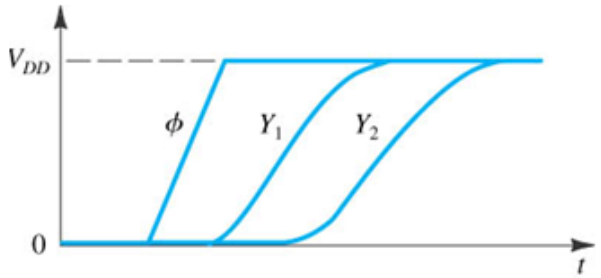
C_{L1} discharges pulling X_1 down

Wait until $v_{X1} \leq V_t$ then Y_1 high(V_{DD})

C_{L2} discharges pulling X_2 down

Wait until $v_{X2} \leq V_t$ then Y_2 high(V_{DD})





Delay

Small size + high speed + zero static power dissipation
Difficult in design