

# Expanding the Synopsys PrimeTime® Solution with Power Analysis

Gordon Yip, Product Marketing Manager, Synopsys, Inc.  
June 2006

## Introduction

Design closure in today's advanced designs requires a delicate balance of many complex issues. Timing remains critical, but power has become important toward achieving design success. Today, power management is a mainstream design challenge and a key concern for chip designers. Power consumption is a critical design delimiter. It affects packaging decisions, cooling requirements, battery life, design performance, and chip reliability. More than ever, accurate power analysis is required for designs. Designers today must consider the impact of their design techniques on power in conjunction with timing and area. A failure to analyze power can lead to chip failure.

Power, timing, and signal integrity (SI) effects are all interdependent at 90-nanometers (nm) and below. To achieve the highest accuracy power analysis, an accurate timing engine is required to perform accurate timing and slew calculations. Since timing parameters affect power dissipation, designers require a solution that takes advantage of these interdependencies. In this white paper, we propose a methodology that combines static timing analysis, signal integrity analysis, and power analysis within a single, unified environment.

## Components of Power Dissipation

For CMOS designs, the total power consumed by a circuit falls into 2 major categories: static power, which is the power consumed when the transistors are not switching, and dynamic power, which represents the power consumed by switching logic states.

### Static Power

Static power is dissipated in several ways. Some are due to the reverse-biased diode leakage from the diffusion layers and the substrate, but the largest percentage of static power results from source-to-drain sub-threshold leakage current. This is caused by reduced threshold voltages which prevent the gate from completely turning off and hence allow this leakage current ( $I_{leak}$ ).

The leakage power is dependent on the voltage, temperature and state of the transistors.

$$\text{Leakage Power} = V * I_{leak}$$

### Dynamic Power

Dynamic power is dissipated any time the voltage on a net changes due to some stimulus. This voltage change charges or discharges the capacitive load of the external net. Also, the voltage change results in a short-circuit current between the N and P transistors internal to the gate. For ASIC designs, the dynamic power consumed by the charging or discharging of the output load external to the cell is classified as switching power, while the dynamic power dissipated within the cell is generally classified as the internal power.

### Switching Power

The switching power is determined by the capacitive load and the frequency of the logic transitions on a cell output.

$$\text{Switching Power} = \frac{1}{2} * C_{load} * V^2 * f$$

where the total load capacitance ( $C_{load}$ ) is the sum of the net and gate capacitances on the driving output, and the frequency ( $f$ ) is the rate of state transitions.

### Internal Power

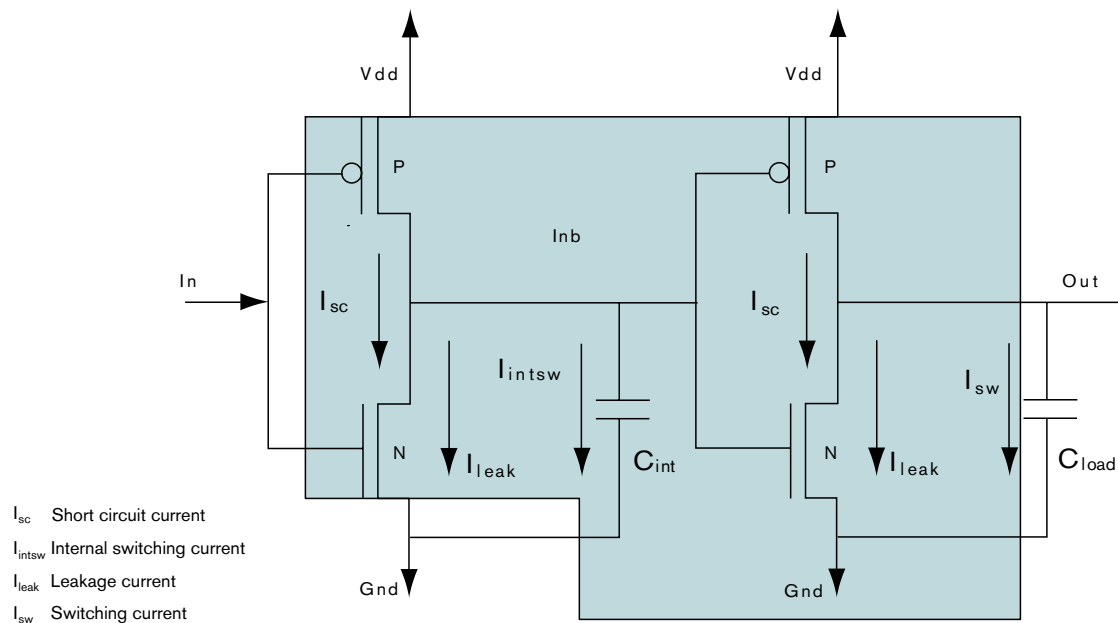
The internal power is caused by the charging of internal loads as well as by the short-circuit current between the N and P transistors of a gate when both are on.

$$\text{Internal Power} = (\frac{1}{2} * C_{int} * V^2 * f) + (V * I_{sc})$$

As the input signals transition, both N and P type transistors can be on simultaneously. During this time, current  $I_{sc}$  flows from Vdd to Gnd causing the dissipation of short-circuit power. The short-circuit power is affected by the dimensions of the transistors, the load capacitance on the output, and the transition time of the input signals. Circuits with slow transition times can dissipate excessive short circuit power as both N and P transistors are on for an extended period.

ASIC or Library vendors provide power models for the internal power consumption of CMOS cells, which are characterized with different driver output loads and input signal transition times.

The diagram below describes the power components for a simple buffer cell.



**Figure 1: Components of Power Dissipation.**

The leakage current  $I_{leak}$  can vary based on the transistor states. For example, when the input signal  $In$  is high, and the N transistor is on, the leakage will differ compared to when the N transistor is off. When a rising signal is applied at the input, internal power is dissipated due to  $I_{sc}$  and  $I_{intsw}$ . During the transition from low to high, the N transistor turns on and the P type transistor turns off resulting in  $I_{sc}$  from Vdd to Gnd. Additionally, internal switching power is incurred in charging and discharging of  $C_{int}$ . The switching power on the Out net is due to  $I_{sw}$  charging and discharging  $C_{load}$ .

## Power Analysis Requirements

In order to analyze the power consumption of a design, it is important to consider all the factors which contribute to both the static and dynamic power. These are shown in the diagram below:

In order to analyze the power consumption, the following are required:

- **Netlist Data**

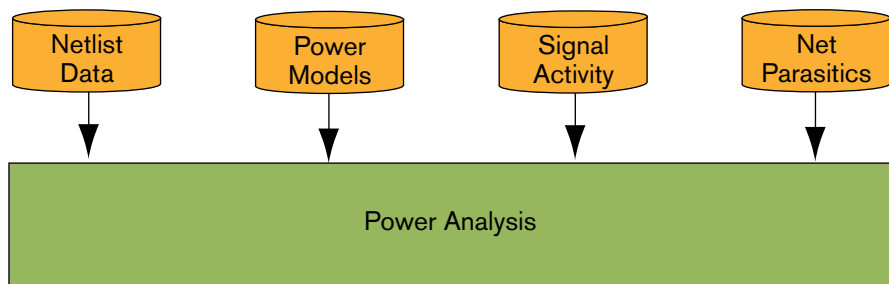
The design netlist is required to determine the design connectivity and type of cells used in the design and to accurately compute the capacitance on the drivers.

- **Cell Library Power Models**

In order to compute the internal power of the CMOS cells used in the design, ASIC or Library vendors must provide cell models which specify both the static and dynamic power consumption internal to the cell.

- **Signal Activity**

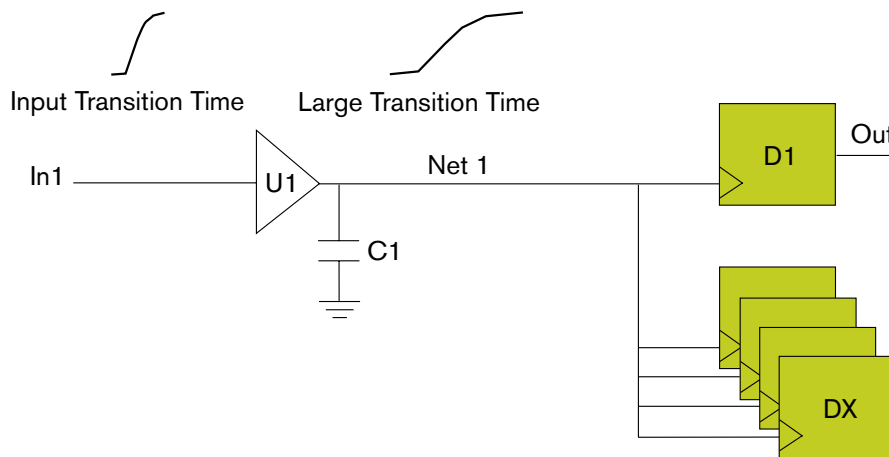
The signal activity of a design affects both the static and dynamic power consumption. The static power (cell leakage) is often state dependent, and the dynamic power is directly proportional to the toggle rate of the pins.



**Figure 2: Power Analysis Requirements.**

- **Net Parasitics / Transition Times**

Net parasitics (or capacitances) affect the dynamic power of the design. Switching power is directly proportional to the net capacitance. Internal power depends on both the input signal transition times, which are determined by the net parasitics, as well as the output load, which is a combination of the net parasitics and input pin capacitances of the fanout. The example below illustrates the relationship between the transition times and the dynamic power consumption.



**Figure 3: Transition Times Affect Dynamic Power Consumption.**

The internal power consumption of *U1* is determined by the transition time on *In1* and the capacitive load on the output *Net1*, which is the sum of the input pin capacitances of the gates it drives (gate fanout) and the net capacitance, *C1*. Now if the net capacitance *C1* is large, the switching power of *Net1* certainly will increase, but additionally, the transition time on *Net1* will be affected.

A large transition time on a net with a large number of fanout loads results in excessive internal power consumption for all of the gates to which it is connected. This is because the internal power consumption of the fanout gates, the registers *D1-DX* in this example, is considerable because the long transition time on the net is allowing for a longer period of time in which short circuit power is being dissipated.

In summary, the accuracy of the power analysis is dependent upon the accuracy of the inputs provided. The netlist, cell library power model, signal activity, and parasitics/transition times need to be accurate to provide accurate power consumption analysis.

## **PrimeTime® PX Power Analysis**

### **Integrating Timing, Signal Integrity (SI) and Power Analysis**

Synopsys PrimeTime PX, the power analysis extension to PrimeTime, enables users to perform full-chip, concurrent timing, signal integrity, and power analysis in a single, easy-to-use environment. PrimeTime PX can perform highly accurate power analysis because it can take advantage of the timing and signal integrity engines of the PrimeTime and PrimeTime SI solutions for processing the design data, parasitic backannotation, and calculation of transition times and timing windows. Also, the power analysis engine supports composite current source (CCS) power models, which accurately model the CMOS cell library. Furthermore, it also supports multiple signal activity formats. Altogether, PrimeTime PX provides the best platform to accurately use and analyze all of the key inputs required for accurate power analysis. The PrimeTime PX solution is described below.

### **Netlist Data**

Clearly the design netlist data provided for analysis must accurately represent the design. Within the PrimeTime PX solution, a variety of netlist formats are supported. For both power and timing analysis, the same netlist reader is able to process netlist and store the analysis results, thereby enabling concurrent analysis on the same design netlist data.

### **Parasitics/Timing**

In the PrimeTime solution, parasitics (resistance and capacitance) for the nets in the design can be annotated onto the design netlist. These parasitics can either be reduced parasitics (lumped RC or reduced pi model) or detailed parasitics (distributed RC). By annotating parasitics, especially detailed parasitics, very accurate delay and transition times can be calculated. These accurate delays and transition times are then used for more accurate dynamic power calculations.

Furthermore, the effect of cross-coupling capacitances on delays and slews can also be accounted for by annotating cross-coupled parasitics and using the signal integrity analysis engine in the PrimeTime SI solution. If the PrimeTime SI solution is not enabled, then any cross-coupling is split to ground, and the cross-coupling effect will not be accurately computed.

The PrimeTime solution's integrated static timing analysis and RC delay calculation engine accurately calculates the delay and transition time for every cell, based on the input slew on the driving cell, the annotated RC network, and the capacitive load on the fanout pins.

### **CCS Cell Library Models**

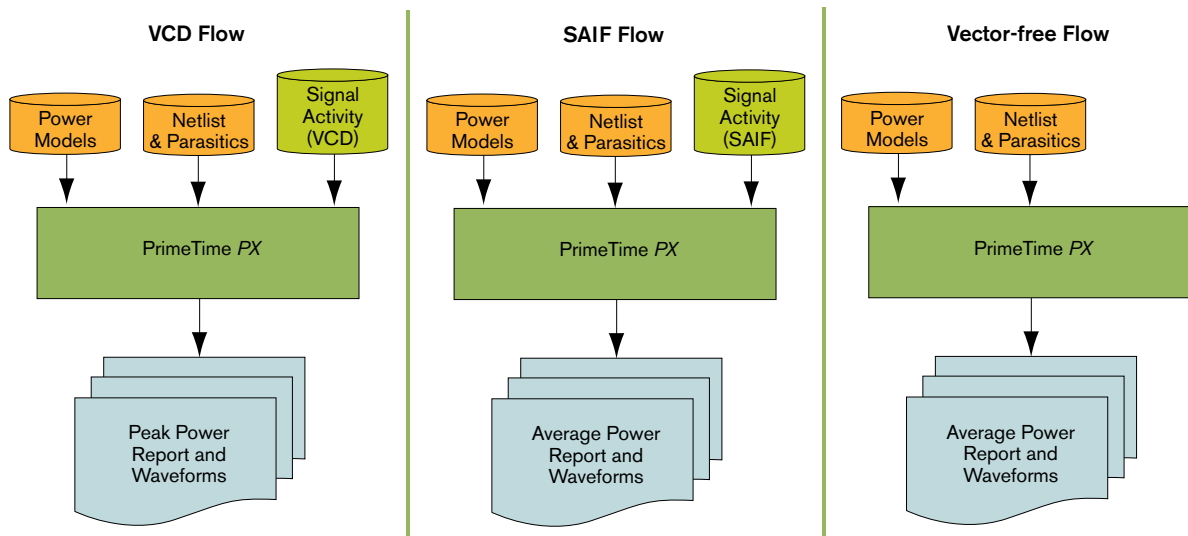
With the advent of smaller nanometer technologies, the CCS approach of modeling cell behavior has been developed to address the effects of very deep nanometer processes. With the use of the CCS cell library models, delay calculation accuracy and dynamic power analysis accuracy is further improved.

For example, the CCS timing receiver model uses 2 capacitance values rather than a single lumped capacitance for the input gate capacitance, or load, of a cell. As the input waveform switches, the first capacitance value is used for the gate load up to the delay threshold. When the input waveform reaches this threshold, the load is dynamically adjusted to the second capacitance value. The result is this timing receiver model provides a more accurate model of the loading effects in the presence of the Miller effect.

The CCS modeling format supports both timing and power, thereby providing a high degree of accuracy.

### **Signal Activity**

Accurate power analysis depends on accurate signal activity. PrimeTime PX power analysis supports both average and peak power analysis based on the signal activity provided. For average power analysis, PrimeTime PX supports the propagation of switching activity based on either tool defaults, user-defined switching activity, or switching activity derived from a logic simulation (either RTL or gate-level), typically saved as a SAIF (Switching Activity Interchange Format) file. For peak power analysis, PrimeTime PX requires a timing logic simulation and generation of a VCD that captures the activity and time of every event on each net.



**Figure 4: Power Analysis Flows.**

The VCD-based analysis is extremely accurate since all the factors contributing to power consumption are supported in an accurate form. Peak and average power can be calculated, and detailed, time-based waveforms can be generated.

If event-based simulation activity is not available, accurate average power can still be calculated by providing gate-level toggle rates, typically with a SAIF file. In the SAIF file, the activity information includes the number of times the signals toggled per net, as well as the percentage of time that the signals were at a given state. This toggle rate information enables both dynamic and leakage power to be accurately determined.

If gate-level logic simulation data is unavailable, the PrimeTime PX solution also supports RTL VCD (generated from a RTL logic simulation), RTL SAIF (also generated from a RTL simulation), user-defined switching, and default analysis. In this case, the activity of unannotated nodes is obtained via an internal zero-delay simulation to compute the toggling of the outputs. With the switching activity for every node in the design now determined, power consumption can be calculated.

### Other Benefits of Integrating Timing, SI, and Power Analysis

By combining timing, signal integrity and power analysis into a single tool and environment, productivity and time to results are improved over separate, standalone timing and power analysis tools. With a single environment, identical operations are not repeated. For example, timing and slew calculations are not repeated. Netlist, parasitic and constraint file reads are not repeated. And tool setup steps are not repeated. As a result, PrimeTime PX delivers up to 2X faster time to results over separate, standalone solutions.

Furthermore, as an extension of the PrimeTime environment, PrimeTime PX is easy to use and adopt. Power analysis can be performed using the familiar PrimeTime commands, user interface, reports, attributes, and multiple debugging features.

## Summary

With the transition to finer process geometries, signal integrity effects and power consumption have become a top concern. When ignored, circuits can either fail in silicon, or not meet performance specifications. Given the effects of parasitics and SI on timing, and the effects of timing on power consumption, designers need an environment in which the interdependencies between power and timing analysis are accounted for.

Use of the PrimeTime environment for processing of the netlist, parasitic and timing data contributes to a high level of accuracy when performing power analysis. The other critical factor is signal activity. If event-based activity is available, both peak and average power can be determined. For purely average power analysis, the toggle rate data can produce accurate leakage and average power results. If gate-level simulation activity data is unavailable, the support for RTL level switching or default switching activity propagation provides a good estimate of the dynamic power and state-dependent leakage.

**SYNOPSYS®**