Project 4
ELET 3132
Digital Systems
State Machine Design

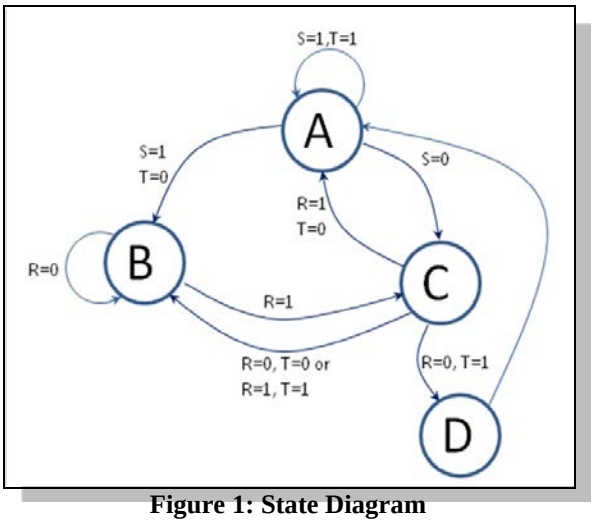

Figure 1: State Diagram

You are provided the state diagram shown in figure 1. Develop a Finite State Machine to implement the state diagram. This is an individual project. You may get some help from others, but all the work must be your own. Using this diagram:

1. Develop a state table
    a. R, S, and T are inputs to the system
    b. The outputs of the system are the outputs of the flip-flops
2. Use One-Hot encoding for encoding the states
3. Use negative-edge-triggered D flip-flops to implement the design
    a. You must include the Karaugh Maps and State Equations
4. Develop and test the circuit
    a. Use Xilinx Schematic Capture to input the circuit developed by you (not the one generated by Xilinx)
    b. Use a test bench to verify operation of the circuit
    c. Include the output from ISim in your report
5. Write the VHDL code to implement this circuit
    a. Use the test bench developed in 4b as a model to create a new test bench to verify the operation of the VHDL code
    b. Compare the results of the schematic and the VHDL code
    c. If something does not match, troubleshoot your design or VHDL code (whichever is incorrect) until both agree
6. Write a report
    a. Show the complete VHDL program(s)
    b. Comment the VHDL code where appropriate
    c. Show the schematic design that was developed by you
    d. Show all test benches and show all ISim results