```
//`timescale 10ns/1ps;


module difequ (in,out,InitialOut,k,clk,reset);
  output [17:0] out;
  input signed [17:0] in,InitialOut;
  input clk,reset;
  input [3:0] k;

  wire  signed [17:0] dx1;
  wire signed [17:0] dx2;
  reg signed [17:0] out;

  integrator int1(dx1,in,InitialOut,k,clk,reset);
  integrator int2(dx2,-dx1,InitialOut,k,clk,reset);

  always @(posedge clk)
    out = dx2;

endmodule
```