```
`timescale 10ns/1ps;

module integrator(out,funct,InitialOut,dt,clk,reset);
  output [17:0] out;
  input signed [17:0] funct;
  input [3:0] dt;
  input clk,reset;

  input signed [17:0] InitialOut;
  wire signed [17:0] InitialOut;

  reg signed [17:0] v1new;

  reg signed [17:0] v1;
  reg [4:0] count;

 initial
 begin
   v1 = 0;
   count = 0;
 end

  always @ (posedge clk)
    begin
      begin
        count <= count + 1;
        if (reset==0)
          begin

          v1 = InitialOut;
          v1new = InitialOut;
          count = 0;

        end

        else if(count == 0)
          v1 = v1new;
       end
          v1new = v1+(funct>>>dt);

    end


  assign out = v1;

endmodule
```