LAB PRO-51

8051 BASED
SINGLE BOARD COMPUTER

USER'S MANUAL

9/1/01

Allen Systems
2346 Brandon Road
Columbus, OH 43221
www.allen-systems.com
614-488-7122

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I. Introduction

A. General Features

The LAB PRO-51 is a single board computer based upon the popular 8051 family of microcontrollers. The particular device installed on the board is the P89C51RB2BA. It is a fully static CPU with optimized internal timing of 6 clocks per machine cycle. The processor can run at up to 20 MHz. Optionally, the processor can be configured for 12 clocks per machine cycle. In this mode, the processor runs at up to 33 MHz.

Like other microcontrollers in its family, the 89C51 uses Flash for on-chip program storage. A major advantage of the 89C51, however, is its mechanism for in-system programming. Its Flash can be programmed by downloading user code over the on-chip serial port. This approach is referred to as "in-system" since the 89C51 remains installed on the LAB PRO-51 during programming.

Typically, a host PC is used to perform the in-system programming. The PC is linked to the LAB PRO-51 by connecting the DB-09 connector on the board to a serial COM port on the PC. Programming software on the PC provides all necessary programming operations. Hence, no special programmer is required.

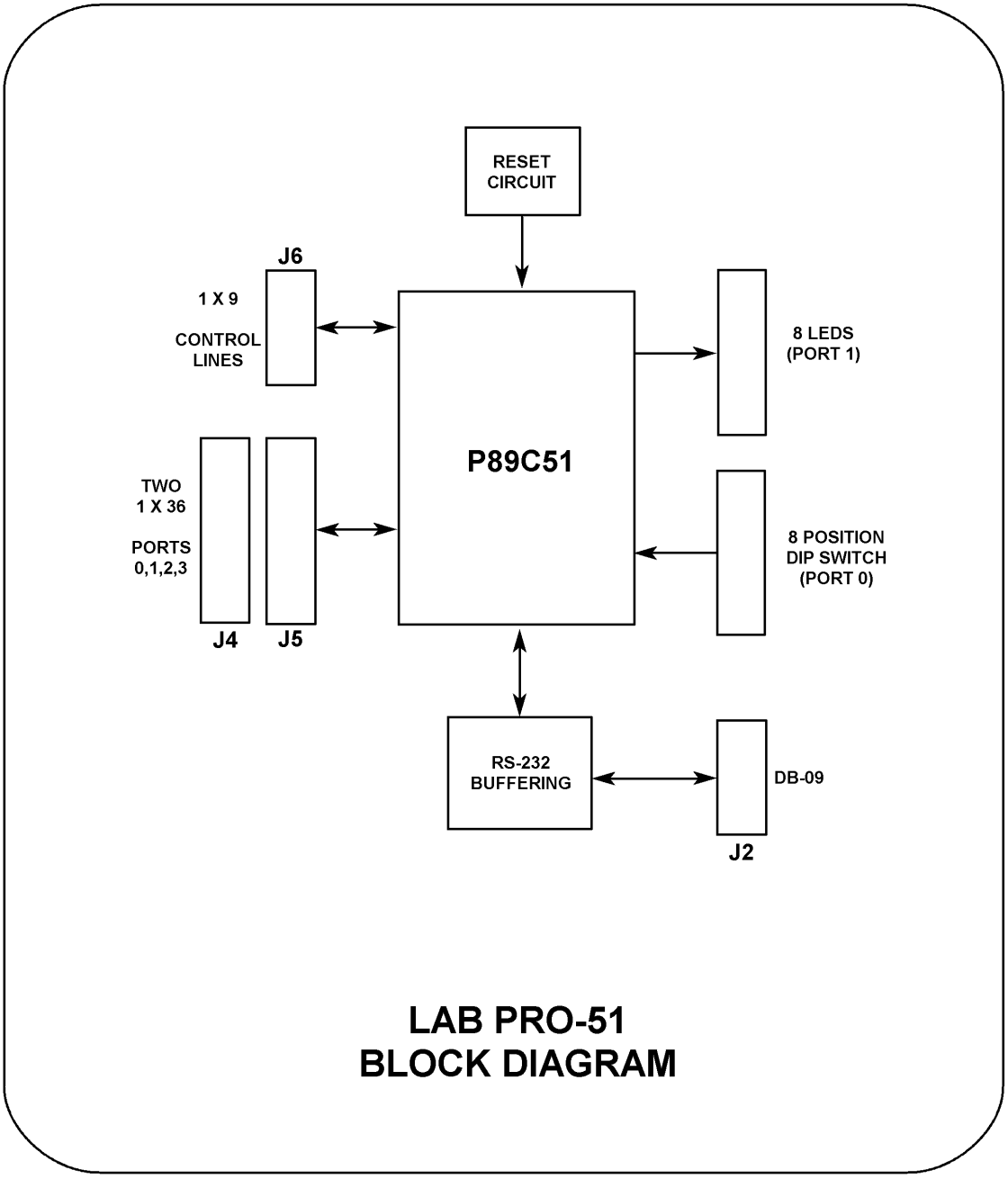
A major design feature of the LAB PRO-51 is its prototyping area. The prototype area contains a large number of solder pads (.060 pad with .036 hole) placed on a .1 inch grid. User circuitry can be built and tested in this area. Board connectors are used to wire 89C51 lines to circuitry in the prototype space.

An optional solderless breadboard can also be purchased and mounted over the prototyping area. This enables the user to quickly build custom circuitry using jumper wires. No soldering is required. In addition, all CPU lines are available at female header connectors. Thus, jumper wires can also be used to make connections from the breadboard to the processor.

The board measures 4.75 by 6.75 inches. Board features include prototyping space or optional solderless breadboard, female header connectors and solder pads for connections to the processor, 8 LEDs, 8-position DIP switch, RS-232 serial port with DB-09 female connector, DS1233 EconoReset device, and 1 amp voltage regulator. The DS1233 generates a reset signal on power–up.

All in all, the LAB PRO-51 is great for building and testing designs which are based on the P89C51 processor.

B. Block Diagram



II. Installation

A. Introduction

This manual uses the following notation when discussing board signals. Signals which are low level true are preceded by a "-". For example, -PSEN, and -EA. This notation is also used on the LAB PRO-51 schematic. The "-" can be considered equivalent to a bar occurring over the signal name in other documentation.

Whenever a reference is made to connectors or jumpers on the board, a diagram will appear in this manual to clarify the discussion. These diagrams correspond to physical connectors or jumpers on the board and will be drawn as they appear when the LAB PRO-51 is oriented right side up, with the board's J1 and J2 connectors positioned along the board's top edge. In this position, J1 is to the left, and J2 is on the right.

The LAB PRO-51 user is urged to exercise extra caution when installing and operating the board. Precautions against electrostatic discharge should be taken. Also, a double check of all connections should be performed before applying power. This is especially important in view of the fact that most I.C.'s on the board are CMOS. The user must be sure to use ground shields and grounded wrist straps to avoid damaging the board's devices.

WARNING!!!

Take precautions against electrostatic discharge whenever working with the board. This includes placing the board and any associated circuitry on an electrostatically protected working surface. Any personnel handling the board or circuitry should wear a properly grounded wrist strap.

WARNING!!!

Double check all connections made to the board before applying power. This pertains to power connections made over connectors J1 and J3, as well as any connections made to J2, J4, J5, or J6.

B. Power Connections

There are two power-related connectors on the LAB PRO-51: J1 and J3. Connector J1 supplies the board's power, and is connected to an AC adapter. Connector J3 is a +5 Volt power source and is used to power circuitry on the prototyping area or solderless breadboard.

WARNING!!!

The board's only source of power is an AC adapter which connects at J1. Do not attempt to connect a power supply or any other power source at J3. J3 is to be used only for supplying +5 Volts to user circuitry residing on the prototyping or breadboard area.

1.) Connector J1

The LAB PRO-51's power source is a 1 amp AC adapter which connects at J1. The plug on the AC adapter is configured so that the tip is positive, and the outer cylinder is ground. The AC adapter plug goes into the jack at connector J1. It is located along the top edge near the upper left-hand corner.

WARNING!!!

It is imperative that only an AC adapter with the proper specifications be used. The user must insure that any AC adapter used with the LAB PRO-51 adheres to the following specifications:

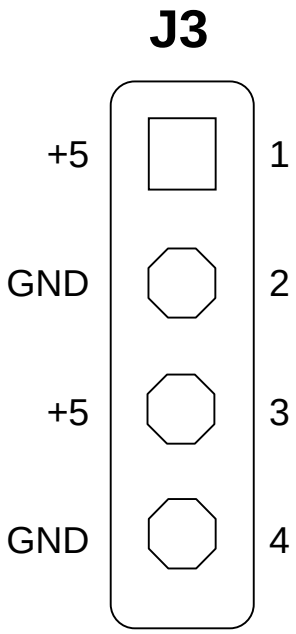
- +9 Volts DC, unregulated
- Rated at 1 amp
- 2.1 mm female plug
- Tip (or center) of plug is positive (+9 Volts DC)
- Outside of plug is negative (GND)

2.) Connector J3

Connector J3 is used to power the user circuitry residing on the prototype or breadboard area. It is a 4-position, terminal block type of connector with screws for attaching wires. The connector has two positions for GND, and two positions for +5 Volts.

Note the following if the optional solderless breadboard is used. Connections to the breadboard should only be made with solid, 22 gauge wire. Also, there are two distribution strips on the breadboard. One runs along the top edge, while the other runs along the bottom edge. Each distribution strip has two rows of holes. The holes of each row are connected. Hence, these rows are useful for connecting to +5 Volts and GND.

The pin out of connector J3 is as follows:



WARNING!!!

J1 is a connection point for power flowing into the LAB PRO-51.
It supplies power to the board by connecting to the AC Adapter

J3 is a connection point for power flowing out of the LAB PRO-51.
It supplies power from the board to user circuitry in the prototyping area or solderless breadboard.

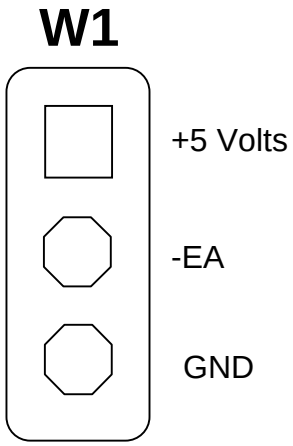
It is important to note that J3 is a power supply output. That is, it provides a power source for user circuitry. J3 must not be connected to a power supply. The board is powered by an AC Adapter which connects at J1. Connector J1 is located along the top edge near the upper left-hand corner.

C. Jumpers

One jumper is available on the LAB PRO-51 at position W1. It selects either +5 Volts or GND as the source for the –EA input on the processor. The default setting for W1 has –EA tied to +5 Volts, thereby enabling the on-chip flash. There is a board trace on the solder side which connects the top two pins of the connector.

This jumper setting can be changed as follows. Carefully cut the trace connecting the top two pins. This trace is located on the board's solder side. Then install a jumper to connect the bottom two pins of W1. This connects –EA to ground, and disables the on-chip Flash. As a result, external program memory must be provided by the user.

Details on W1 are given below:



D. Connectors

1.) Introduction

There are six connectors available for board installation. Because of the critical nature of power connectors J1 (power in to board) and J3 (power out from board), they were covered previously. Once again, refer to Part II., Section B. and exercise extreme caution when making the power connections.

The following table identifies the connectors on the board. A detailed explanation of each is given following the table.

Connector	Description
J1	Board Power Connector, +9V DC Unregulated (Power in)
J2	RS-232 Buffered Serial Port Lines
J3	User Circuitry Power Connector, +5V DC Regulated (Power out)
J4	Ports 0, 1, 2, and 3 of processor, female header connector
J5	Ports 0, 1, 2, and 3 of processor, pads for soldering
J6	Processor control lines, female header connector

2.) Connector J1

J1 is used to supply power to the PRO LAB-51 from an AC adapter. Because of its critical nature, it was covered previously in Part II., Section B.

3.) Connector J2

Connector J2 brings out the RS-232 buffered serial port of the 89C51. J2 is a DB-09 connector and is configured at DCE (data communication equipment). It can be connected to the COM serial port on a PC. Note that pins 1, 4, 6, and 8 on J2 are tied together, so no RTS/CTS handshaking is used.

The pin out of connector J2 is shown below. Pin 1 of J2 is identified on the board's silkscreen. The connector has 9 holes for mating with the cable. On the connector, each hole is labeled with its corresponding pin number. Note that N.C. = no connection.

Connector J2 – RS-232 Buffered Serial Port

Pin Number	Connector J2 Line	Associated CPU Line
1	DCD	None
2	RS-232 TXD (Out)	P3.1/TXD
3	RS-232 RXD (In)	P3.0/RXD
4	DTR	None
5	GND	GND
6	DSR	None
7	RTS	None
8	CTS	None
9	N.C.	None

4.) Connector J3

Connector J3 supplies power to user circuitry on the prototype or breadboard area. Because of its critical nature, it was covered previously in Part II., Section B

5.) Connector J4

Connector J4 is a female header connector in a 1 by 36 configuration. It brings out Ports 0, 1, 2, and 3 of the 89C51. Jumper wires can be used to connect J4 to user circuitry on the solderless breadboard.

Note that connections should only be made to J4 using solid, 22-gauge wire. This type of wire is also recommended for making connections on the breadboard.

The pin out of connector J4 is shown below. Pin 1 of J4 is identified on the board's silkscreen at the left-most pin. Pin numbers proceed in sequence from left to right along the connector. Note that N.C. = no connection.

Connector J4 – Ports 0, 1, 2, and 3 of the 89C51

J4 Pin Number	89C51 Line	89C51 Pin Number
1	P3.7	19
2	P3.6	18
3	P3.5	17
4	P3.4	16
5	P3.3	15
6	P3.2	14
7	P3.1	13
8	P3.0	11
9	N.C.	None
10	P2.7	31
11	P2.6	30
12	P2.5	29
13	P2.4	28
14	P2.3	27
15	P2.2	26
16	P2.1	25
17	P2.0	24
18	N.C.	None
19	P0.7	36
20	P0.6	37
21	P0.5	38
22	P0.4	39
23	P0.3	40
24	P0.2	41
25	P0.1	42
26	P0.0	43
27	N.C.	None
28	P1.7	9
29	P1.6	8
30	P1.5	7
31	P1.4	6
32	P1.3	5
33	P1.2	4
34	P1.1	3
35	P1.0	2
36	N.C.	None

6.) Connector J5

Connector J5 brings out Ports 0, 1, 2, and 3 of the 89C51. It has the same pin out as connector J6. However, J6 has solder pads for connecting the port lines to user circuitry. This is convenient if the prototyping area is used, rather than a solderless breadboard.

The pin out of connector J5 is identical to that of connector J4. Please see details on connector J4 in the preceding section.

7.) Connector J6

Connector J6 is a female header connector in a 1 by 9 configuration. It brings out control lines of the 89C51. Jumper wires can be used to connect J6 to user circuitry on the solderless breadboard.

The pin out of connector J4 is shown below. Pin 1 of J4 is the left-most pin. Pin numbers proceed in sequence from left to right along the connector. Note that N.C. = no connection.

Connector J6 – Control Lines of the 89C51

J6 Pin Number	89C51 Line	89C51 Pin Number
1	ALE	33
2	ALE	33
3	-PSEN	32
4	-PSEN	32
5	RST	10
6	RST	10
7	-RST	None
8	-RST	None
9	GND	22

III. 89C51 Programming

A. Introduction

The 89C51 has 16K bytes of Flash program memory It supports parallel programming in a manner similar to other 8051s with on-chip EPROM or Flash. An important improvement in the 89C51, however, is its ability to be serially programmed via the on-chip UART. This greatly facilitates Flash programming since the chip remains installed in the board. It is referred to as in-system programming.

Connector J2 brings out the RS-232 buffered serial port. It allows the LAB PRO-51 to be serially linked to a host PC. Programming software on the PC provides all of the necessary programming operations. This eliminates the need for special programming equipment.

B. Conventional (Parallel) Programming

If desired, conventional programming methods can be used with the 89C51. All I.C.'s on the LAB PRO-51 are in sockets, including the 89C51. Hence, it may be removed from the board and programmed using standard programming equipment. Note that a programmer specifically supporting the P89C51RB2BA must be used.

C. In-System (Serial) Programming

In-system programming is supported on the LAB PRO-51. It is performed by serially linking the board to a host PC. Windows 98-based software on the PC performs the various programming operations. The program is called WinISP and can be downloaded from the Philips Web Site.

The following items are needed to carry out serial programming:

Items Required for In-System Programming

1.) LAB PRO-51 with 89C51 installed
2.) DB-09 Serial cable
3.) PC with Windows 98 Operating System and serial port.
4.) WinISP.exe In-System Programming Software

The WinISP.exe program can be downloaded from Philips Web Site. Their home page is www.philips.com. The download page is located at address:

www.semiconductors.philips.com/mcu/download/80c51/flash/

A Tutorial on using the software can also be downloaded from this page. It is called wisptuto.zip .

The recommended procedure for in-system programming is given below:

In-System (Serial) Programming Procedure

1.) Make sure that both the LAB PRO-51 and Host PC are off.

2.) Use the DB-09 serial cable to connect J2 on the LABN PRO-51 to a serial port on the Host PC. The PC serial port must be COM1, COM2, or COM4.

3.) Disconnect any lines tied to P3.0 and P3.1 on the board.
These are the UART's unbuffered TXD and RXD lines. User circuitry would typically be tied to these lines at connectors J4 or J5.

4.) Set switch SW2 on the LAB PRO-51 to the PROG position (down).
This will cause the P89C51 to enter the programming mode when power is applied to the board.

5.) Recheck all connections and the setting on SW2.

6.) Turn on the host PC.

7.) Apply power to the LAB PRO-51.

8.) Run the 89C51 WinISP.exe program.

9.) Specify the following fields in the WinISP Window:
   a.) Chip: P89C51RB2
   b.) Port: Select the serial port connected to the DB-09 cable.
   c.) OSC: 11.0592 MHz

10.) If the Flash is not blank, perform an Erase operation.

11.) Load the .hex file containing the object code to be programmed into the Flash.
This file is typically generated using a cross assembler or cross compiler.

12.) Program the Flash.

13.) Refer to the MISC box in the WinISP Window. Press the Read button. If the Status byte is 0, proceed to step 14.). If not, set the Status byte to 0, and then press the Write button. The significance of this is explained below.

14.) Move SW1 on the LAB PRO-51 to the RUN position (UP). Press the reset switch at SW3 on the LAB PRO-51 to reset the board.

15.) The programmed user software should execute.

Explanation of Vector and Status Bytes

The WinISP Window has a box labeled MISC. It contains information on the Vector and Status bytes, the security bits, and has buttons for Read and Write. Pressing the Read button will read these values from the chip. Pressing the Write button will cause the displayed values to be written to the 89C51.

The values shown in the MISC box do not reflect the actual chip state until the Read button has been pressed. Perform a Read operation to obtain the current chip state.

The vector byte should be FC and the Status byte should be either FF or 0. The Status byte determines which software executes out of reset while in the run mode. If the Status byte is FF, the Boot Loader will execute. If the Status byte is 0, user code programmed into the Flash will execute.

To insure that user code executes in the Run mode, the Status byte must be programmed to 0. This can be performed by setting the Status value to 0 and then pressing the Write button.

Do not modify the security bits.

IV. DS1233 5V EconoReset

The DS1233 5V EconoReset provides processor supervisory functions on the board. This includes the generation of a reliable hardware reset during power-up, power-down, and brownout conditions.

A hardware reset occurs when the regulated +5 supply line on the board is below 4.625 (typical) Volts. When power is applied to the board, the -RST (low level true) output of the DS1233 is enabled until the board's +5 Volt supply line reaches the 4.625 Volt level. This forces the CPU into reset to avoid any erratic behavior. Once a voltage level of 4.625 Volts (or higher) is reached, the reset output stays enabled for a minimum of 250 milliseconds (ms). The reset line is then disabled, and CPU operation begins.

Should power fall below 4.625 Volts, the DS1233 will again force a reset. The reset will continue until the board's regulated supply goes above 4.625 Volts and remains there for at least 250 ms.

See the DS1233 data sheet for complete details on using the part.

Note that no watchdog timer function is available on the DS1233. However, a programmable watchdog timer is included on the 89C51. Refer to the 89C51 data sheet for information on using its watchdog timer.

V. LEDs and DIP Switch

A. Introduction

There are 8 LEDs and an 8-position DIP Switch available on the LAB PRO-51. These can be used for projects requiring simple user input and output. The LED's are controlled by Port 1, and the DIP switches are read at Port 0.

B. LEDs

The 8 LEDs are controlled by Port 1 and mapped so that the P1.7 controls the left-most LED and P1.0 controls the right-most LED. Hence, the row of LEDs directly represents the binary value in Port 1.

Out of reset, Port 1 lines are configured as high outputs. As a result, the LEDs are on after a board reset. They remain on until user software clears one or more of the Port 1 lines to a low level.

C. DIP Switch

The 8-position DIP Switch is connected to Port 0. Just as with the LEDs, the left-most switch is tied to P0.7 and the right-most switch connects to P0.0. Hence, the byte value read from Port 0 directly represents the switch settings.

Each switch is open when down. Hence, the corresponding Port 0 line is pulled high by RN2, and will read high. When a switch is in the up position, it is closed and the Port 0 line is connected to GND. In this case, the corresponding port line will read low.

D. Disabling the LEDs and DIP Switch

It may be desirable to disconnect the LED circuitry and DIP Switch in applications which use Port 0 and Port 1. If left connected, there could be interference with activity on these port lines.

To disconnect Port 1 from LED circuitry, simply remove the 74HC245 chip installed at U4. If it is reinstalled at a later time, be sure to observe the proper chip orientation.

To disconnect Port 0 from the DIP Switch, make sure that all switches are open (down). This insures that Port 0 lines are disconnected.

VI. Specifications

This section identifies the operating and environmental specifications for the LAB PRO-51. Specifications given below assume no user circuitry is connected to the board.

A. Electrical

	Operating Range			
Parameter	Min.	Typ.	Max.	Units
+5 Supply Voltage	4.75	5.0	5.25	Volts
+5 Supply Current	20	50	90	milliamps

B. Environmental

	Operating Range			Storage			
Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Ambient Temp.	0	25	55	-20	25	75	Degrees C
Humidity	5	-	95	5	-	95	%RH

VII. Operation

Typical use of the LAB PRO-51 single board computer might involve adding custom user circuitry to the prototyping area or solderless breadboard. User circuitry is tied to the processor using connectors J4, J5, and J6. J4 and J6 are female header connectors. These are typically used to connect to the solderless breadboard. Connector J5 is used to make solder connections, which is typical when circuitry is soldered at the prototyping area.

The 89C51 has a single UART for serial communication. The UART is RS-232 buffered and brought out at J2. It supports In-System programming of the 89C51 Flash. When not programming the Flash, the LAB PRO-51's serial port is available to the user's application.

There are 8 LEDs controlled by Port 1, and an 8-position DIP Switch connected to Port 0. These can be used for simple I/O in user projects.

Board circuitry provides a power-up reset. That is, upon applying +9 VDC to the board, the 89C51 is reset. A push button switch at SW3 provides an additional method for resetting the board.

Switch SW2 is used to select either the programming mode, or the run mode. With SW2 in the PROG position (down), -PSEN is tied to GND. In this case, the board enters the programming mode following a board reset. When SW2 is in the RUN position (up), -PSEN is floating. Following a hardware reset, the board will be in the run mode, and will execute software programmed into the on-chip Flash. This, of course, assumes that the Status byte is 0. Please see Part III., Section C. for details on the Status byte.

VIII. Warranty

The products sold hereunder are warranted as free from defects of materials and workmanship and in conformance with specifications for a period of one year from date of shipment. There are no other oral, statutory, or implied warranties. In no event will the seller be liable for special or consequential damages as a result of alleged breach of this warranty provision. Under no circumstances should the LAB PRO-51 Single Board Computer be used in life support systems or applications where life or property is at stake. Seller's obligation hereunder shall be limited to replacing F.O.B. its plant in Columbus, Ohio or refund the purchase price of any such product which fails to conform to specifications therefore, provided that (1) written notice of such defect or failure is received by seller from purchaser within one year after the date of shipment of such products by seller, and (2) such defects, in the opinion of the seller, shall not have arisen from improper use. The absence of specifications within the specified time of notice, require the purchaser to send said products, transportation prepaid, to the seller for its examination and inspection.

WARNING!!!

Under no circumstances should the LAB PRO-51 Single Board Computer be used in life support systems or applications where life or property is at stake.

IX. Appendices

A. Appendix A - Parts List

The following list identifies parts used on the assembled and tested version of the LAB PRO-51. All resistors are 1/4 Watt, 5%. A "*" indicates that a component may be installed on the board, but is not supplied with the assembled and tested LAB PRO-51.

	Qty.	Description	Designation
1.)	I.C.'s		
	1	7805	U1
	1	DS275	U2
	1	P89C51RB2	U3
	1	74HC245	U4
	1	DS1233	U5
2.)	I.C. Sockets		
	1	44 Pin PLCC	U3
	1	8 Pin DIP	U2
	1	20 Pin DIP	U4
3.)	Resistors		
	1	20K Ohm	R1
	1	4.7K Ohm	R2
5.)	Resistor Networks		
	1	1K Ohm, 9 Element	RN1
	1	10K Ohm, 9 Element	RN2
4.)	Capacitors		
	1	47 ufd Electrolytic	C1
	2	33 pfd	C2,C7
	7	.1 ufd Mono By-pass	C3,C4,C6,C8 C9,C11,C13
	1	220 ufd Electrolytic	C5 *
	1	47 ufd Electrolytic	C10 *
	1	100 ufd Electrolytic	C12
	1	100 pfd	C14

5.) Misc. Components and Parts

1	11.0592 MHz Crystal	XTAL1
1	2N3906	TR1
8	LEDs, T1	L0 through L7
1	8-Pos. DIP Switch	SW1
1	SPDT Switch	SW2
1	Reset Switch	SW3
1	User's Manual	

6.) Misc. Hardware

1	AC Adapter Jack	J1
1	DB-09 Female Conn.	J2
1	4 Pos. Terminal Conn.	J3
1	1 by 36 Female Header	J4
1	1 by 9 Female Header	J6
1	PC Board	LAB PRO-51
1	Solderless Breadboard	* (optional)
1	Heat Sink	U1
1	4-40 Screw and Nut	U1
4	Rubber Feet	

B. Appendix B - Useful WWW Links

The Internet is a great source for data sheets, application notes, and software relating to the LAB PRO-51. Please see the following links:

1.) Philips Home Page

www.philips.com

2.) P89C51 Data Sheets and Application Notes

www.semiconductors.philips.com/mcu/

3.) In-System Programming Software and Tutorial Download Page

www.semiconductors.philips.com/mcu/download/80c51/flash/

4.) Dallas Semiconductor Home Page

www.dalsemi.com

5.) Allen Systems Home Page

www.allen-systems.com

C. Appendix C - Schematic

The next two pages contain the schematic for the LAB PRO-51.

D. Appendix D - References

The following references should be consulted for additional details regarding devices used on the LAB PRO-51: Most of these are downloadable from the Philips Web Site.

1. P89C51RB2/P89C51RC2/ P89C51RD2 Datasheet, Philips Semiconductors, 6/27/2001. Download Filename: R89C51RX2_8.pdf

2. AN461 In-circuit and In-application programming of the 89C51Rx+/Rx2/66x microcontrollers, Philips Semiconductors, 7/28/2000. Download filename: AN461_7.pdf

3. Flash Microcontroller Frequently Asked Questions and Answers, Philips Semiconductors, 4/8/1999. Download Filename: ispfaq.zip

4. "System Extension Data Book", Dallas Semiconductor, 1994-1995.

E. Appendix E - LAB PRO-51 Errata

The following errors have been identified on the LAB PRO-51 single board computer:

As of 9/1/01, no problems have been identified with the LAB PRO-51.

Flash Microcontroller
Frequently Asked Questions and Answers

#1

Question: How do I get the WinISP software utility to program 89C51RC+ and 89C51RD+ microcontrollers below 10MHz?

Answer: This problem was fixed in WinISP Ver 2.14. Download the latest WinISP version from http://www.semiconductors.philipsmcu.com/flash/flash.html. **HOTLINK**

#2

Question: I programmed and verified code on the 89C51RC+ and 89C51RD+. But, I cannot get the parts to execute the code in my application. How can I get my code to execute?

Answer: The status byte must be 00H and PSEN must be high for user code to run. Program the status byte to 00H with a programmer or with ISP and drive PSEN high during reset. See Application Note AN461 for more details. **HOTLINK**

#3

Question: I have programmed and verified code on the 89C51RC+ and 89C51RD+ using the reference design in Applications Note AN461. **HOTLINK**. How can I get my code to run on the reference design?

Answer: The status byte must be 00H and S2 on the reference design must be in the "NORMAL" position for user code to run. Program the status byte to 00H with the WinISP utility, change S2 to the "NORMAL" position, and reset the microcontroller with S1.

#4

Question: I have programmed and run code on the 89C51RC+ and 89C51RD+. Now I cannot get the 89C51RC+ and 89C51RD+ to erase and program as before. What can I do?

Answer: You will need to do a hardware activation of the boot loader. Drive PSEN low and EA/VPP to 12V during reset. See Application Note AN461 for more details. **HOTLINK** If you using the reference design in AN461, the loader is hardware activated by changing S2 to the "TEST" position and resetting the microcontroller with S1.

#5

Question: I have 89C51RC+ and 89C51RD+ microcontrollers, and they do not program or erase consistently. What can I do?

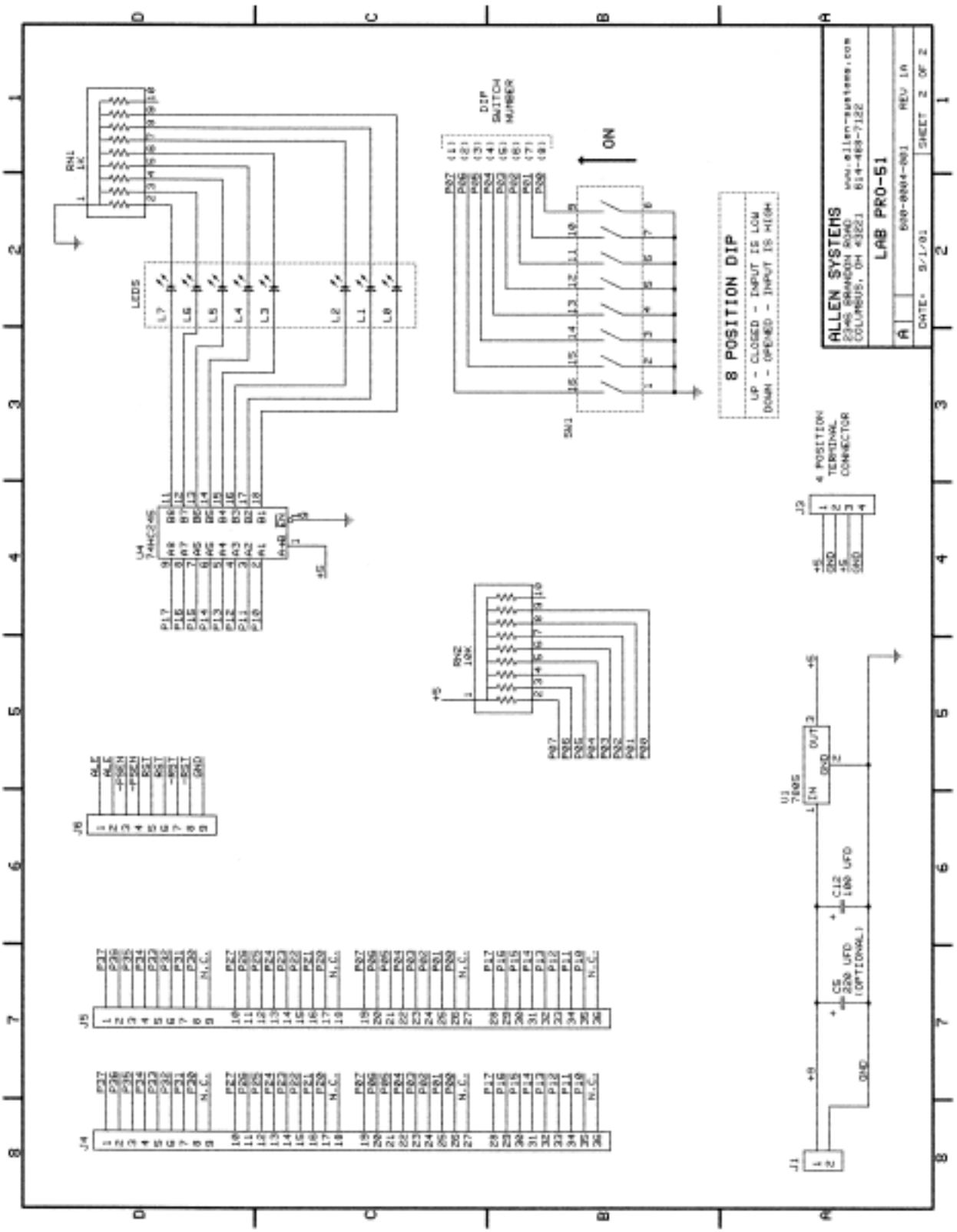
Answer: Check if the package marking second line begins with "MC". Parts marked with MC were early Engineering Samples with incomplete test coverage. If you have parts marked MC, send a request to 80C51_help@sv.sc.philips.com to have new samples sent to you.

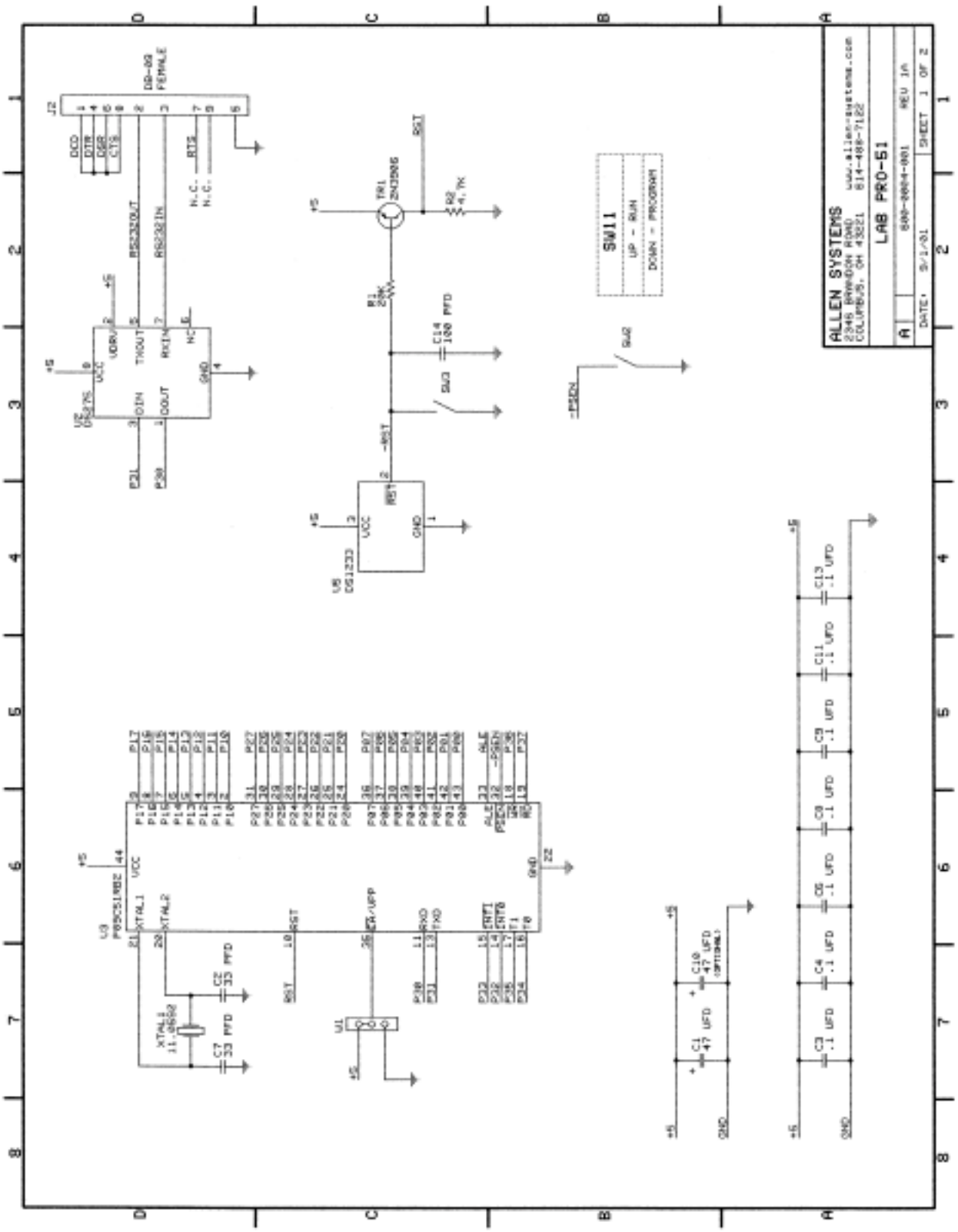
#6
Question: I am programming a P89C51U (or P89C52U or P89C54U or P89C58U). The part programs and verifies but will not run in my application. How can I get my code to execute?

Answer: Some early Engineering Samples were incorrectly configured at the factory. If you have samples, send a request to 80C51_help@sv.sc.philips.com to have new samples sent to you. If you have production parts with this problem, return the parts to the factory using the standard Philips Quality Return procedure. Call your local Philips office for details.

#7
Question: I am programming a P89C52U (or P89C54U) flash microcontroller and selecting P89C52 (or P89C54) from the menu. The part will not program. What do I do?

Answer: P89C52U and P89C54U flash microcontrollers require different programming algorithms than earlier P89C52 and P89C54 devices. Check the available programming support at Philips Web Site: /microcontrol/support/80C51/flashprog/ **HOTLINK**. If your programming vendor supports the 89C52U and 89C54U products, download the latest software release from your programming vendor and select P89C52U or 89C54U from the programmer menu.


ALLEN SYSTEMS
2245 BRANDON ROAD
COLUMBUS, OH 43221
www.allen-systems.com
614-488-7122
LAB PRO-51
600-0004-001
REV 1A
DATE: 9/1/01
SHEET 2 OF 2
8 POSITION DIP
UP - CLOSED - INPUT IS LOW
DOWN - OPENED - INPUT IS HIGH
ON
DIP SWITCH NUMBER
LEDS
RN1 1K
RN2 10K
4 POSITION TERMINAL CONNECTOR
74HC245
7805
C5 220 UFD (OPTIONAL)
C12 100 UFD
GND
+5


ALLEN SYSTEMS
2345 BROWDON ROAD
COLUMBUS, OH 43221
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LAB PRO-51
040-0004-001
REV 1A
DATE: 9/1/01
SHEET 1 OF 2
SW11
UP - RUN
DOWN - PROGRAM
DB-9S FEMALE
DCD
DTR
DSR
CTS
RTS
N.C.
N.C.
RS232OUT
RS232IN
MAX232
VCC
VDRV
TXOUT
RXIN
NC
GND
DIN
DOUT
P31
P30
DS1233
RST
2N3906
R1
20K
R2
4.7K
C14
100 PFD
SW3
SW2
-PSEN
P89C51RB2
XTAL1
XTAL2
EA/VPP
RXD
TXD
INT1
INT0
T1
T0
ALE
-PSEN
RD
WR
GND
XTAL1
11.0592
C2
33 PFD
C7
33 PFD
U1
C10
47 UFD
OPTIONAL
C1
47 UFD
C3
.1 UFD
C4
.1 UFD
C5
.1 UFD
C6
.1 UFD
C8
.1 UFD
C9
.1 UFD
C11
.1 UFD
C13
.1 UFD

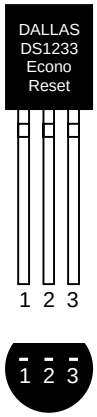
DS1233
5V EconoReset

www.dalsemi.com

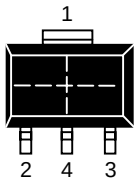
FEATURES

- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Internal circuitry debounces pushbutton switch
- Maintains reset for 350 ms after V_{CC} returns to an in-tolerance condition or pushbutton released
- Accurate 5%, 10% or 15% microprocessor 5V power supply monitoring
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- Low-cost TO-92 package or surface-mount SOT-223 package
- Internal 5kΩ pull-up resistor
- Operating temperature of -40°C to +85°C

PIN ASSIGNMENT



TO-92 PACKAGE
See Mech.
Drawings Section



SOT-223 PACKAGE
See Mech.
Drawings Section

PIN DESCRIPTION

PIN 1	GROUND
PIN 2	$\overline{\text{RESET}}$
PIN 3	V_{CC}
PIN 4	GROUND (SOT-223 ONLY)

DESCRIPTION

The DS1233 EconoReset monitors two vital conditions for a microprocessor: power supply and external override. A precision temperature compensated reference and comparator circuit are used to monitor the status of the power supply (V_{CC}). When an out-of-tolerance condition is detected, an internal power-fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 350 ms to allow the power supply and processor to stabilize. The second function of the DS1233 is pushbutton reset control. The DS1233 debounces a pushbutton closure and will generate a 350 ms reset pulse upon release.

OPERATION - POWER MONITOR

The DS1233 provides the functions of detecting out-of-tolerance power supply conditions and warning a processor-based system of impending power failure. When V_{CC} is detected as out-of-tolerance, as defined by the tolerance of the part selected, the $\overline{\text{RST}}$ signal is asserted. On power-up, $\overline{\text{RST}}$ is kept active for approximately 350 ms after the power supply has reached the selected tolerance. This allows the power supply and microprocessor to stabilize before $\overline{\text{RST}}$ is released.

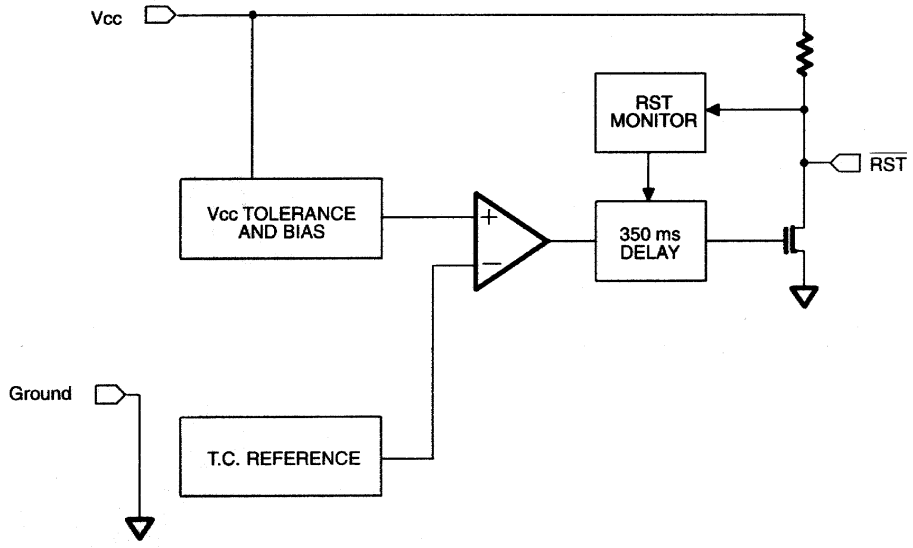
OPERATION - PUSHBUTTON RESET

The DS1233 provides for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS1233 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge is detected, the DS1233 will debounce the switch by pulling the $\overline{RST}$ line low. After the internal timer has expired, the DS1233 will continue to monitor the $\overline{RST}$ line. If the line is still low, the DS1233 will continue to monitor the line looking for a rising edge. Upon detecting a release, the DS1233 will force the $\overline{RST}$ line low and hold it low for 350 ms.

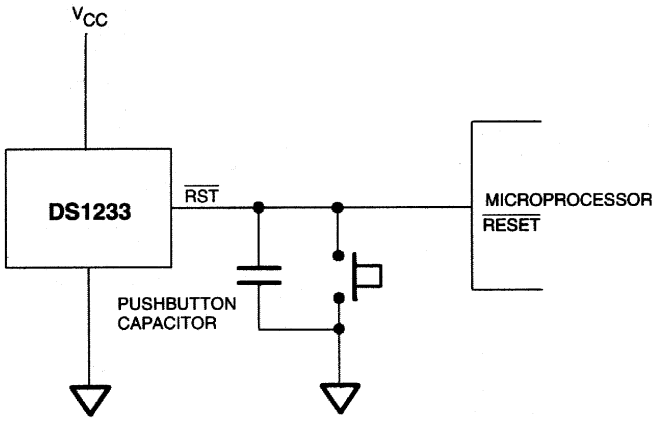
NOTE:

For proper operation with an external pushbutton, a capacitor between 100 pF and 0.01 µF must be connected between $\overline{RST}$ and ground. In applications where additional reset current is required, a minimum capacitance of 500 pF should be used, along with a parallel external pull-up resistor of 1 kΩ minimum.

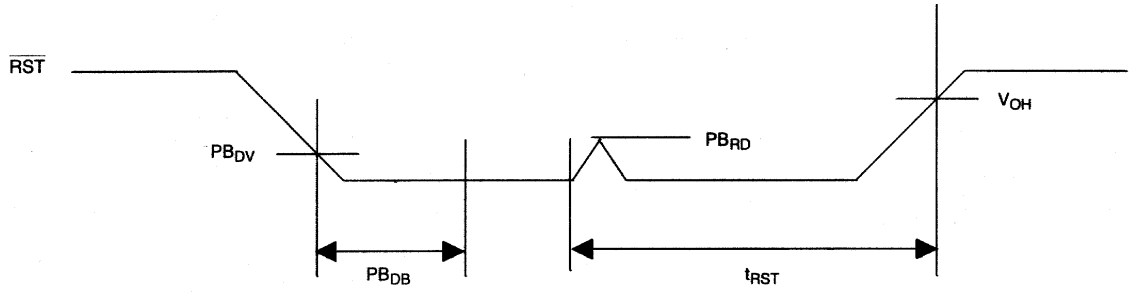
BLOCK DIAGRAM Figure 1



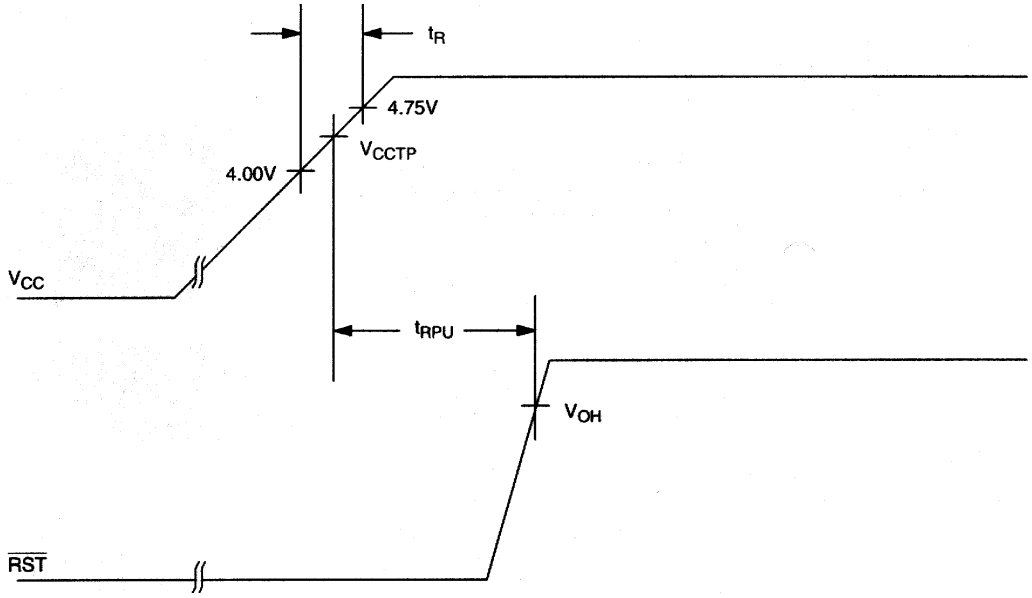
APPLICATION EXAMPLE Figure 2



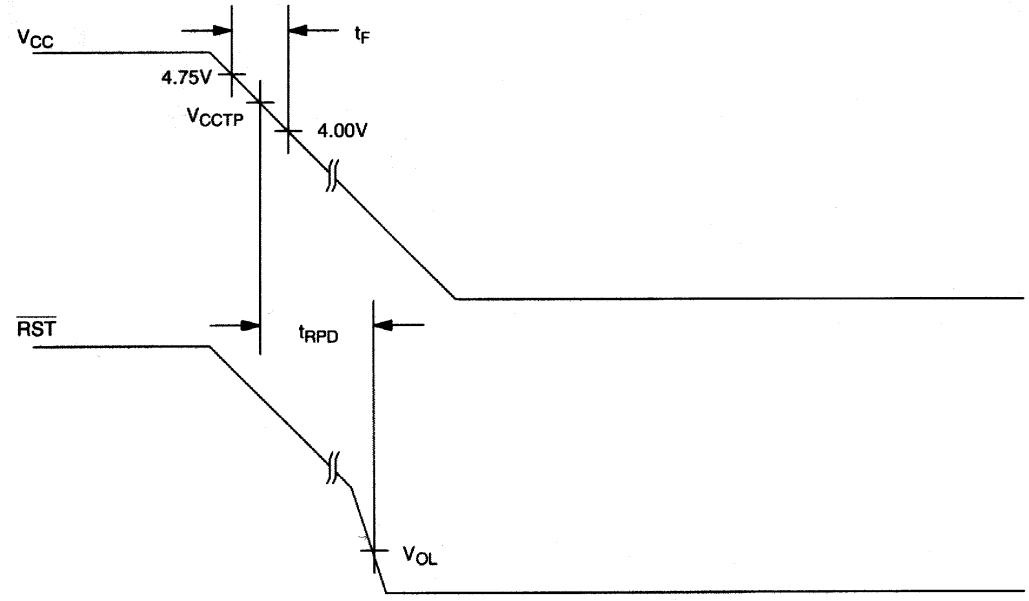
PUSHBUTTON RESET Figure 3



POWER UP Figure 4



POWER DOWN Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	-0.5V to V_{CC} +0.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.2	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{DD}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Low Level @ $\overline{RST}$	V_{OL}			0.4	V	1
Output Current @ 0.4V	I_{OL}	+8			mA	
Operating Current	I_{CC}			50	µA	
V_{CC} Trip Point 5%	V_{CCTP0}	4.50	4.625	4.75	V	1
V_{CC} Trip Point 10%	V_{CCTP1}	4.25	4.375	4.49	V	1
V_{CC} Trip Point 15%	V_{CCTP2}	4.0	4.125	4.24	V	1
Output Capacitance	C_{OUT}			10	pF	
Pushbutton Detect	PB_{DV}	1.8		3.3	V	1
Pushbutton Release	PB_{RD}		0.3	0.8	V	1, 2
Internal Pull-Up Resistor	R_P	3.75	5	6.25	kΩ	

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RESET Active Time	t_{RST}	250	350	450	ms	
V_{CC} Detect to $\overline{RST}$	t_{RPD}			100	ns	
V_{CC} Slew Rate (4.75V - 4.00V)	t_F	300			µs	
V_{CC} Slew Rate (4.00V - 4.75V)	t_R	0			ns	
Pushbutton Debounce	PB_{DB}	250	350	450	ms	
V_{CC} Detect to RST	t_{RPU}	250	350	450	ms	

NOTES:

1. All voltages are referenced to ground.
2. With a 100 pF to 0.01 µF capacitor connected from $\overline{RST}$ to ground.

ECONORESET SELECTION GUIDE

		VCC TRIP POINT			PUSHBUTTON DETECT		
		MIN	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**
5V	DS1233-15	4.0	4.125	4.24	2.4	-	3.3
	DS1233-10	4.25	4.375	4.49	2.4	-	3.3
	DS1233-5	4.5	4.625	4.75	2.4	-	3.3
	DS1233D-15	4.0	4.125	4.24	N/A		N/A
	DS1233D-10	4.25	4.375	4.49	N/A		N/A
	DS1233D-5	4.5	4.625	4.75	N/A		N/A
	DS1833-15	4.0	4.125	4.24	N/A		N/A
	DS1833-10	4.25	4.375	4.49	N/A		N/A
	DS1833-5	4.5	4.625	4.75	N/A		N/A
3.3V	DS1233A-15	2.64	2.72	2.80	1.8	-	3.0
	DS1233A-10	2.8	2.88	2.97	1.8	-	3.0

DS275
Line-Powered RS-232 Transceiver Chip

www.dalsemi.com

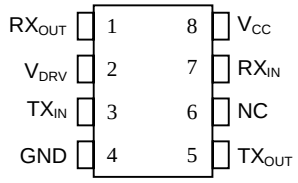
FEATURES

- Low-power serial transmitter/receiver for battery-backed systems
- Transmitter steals power from receive signal line to save power
- Ultra-low static current, even when connected to RS-232-E port
- Variable transmitter level from +5 to +12 volts
- Compatible with RS-232-E signals
- Available in 8-pin, 150 mil wide SOIC package (DS275S)
- Low-power CMOS

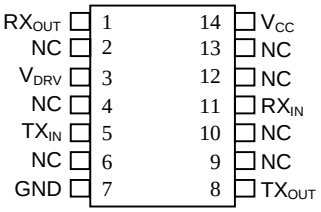
ORDERING INFORMATION

DS275	8-pin DIP
DS275S	8-pin SOIC
DS275E	14-pin TSSOP

PIN ASSIGNMENT



DS275 8-Pin DIP (300-mil)
DS275 8-Pin SOIC (150-mil)



DS275E 14-Pin TSSOP

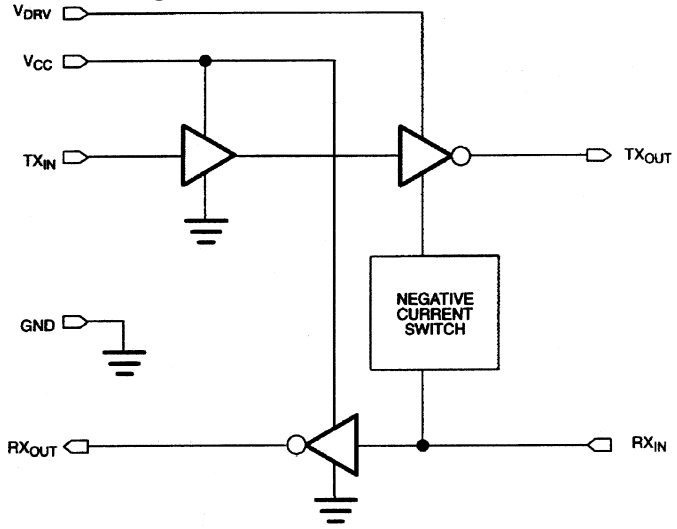
PIN DESCRIPTION

RX_{OUT}	- RS-232 Receiver Output
V_{DRV}	- Transmit driver +V
TX_{IN}	- RS-232 Driver Input
GND	- System Ground (0V)
TX_{OUT}	- RS-232 Driver Output
NC	- No Connection
RX_{IN}	- RS-232 Receive Input
V_{CC}	-System Logic Supply (+5V)

DESCRIPTION

The DS275 Line-Powered RS-232 Transceiver Chip is a CMOS device that provides a low-cost, very low-power interface to RS-232 serial ports. The receiver input translates RS-232 signal levels to common CMOS/TTL levels. The transmitter employs a unique circuit which steals current from the receive RS-232 signal when that signal is in a negative state (marking). Since most serial communication ports remain in a negative state statically, using the receive signal for negative power greatly reduces the DS275's static power consumption. This feature is especially important for battery-powered systems such as laptop computers, remote sensors, and portable medical instruments. During an actual communication session, the DS275's transmitter will use system power (5-12 volts) for positive transitions while still employing the receive signal for negative transitions.

DS275 BLOCK DIAGRAM Figure 1



OPERATION

Designed for the unique requirements of battery-backed systems, the DS275 provides a low-power half-duplex interface to an RS-232 serial port. Typically, a designer must use an RS-232 device which uses system power during both negative and positive transitions of the transmit signal to the RS-232 port. If the connector to the RS-232 port is left connected for an appreciable time after the communication session has ended, power will statically flow into that port, draining the battery capacity. The DS275 eliminates this static current drain by stealing current from the receive line (RXIN) of the RS-232 port when that line is at a negative level (marking). Since most asynchronous communication over an RS-232 connection typically remains in a marking state when data is not being sent, the DS275 will not consume system power in this condition. System power would only be used when positive-going transitions are needed on the transmit RS-232 output (TXOUT) when data is sent. However, since synchronous communication sessions typically exhibit a very low duty-cycle, overall system power consumption remains low.

RECEIVER SECTION

The RXIN pin is the receive input for an RS-232 signal whose levels can range from ±3 to ±15 volts. A negative data signal is called a mark while a positive data signal is called a space. These signals are inverted and then level-shifted to normal +5-volt CMOS/TTL logic levels. The logic output associated with RXIN is RXOUT which swings from +VCC to ground. Therefore, a mark on RXIN produces a logic 1 at RXOUT; a space produces a logic 0.

The input threshold of RXIN is typically around 1.8 volts with 500 millivolts of hysteresis to improve noise rejection. Therefore, an input positive-going signal must exceed 1.8 volts to cause RXOUT to switch states. A negative-going signal must now be lower than 1.3 volts (typically) to cause RXOUT to switch again. An open on RXIN is interpreted as a mark, producing a logic 1 at RXOUT.

TRANSMITTER SECTION

TXIN is the CMOS/TTL-compatible input for digital data from the user system. A logic 1 at TXIN produces a mark (negative data signal) at TXOUT while a logic 0 produces a space (positive data signal). As mentioned earlier, the transmitter section employs a unique driver design that uses the RXIN line for swinging to negative levels. The RXIN line must be in a marking or idle state to take advantage of this design; if RXIN is in a spacing state, TXOUT will only swing to ground. When TXOUT needs to transition to a positive level, it uses the VDRV power pin for this level. VDRV can be a voltage supply between 5 to 12

volts, and in many situations it can be tied directly to the +5 volt V_{CC} supply. *It is important to note that V_{DRV} must be greater than or equal to V_{CC} at all times.*

The voltage range on V_{DRV} permits the use of a 9-volt battery in order to provide a higher voltage level when TX_{OUT} is in a space state. When V_{CC} is shut off to the DS275 and V_{DRV} is still powered (as might happen in a battery-backed condition), only a small leakage current (about 50-100 nA) will be drawn. If TX_{OUT} is loaded during such a condition, V_{DRV} will draw current only if RX_{IN} is not in a negative state. During normal operation (V_{CC}=5 volts), V_{DRV} will draw less than 2 uA when TX_{OUT} is marking. Of course, when TX_{OUT} is spacing, V_{DRV} will draw substantially more current— about 3 mA, depending upon its voltage and the impedance that TX_{OUT} sees.

The TX_{OUT} output is slew rate-limited to less than 30 volts/us in accordance with RS-232 specifications. In the event TX_{OUT} should be inadvertently shorted to ground, internal current-limiting circuitry prevents damage, even if continuously shorted.

RS-232 COMPATIBILITY

The intent of the DS275 is not so much to meet all the requirements of the RS-232 specification as to offer a low-power solution that will work with most RS-232 ports with a connector length of less than 10 feet. As a prime example, the DS275 will not meet the RS-232 requirement that the signal levels be at least ±5 volts minimum when terminated by a 3 kΩ load and V_{DRV} = +5 volts. Typically a voltage of 4 volts will be present at TX_{OUT} when spacing. However, since most RS-232 receivers will correctly interpret any voltage over 2 volts as a space, there will be no problem transmitting data.

APPLICATIONS INFORMATION

The DS275 is designed as a low-cost, RS-232-E interface expressly tailored for the unique requirements of battery-operated handheld products. As shown in the electrical specifications, the DS275 draws exceptionally low operating and static current. During normal operation when data from the handheld system is sent from the TX_{OUT} output, the DS275 only draws significant V_{DRV} current when TX_{OUT} transitions positively (spacing). This current flows primarily into the RS-232 receiver's 3-7 kΩ load at the other end of the attaching cable. When TX_{OUT} is marking (a negative data signal), the V_{DRV} current falls dramatically since the negative voltage is provided by the transmit signal from the other end of the cable. This represents a large reduction in overall operating current, since typical RS-232 interface chips use charge-pump circuits to establish both positive and negative levels at the transmit driver output.

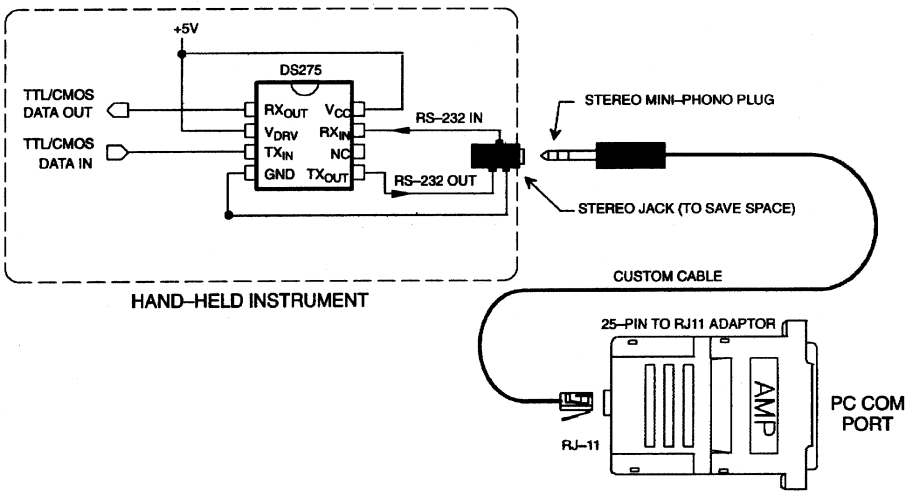
To obtain the lowest power consumption from the DS275, observe the following guidelines. First, to minimize V_{DRV} current when connected to an RS-232 port, always maintain TX_{IN} at a logic 1 when data is not being transmitted (idle state). This will force TX_{OUT} into the marking state, minimizing V_{DRV} current. Second, V_{DRV} current will drop to less than 100 nA when V_{CC} is grounded. Therefore, if V_{DRV} is tied directly to the system battery, the logic +5 volts can be turned off to achieve the lowest possible power state.

FULL-DUPLEX OPERATION

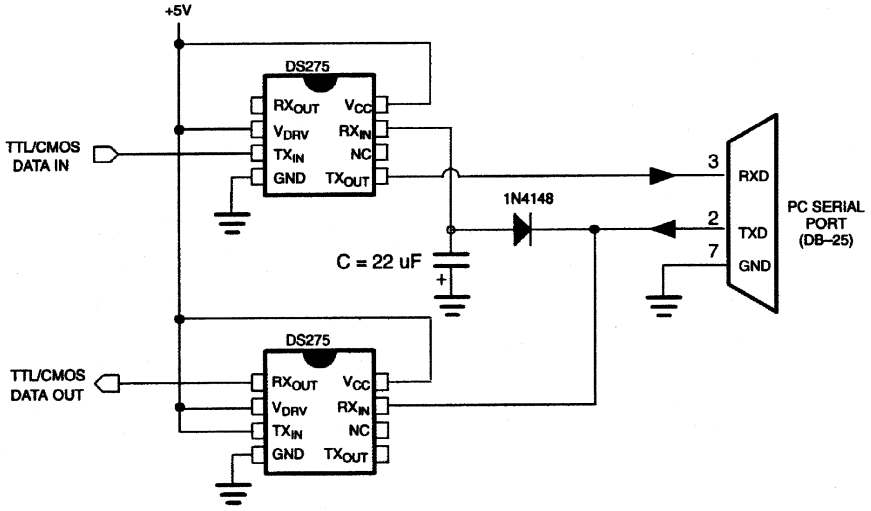
The DS275 is intended primarily for half-duplex operation; that is, RX_{IN} should remain idle in the marking state when transmitting data out TX_{OUT} and visa versa. However, the part can be operated full-duplex with most RS-232-E serial ports since signals swinging between 0 and +5V will usually be correctly interpreted by an RS-232-E receiver device. The 5-volt swing occurs when TX_{OUT} attempts to swing negative while RX_{IN} is at a positive voltage, which turns on an internal weak pulldown to ground for the TX_{OUT} driver's negative reference. So, transmit mark signals at TX_{OUT} may have voltage jumps from some negative value (corresponding to RX_{IN} marking) to approximately ground. One possible

problem that may occur in this case is if the receiver at the other end requires a negative voltage for recognizing a mark. In this situation, the full-duplex circuit shown in Figure 3 can be used as analternative. The 22 µF capacitor forms a negative-charge reservoir; consequently, when the TXD line is spacing (positive), TXOUT still has a negative source available for a time period determined by the capacitor and the load resistance at the other end (3-7 kΩ). This circuit was tested from 150-19,200 bps with error-free operation using a SN75154 Quad Line Receiver as the receiver for the TXOUT signal. Note that the SN75154 can have a marking input threshold below ground; hence there is the need for TXOUT to swing both positive and negative in full-duplex operation with this device.

HANDHELD RS-232-C APPLICATION USING A STEREO MINI-JACK Figure 2



FULL-DUPLEX CIRCUIT USING NEGATIVE-CHARGE STORAGE Figure 3



NOTE:

The capacitor stores negative charge whenever the TXD signal from the PC serial port is in a marking data state (a negative voltage that is typically -10 volts). The top DS275's TXOUT uses this negative charge reservoir when it is in a marking state. The capacitor will discharge to 0 volts when the TXD line is spacing (and TXOUT is still marking) at a time constant determined by its value and the value of the load resistance reflected back to TXOUT. However, when TXD is marking the capacitor will quickly charge back to -10 volts. Note that TXD remains in a marking state when idle, which improves the performance of this circuit.

ABSOLUTE MAXIMUM RATINGS*

VCC	-0.3 to +7.0 volts
VDRV	-0.3 to +13.0 volts

RX_{IN}	±15 volts
TX_{IN}	-0.3 to V_{CC} + 0.3 volts
TX_{OUT}	±15 volts
RX_{OUT}	-0.3 to V_{CC} + 0.3 volts
Storage Temperature	-55°C to +125°C
Operating Temperature	0°C to 70°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic Supply	V_{CC}	4.5	5.0	5.5	V	1
Transmit Driver Supply	V_{DRV}	4.5	5-12	13.0	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC}+0.3	V	2
Logic 0 Input	V_{IL}	-0.3		+0.8	V	
RS-232 Input Range (RX_{IN})	V_{RS}	-15		+15	V	
Dynamic Supply Current						
$TX_{IN} = V_{CC}$	I_{DRV1}		400	800	µA	
	I_{CC1}		40	100	µA	3
TX_{IN} = GND	I_{DRV1}		3.8	5.0	µA	
	I_{CC1}		40	100	µA	
Static Supply Current						
$TX_{IN} = V_{CC}$	I_{DRV2}		1.5	10.0	µA	
	I_{CC2}		10.0	15.0	µA	4
TX_{IN} = GND	I_{DRV2}		3.8	5.0	mA	
	I_{CC2}		10.0	20.0	µA	
Driver Leakage Current (V_{CC}=0V)	I_{DRV3}		0.05	1.0	µA	5

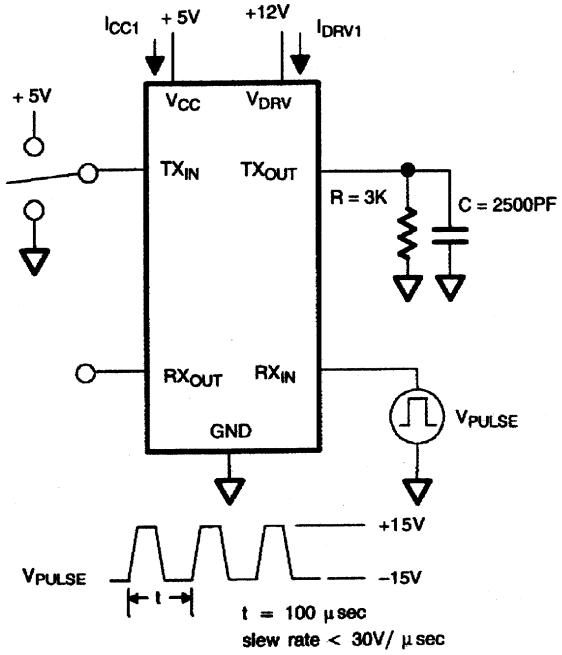
DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = V_{DRV} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TX_{OUT} Level High	V_{OTXH}	3.5	4.0	5.0	V	6
TX_{OUT} Level Low	V_{OTXL}	-8.5	-9.0		V	7
TX_{OUT} Short Circuit Current	I_{SC}		+60	+85	mA	
TX_{OUT} Output Slew Rate	t_{SR}			30	V/µs	
Propagation Delay	t_{PD}		5		µs	8
RX_{IN} Input Threshold Low	V_{TL}	0.8	1.2	1.6	V	
RX_{IN} Input Threshold High	V_{TH}	1.6	2.0	2.4	V	
RX_{IN} Threshold Hysteresis	V_{HYS}	0.5	0.8		V	9
RX_{OUT} Output Current @ 2.4V	I_{OH}	-1.0			mA	
RX_{OUT} Output Current @ 0.4V	I_{OL}			3.2	mA	

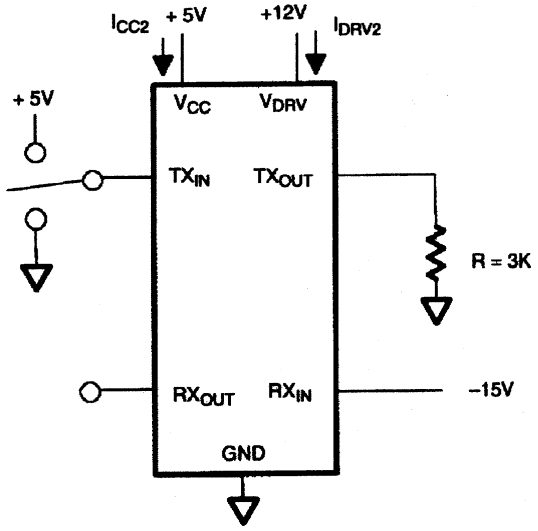
NOTES:

1. V_{DRV} must be greater than or equal to V_{CC}.
2. V_{CC} = V_{DRV} = 5V ± 10%.
3. See test circuit in Figure 4.
4. See test circuit in Figure 5.
5. See test circuit in Figure 6.
6. TX_{IN} = V_{IL} and TX_{OUT} loaded by 3 kΩ to ground.
7. TX_{IN} = V_{IH}, RX_{IN} = -10 volts and TX_{OUT} loaded by 3 kΩ to ground.
8. TX_{IN} to TX_{OUT} - see Figure 7.
9. V_{HYS} = V_{TH} - V_{TL}.

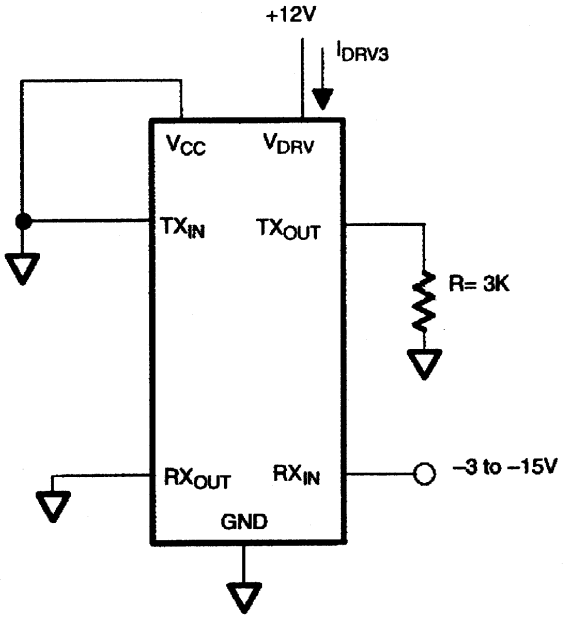
DYNAMIC OPERATING CURRENT TEST CIRCUIT Figure 4



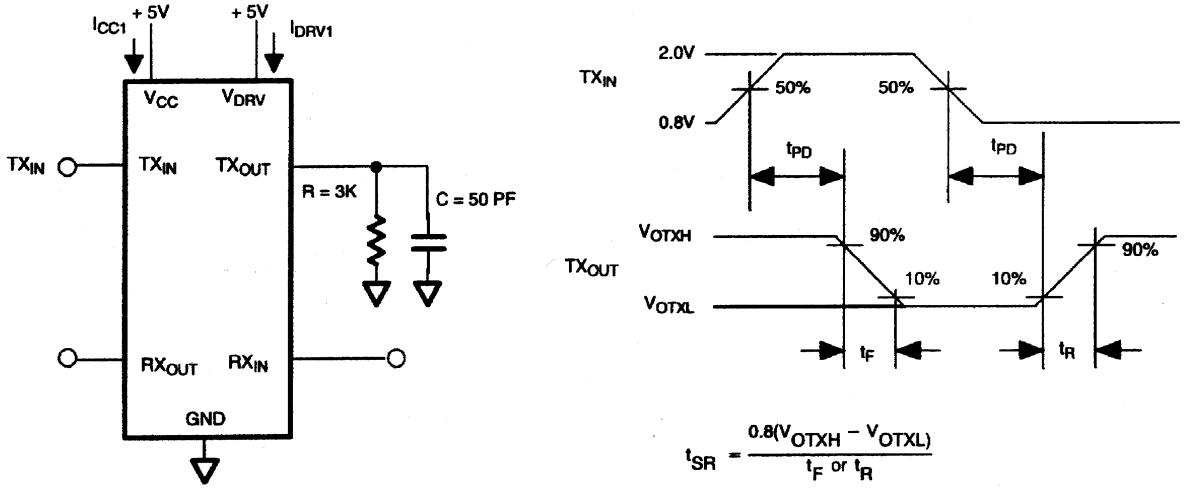
STATIC OPERATING CURRENT TEST CIRCUIT Figure 5



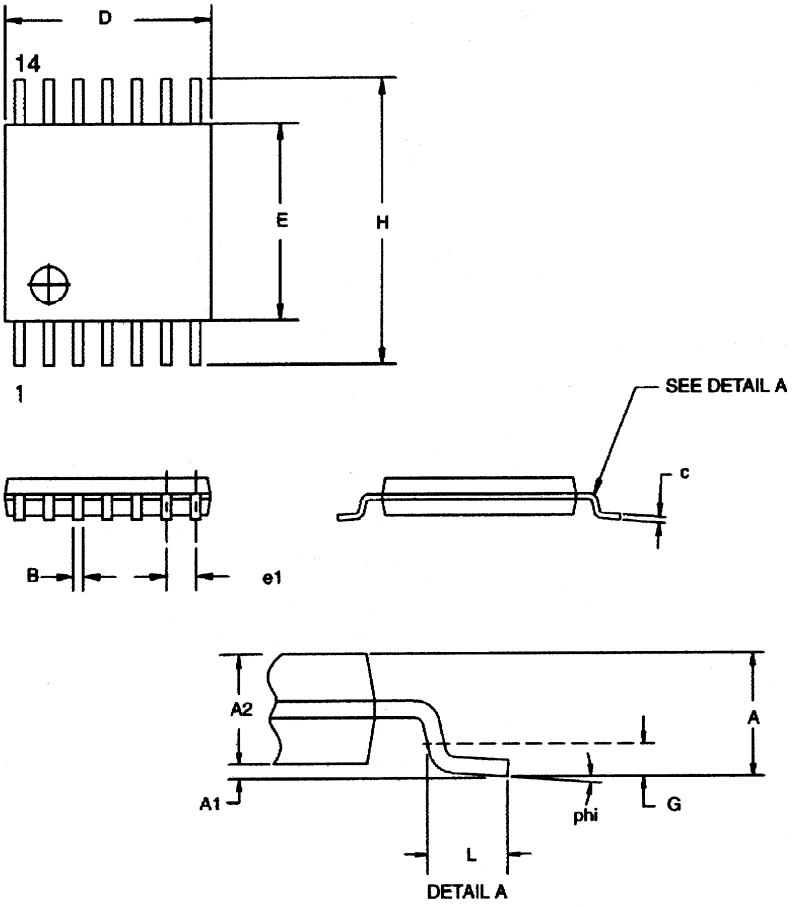
DRIVER LEAKAGE TEST CIRCUIT Figure 6



PROPAGATION DELAY TEST CIRCUIT Figure 7



DS275E 14-PIN TSSOP



DIM	14-PIN	
	MIN	MAX
A MM	-	1.10
A1 MM	0.05	-
A2 MM	0.75	1.05
B MM	0.18	0.30
C MM	0.09	0.18
D MM	4.90	5.10
E MM	4.40 NOM	
e1 MM	0.65 BSC	
G MM	0.25 REF	
H MM	6.25	6.55
L MM	0.50	0.70
phi	0°	8°

DATA SHEET

P89C51RB2/P89C51RC2/P89C51RD2

80C51 8-bit Flash microcontroller family

16KB/32KB/64KB ISP/IAP Flash with 512B/512B/1KB RAM

Preliminary specification
Supersedes data of 2001 Jan 11
IC28 Data Handbook

2001 Jun 27

Philips
Semiconductors

PHILIPS

80C51 8-bit Flash microcontroller family
16KB/32KB/64KB ISP/IAP Flash with 512B/512B/1KB RAM

P89C51RB2/P89C51RC2/ P89C51RD2

DESCRIPTION

The P89C51RB2/RC2/RD2 device contains a non-volatile 16KB/32KB/64KB Flash program memory that is both parallel programmable and serial In-System and In-Application Programmable. In-System Programming (ISP) allows the user to download new code while the microcontroller sits in the application. In-Application Programming (IAP) means that the microcontroller fetches new program code and reprograms itself while in the system. This allows for remote programming over a modem link. A default serial loader (boot loader) program in ROM allows serial In-System programming of the Flash memory via the UART without the need for a loader in the Flash code. For In-Application Programming, the user program erases and reprograms the Flash memory by use of standard routines contained in ROM.

This device executes one machine cycle in 6 clock cycles, hence providing twice the speed of a conventional 80C51. An OTP configuration bit lets the user select conventional 12 clock timing if desired.

This device is a Single-Chip 8-Bit Microcontroller manufactured in advanced CMOS process and is a derivative of the 80C51 microcontroller family. The instruction set is 100% compatible with the 80C51 instruction set.

The device also has four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, four-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits.

The added features of the P89C51RB2/RC2/RD2 makes it a powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control.

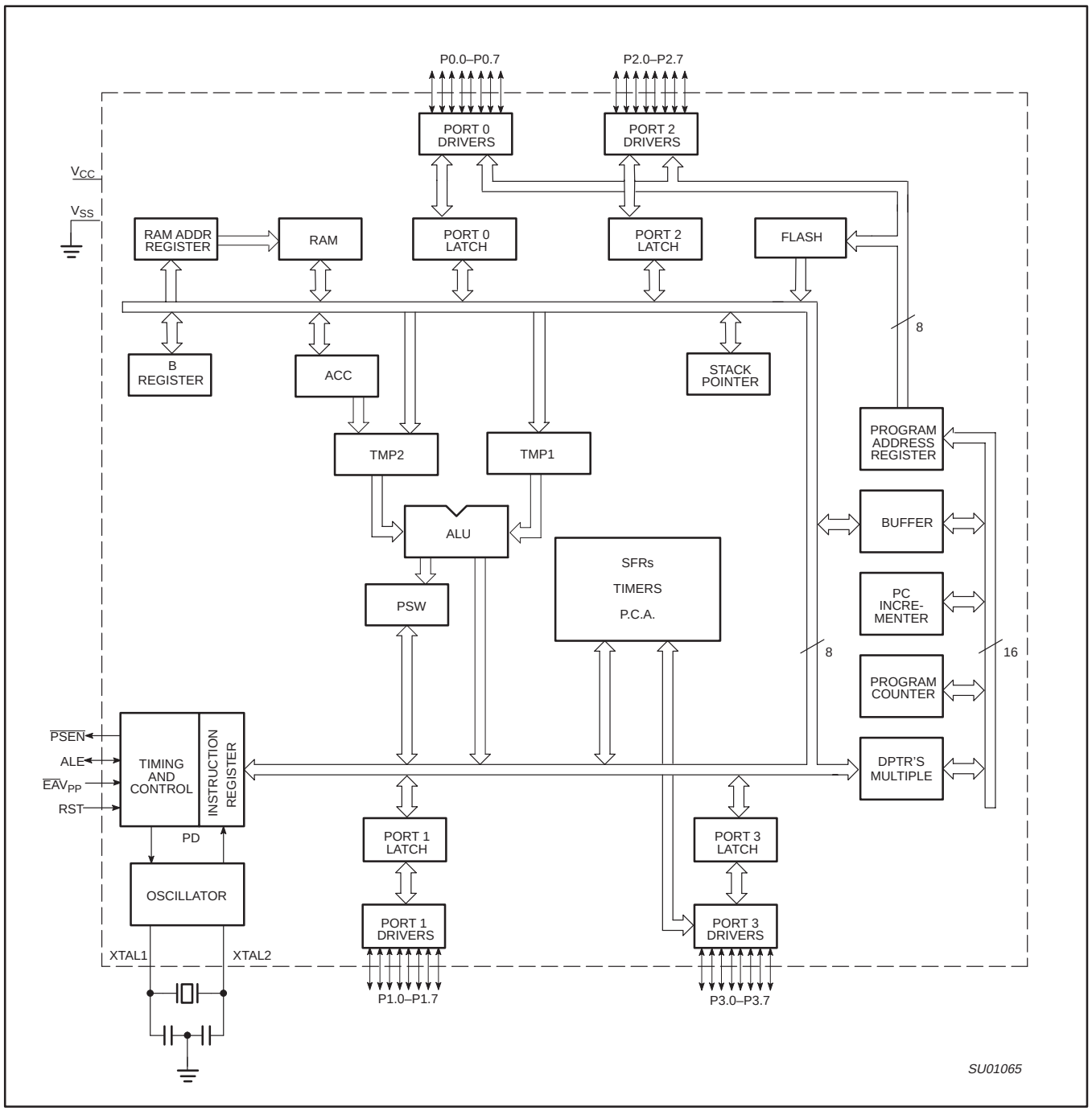
FEATURES

- 80C51 Central Processing Unit
- On-chip Flash Program Memory with In-System Programming (ISP) and In-Application Programming (IAP) capability
- Boot ROM contains low level Flash programming routines for downloading via the UART
- Can be programmed by the end-user application (IAP)
- Parallel programming with 87C51 compatible hardware interface to programmer
- 6 clocks per machine cycle operation (standard)
- 12 clocks per machine cycle operation (optional)
- Speed up to 20 MHz with 6 clock cycles per machine cycle (40 MHz equivalent performance); up to 33 MHz with 12 clocks per machine cycle
- Fully static operation
- RAM expandable externally to 64 kbytes
- 4 level priority interrupt
- 7 interrupt sources
- Four 8-bit I/O ports
- Full-duplex enhanced UART
  - Framing error detection
  - Automatic address recognition
- Power control modes
  - Clock can be stopped and resumed
  - Idle mode
  - Power down mode
- Programmable clock out
- Second DPTR register
- Asynchronous port reset
- Low EMI (inhibit ALE)
- Programmable Counter Array (PCA)
  - PWM
  - Capture/compare

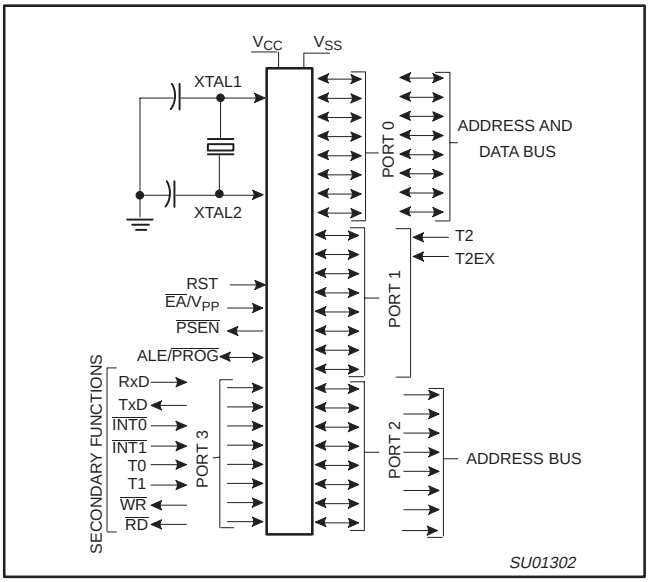
ORDERING INFORMATION

	PHILIPS (EXCEPT NORTH AMERICA) PART ORDER NUMBER PART MARKING	PHILIPS NORTH AMERICA PART ORDER NUMBER	MEMORY		TEMPERATURE RANGE (°C) AND PACKAGE	VOLTAGE RANGE	FREQUENCY (MHz)		DWG #
			FLASH	RAM			6 CLOCK MODE	12 CLOCK MODE	
1	P89C51RB2HBA	P89C51RB2BA	16 kB	512 B	0 to +70, PLCC	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
2	P89C51RB2HBBD	P89C51RB2BBD	16 kB	512 B	0 to +70, LQFP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
3	P89C51RC2HBP	P89C51RC2BN	32 kB	512 B	0 to +70, PDIP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT129-1
4	P89C51RC2HBA	P89C51RC2BA	32 kB	512 B	0 to +70, PLCC	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
5	P89C51RC2HFA	P89C51RC2FA	32 kB	512 B	–40 to +85, PLCC	4.75–5.25 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
6	P89C51RC2HBBD	P89C51RC2BBD	32 kB	512 B	0 to +70, LQFP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
7	P89C51RC2HFBD	P89C51RC2FBD	32 kB	512 B	–40 to +85, LQFP	4.75–5.25 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
8	P89C51RD2HBP	P89C51RD2BN	64 kB	1 kB	0 to +70, PDIP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT129-1
9	P89C51RD2HBA	P89C51RD2BA	64 kB	1 kB	0 to +70, PLCC	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
10	P89C51RD2HBBD	P89C51RD2BBD	64 kB	1 kB	0 to +70, LQFP	4.5–5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1

BLOCK DIAGRAM

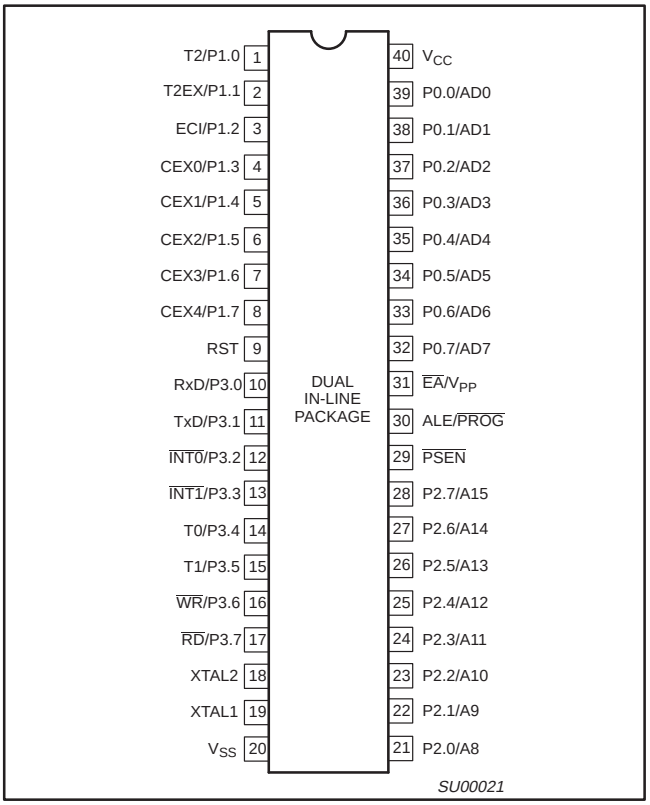


LOGIC SYMBOL

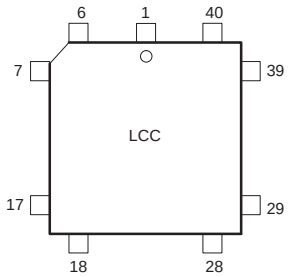


PINNING

Plastic Dual In-Line Package



Plastic Leaded Chip Carrier

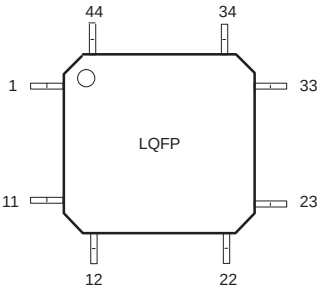


Pin	Function	Pin	Function	Pin	Function
1	NIC*	16	P3.4/T0	31	P2.7/A15
2	P1.0/T2	17	P3.5/T1	32	PSEN
3	P1.1/T2EX	18	P3.6/WR	33	ALE/PROG
4	P1.2/ECI	19	P3.7/RD	34	NIC*
5	P1.3/CEX0	20	XTAL2	35	EA/VPP
6	P1.4/CEX1	21	XTAL1	36	P0.7/AD7
7	P1.5/CEX2	22	VSS	37	P0.6/AD6
8	P1.6/CEX3	23	NIC*	38	P0.5/AD5
9	P1.7/CEX4	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	P3.0/RxD	26	P2.2/A10	41	P0.2/AD2
12	NIC*	27	P2.3/A11	42	P0.1/AD1
13	P3.1/TxD	28	P2.4/A12	43	P0.0/AD0
14	P3.2/INT0	29	P2.5/A13	44	VCC
15	P3.3/INT1	30	P2.6/A14		

* NO INTERNAL CONNECTION

SU00023

Plastic Quad Flat Pack



Pin	Function	Pin	Function	Pin	Function
1	P1.5/CEX2	16	VSS	31	P0.6/AD6
2	P1.6/CEX3	17	NIC*	32	P0.5/AD5
3	P1.7/CEX4	18	P2.0/A8	33	P0.4/AD4
4	RST	19	P2.1/A9	34	P0.3/AD3
5	P3.0/RxD	20	P2.2/A10	35	P0.2/AD2
6	NIC*	21	P2.3/A11	36	P0.1/AD1
7	P3.1/TxD	22	P2.4/A12	37	P0.0/AD0
8	P3.2/INT0	23	P2.5/A13	38	VCC
9	P3.3/INT1	24	P2.6/A14	39	NIC*
10	P3.4/T0	25	P2.7/A15	40	P1.0/T2
11	P3.5/T1	26	PSEN	41	P1.1/T2EX
12	P3.6/WR	27	ALE/PROG	42	P1.2/ECI
13	P3.7/RD	28	NIC*	43	P1.3/CEX0
14	XTAL2	29	EA/VPP	44	P1.4/CEX1
15	XTAL1	30	P0.7/AD7		

* NO INTERNAL CONNECTION

SU01400

PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	PDIP	PLCC	LQFP		
V_{SS}	20	22	16	I	**Ground:** 0 V reference.
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups on all pins except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}).
					Alternate functions for 89C51RB2/RC2/RD2 Port 1 include:
	1	2	40	I/O	**T2 (P1.0):** Timer/Counter 2 external count input/Clockout (see Programmable Clock-Out)
	2	3	41	I	**T2EX (P1.1):** Timer/Counter 2 Reload/Capture/Direction Control
	3	4	42	I	**ECI (P1.2):** External Clock Input to the PCA
	4	5	43	I/O	**CEX0 (P1.3):** Capture/Compare External I/O for PCA module 0
	5	6	44	I/O	**CEX1 (P1.4):** Capture/Compare External I/O for PCA module 1
	6	7	1	I/O	**CEX2 (P1.5):** Capture/Compare External I/O for PCA module 2
	7	8	2	I/O	**CEX3 (P1.6):** Capture/Compare External I/O for PCA module 3
	8	9	3	I/O	**CEX4 (P1.7):** Capture/Compare External I/O for PCA module 4
P2.0–P2.7	21–28	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
					P2.7 must be a “I” to program and erase the device.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 89C51RB2/RC2/RD2, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt
	13	15	9	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE	30	33	27	O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted twice every machine cycle, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction.

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	PDIP	PLCC	LQFP		
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}/V_{PP}$	31	35	29	I	**External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations. If $\overline{EA}$ is held high, the device executes from internal program memory. The value on the $\overline{EA}$ pin is latched when RST is released and any subsequent changes have no effect. This pin also receives the programming supply voltage (V_{PP}) during Flash programming.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

NOTE:
To avoid “latch-up” effect at power-on, the voltage on any pin (other than V_{PP}) must not be higher than V_{CC} + 0.5 V or less than V_{SS} – 0.5 V.

Table 1. Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	–	–	–	–	–	–	EXTRAM	AO	xxxxxx00B
AUXR1#	Auxiliary 1	A2H	–	–	ENBOOT	–	GF2	0	–	DPS	xxxxxxx0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
CCAP0H#	Module 0 Capture High	FAH									xxxxxxxxB
CCAP1H#	Module 1 Capture High	FBH									xxxxxxxxB
CCAP2H#	Module 2 Capture High	FCH									xxxxxxxxB
CCAP3H#	Module 3 Capture High	FDH									xxxxxxxxB
CCAP4H#	Module 4 Capture High	FEH									xxxxxxxxB
CCAP0L#	Module 0 Capture Low	EAH									xxxxxxxxB
CCAP1L#	Module 1 Capture Low	EBH									xxxxxxxxB
CCAP2L#	Module 2 Capture Low	ECH									xxxxxxxxB
CCAP3L#	Module 3 Capture Low	EDH									xxxxxxxxB
CCAP4L#	Module 4 Capture Low	EEH									xxxxxxxxB
CCAPM0#	Module 0 Mode	DAH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM1#	Module 1 Mode	DBH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM2#	Module 2 Mode	DCH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM3#	Module 3 Mode	DDH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM4#	Module 4 Mode	DEH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
			DF	DE	DD	DC	DB	DA	D9	D8	
CCON*#	PCA Counter Control	D8H	CF	CR	–	CCF4	CCF3	CCF2	CCF1	CCF0	00x00000B
CH#	PCA Counter High	F9H									00H
CL#	PCA Counter Low	E9H									00H
CMOD#	PCA Counter Mode	D9H	CIDL	WDTE	–	–	–	CPS1	CPS0	ECF	00xxx000B
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt Enable 0	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*	Interrupt Priority	B8H	–	PPC	PT2	PS	PT1	PX1	PT0	PX0	x0000000B
			B7	B6	B5	B4	B3	B2	B1	B0	
IPH#	Interrupt Priority High	B7H	–	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	x0000000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	CEX4	CEX3	CEX2	CEX1	CEX0	ECI	T2EX	T2	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD	FFH
PCON#[1]	Power Control	87H	SMOD1	SMOD0	–	POF	GF1	GF0	PD	IDL	00xxx000B

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
– Reserved bits.
1. Reset value depends on reset source.

Table 1. Special Function Registers (Continued)

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00000000B
RCAP2H#	Timer 2 Capture High	CBH									00H
RCAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	00H
T2MOD#	Timer 2 Mode Control	C9H	–	–	–	–	–	–	T2OE	DCEN	xxxxxx00B
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH									00H
TMOD	Timer Mode	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00H
WDTRST	Watchdog Timer Reset	A6H									

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
– Reserved bits.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. Minimum and maximum high and low times specified in the data sheet must be observed.

This device is configured at the factory to operate using 6 clock periods per machine cycle, referred to in this datasheet as “6 clock mode”. (This yields performance equivalent to twice that of standard 80C51 family devices). It may be optionally configured on commercially-available EPROM programming equipment to operate at 12 clocks per machine cycle, referred to in this datasheet as “12 clock mode”. Once 12 clock mode has been configured, it cannot be changed back to 6 clock mode.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (12 oscillator periods in 6 clock mode, or 24 oscillator periods in 12 clock mode), while the oscillator is running. To ensure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up. Ports 1, 2, and 3 will asynchronously be driven to their reset condition when a voltage above V_{IH1} (min.) is applied to RESET.

The value on the $\overline{EA}$ pin is latched when RST is deasserted and has no further effect.

LOW POWER MODES

Stop Clock Mode

The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power Down mode is suggested.

Idle Mode

In the idle mode (see Table 2), the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode (see Table 2) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to 2.0 V and care must be taken to return V_{CC} to the minimum specified operating voltages before the Power Down Mode is terminated.

Either a hardware reset or external interrupt can be used to exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

POWER OFF FLAG

The Power Off Flag (POF) is set by on-chip circuitry when the V_{CC} level on the P89C51RB2/RC2/RD2 rises from 0 to 5 V. The POF bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after powerdown. The V_{CC} level must remain above 3 V for the POF to remain unaffected by the V_{CC} level.

Design Consideration

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE™ Mode

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems without the device having to be removed from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Programmable Clock-Out

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or
2. to output a 50% duty cycle clock ranging from 122 Hz to 8 MHz at a 16 MHz operating frequency (61 Hz to 4 MHz in 12 clock mode).

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T}$2 (in T2CON) must be cleared and bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{n \times (65536 - \text{RCAP2H, RCAP2L})}$$

n = 2 in 6 clock mode
4 in 12 clock mode

Where (RCAP2H,RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

Table 2. External Pin Status During Idle and Power-Down Mode

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

TIMER 2 OPERATION

Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/$\overline{T}$2* in the special function register T2CON (see Figure 1). Timer 2 has three operating modes: Capture, Auto-reload (up or down counting), and Baud Rate Generator, which are selected by bits in the T2CON as shown in Table 3.

Capture Mode

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then timer 2 is a 16-bit timer or counter (as selected by C/$\overline{T}$2* in T2CON) which, upon overflowing sets bit TF2, the timer 2 overflow bit. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register). If EXEN2= 1, Timer 2 operates as described above, but with the added feature that a 1- to -0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt. The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt). The capture mode is illustrated in Figure 2 (There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or osc/6 pulses (osc/12 in 12 clock mode).).

Auto-Reload Mode (Up or Down Counter)

In the 16-bit auto-reload mode, Timer 2 can be configured (as either a timer or counter [C/$\overline{T}$2* in T2CON]) then programmed to count up or down. The counting direction is determined by bit DCEN (Down Counter Enable) which is located in the T2MOD register (see Figure 3). When reset is applied the DCEN=0 which means Timer 2 will default to counting up. If DCEN bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 4 shows Timer 2 which will count up automatically since DCEN=0. In this mode there are two options selected by bit EXEN2 in T2CON register. If EXEN2=0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

If EXEN2=1, then a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

In Figure 5 DCEN=1 which enables Timer 2 to count up or down. This mode allows pin T2EX to control the direction of count. When a logic 1 is applied at pin T2EX Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

When a logic 0 is applied at pin T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2.

The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

(MSB) (LSB)

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Symbol	Position	Name and Significance
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/$\overline{T2}$	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/6 in 6 clock mode or OSC/12 in 12 clock mode) 1 = External event counter (falling edge triggered).
CP/$\overline{RL2}$	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

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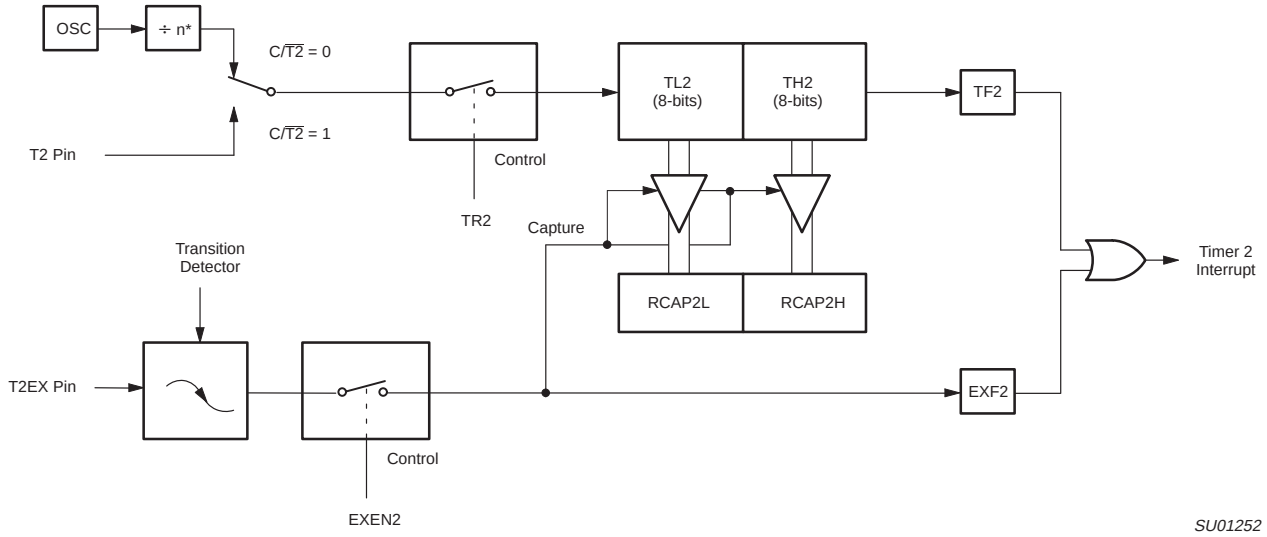
Figure 1. Timer/Counter 2 (T2CON) Control Register

Table 3. Timer 2 Operating Modes

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate generator
X	X	0	(off)



* n = 6 in 6 clock mode, or 12 in 12 clock mode.

Figure 2. Timer 2 in Capture Mode

T2MOD Address = 0C9H Reset Value = XXXX XX00B

Not Bit Addressable

—	—	—	—	—	—	T2OE	DCEN
Bit 7	6	5	4	3	2	1	0

Symbol	Function
—	Not implemented, reserved for future use.*
T2OE	Timer 2 Output Enable bit.
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

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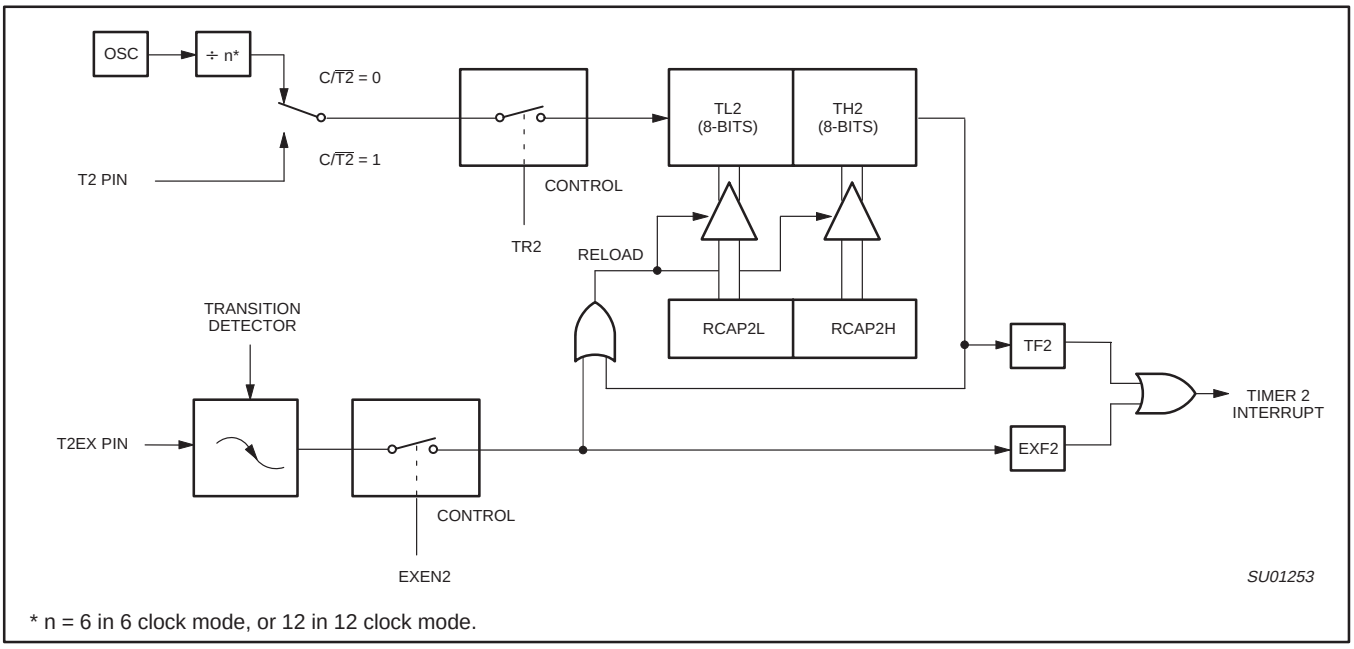
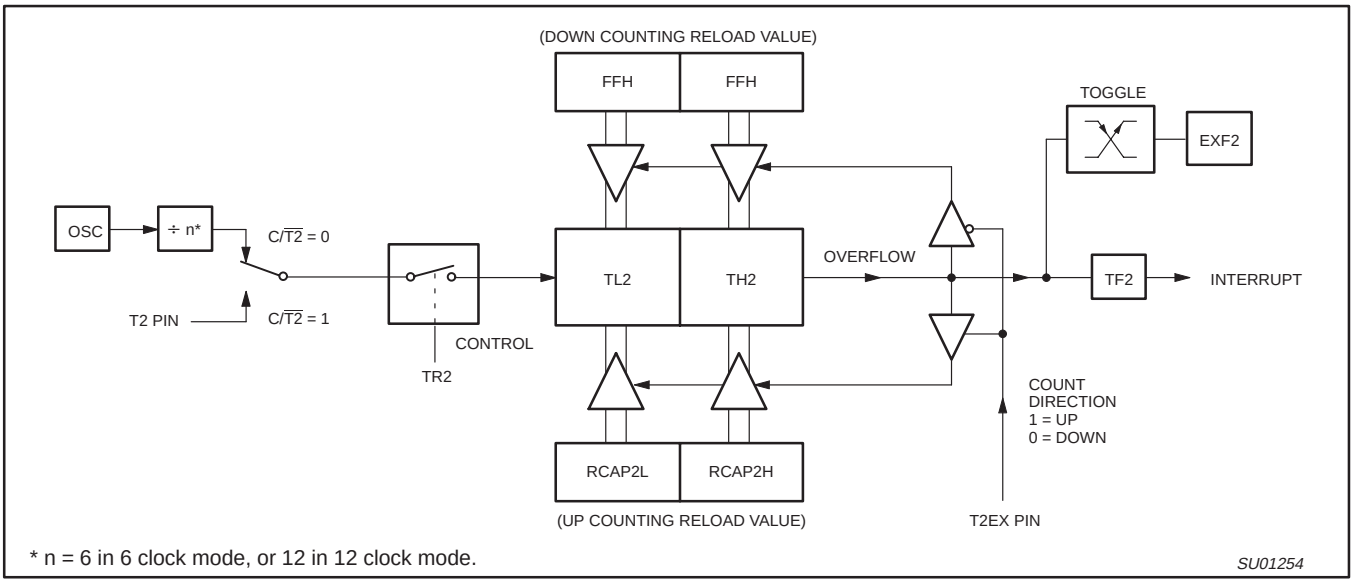
Figure 3. Timer 2 Mode (T2MOD) Control Register



* n = 6 in 6 clock mode, or 12 in 12 clock mode.

Figure 4. Timer 2 in Auto-Reload Mode (DCEN = 0)



* n = 6 in 6 clock mode, or 12 in 12 clock mode.

Figure 5. Timer 2 Auto Reload Mode (DCEN = 1)

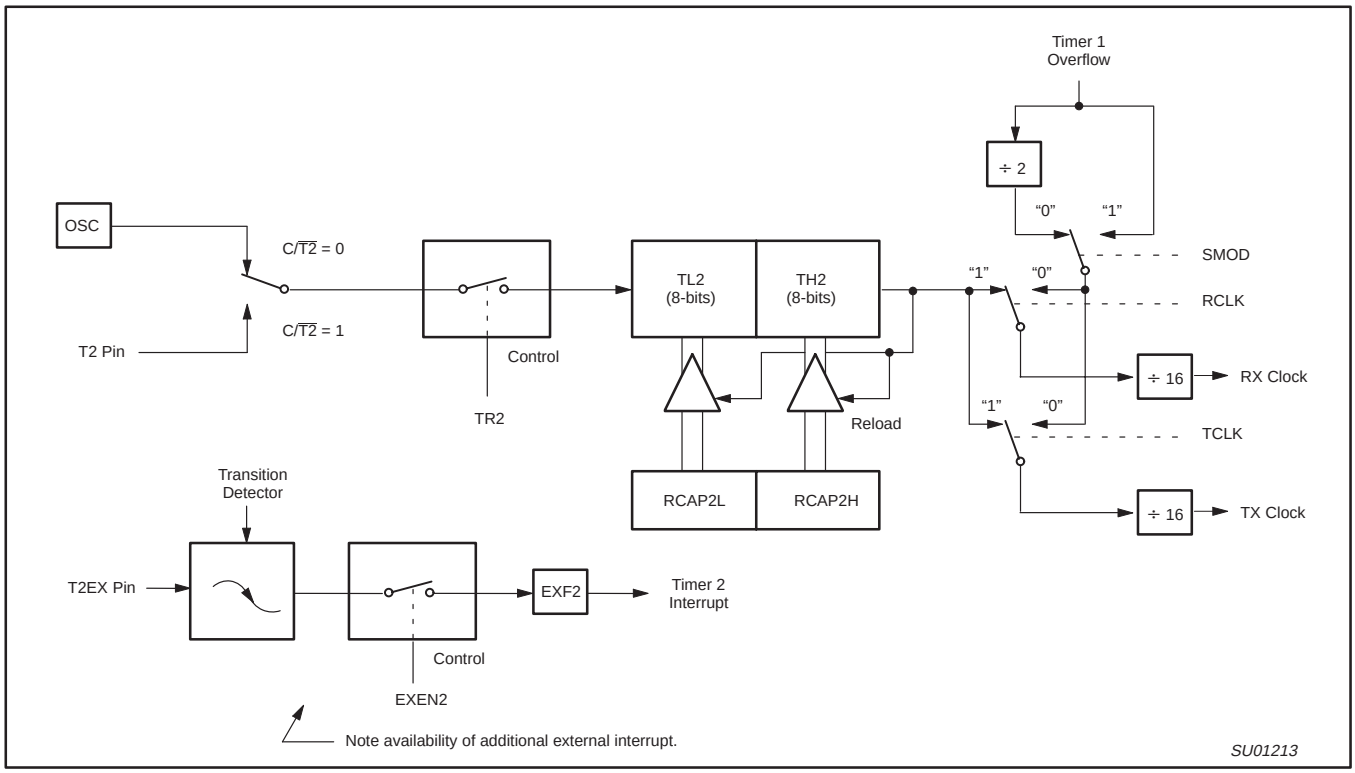


Figure 6. Timer 2 in Baud Rate Generator Mode

Table 4. Timer 2 Generated Commonly Used Baud Rates

Baud Rate		Osc Freq	Timer 2	
12 clock mode	6 clock mode		RCAP2H	RCAP2L
375 k	750 k	12 MHz	FF	FF
9.6 k	19.2 k	12 MHz	FF	D9
2.8 k	5.6 k	12 MHz	FF	B2
2.4 k	4.8 k	12 MHz	FF	64
1.2 k	2.4 k	12 MHz	FE	C8
300	600	12 MHz	FB	1E
110	220	12 MHz	F2	AF
300	600	6 MHz	FD	8F
110	220	6 MHz	F9	57

Baud Rate Generator Mode

Bits TCLK and/or RCLK in T2CON (Table 4) allow the serial port transmit and receive baud rates to be derived from either Timer 1 or Timer 2. When TCLK= 0, Timer 1 is used as the serial port transmit baud rate generator. When TCLK= 1, Timer 2 is used as the serial port transmit baud rate generator. RCLK has the same effect for the serial port receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates – one generated by Timer 1, the other by Timer 2.

Figure 6 shows the Timer 2 in baud rate generation mode. The baud rate generation mode is like the auto-reload mode,in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The timer can be configured for either "timer" or "counter" operation. In many applications, it is configured for "timer" operation (C/$\overline{T}$2*=0). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., $^1/_6$ the oscillator frequency in 6 clock mode, $^1/_{12}$ the oscillator frequency in 12 clock mode). As a baud rate generator, it increments at the oscillator frequency in 6 clock mode ($^{OSC}/_2$ in 12 clock mode). Thus the baud rate formula is as follows:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Oscillator Frequency}}{[\,n^* \times [65536 - (\text{RCAP2H, RCAP2L})]]}$$

* n = 16 in 6 clock mode
32 in 12 clock mode

Where: (RCAP2H, RCAP2L)= The content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 as a baud rate generator mode shown in Figure 6, is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2,TL2). Therefore when Timer 2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. As a baud rate generator, Timer 2 is incremented every state time (osc/2) or asynchronously from pin T2; under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 4 shows commonly used baud rates and how they can be obtained from Timer 2.

Summary of Baud Rate Equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2(P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer 2 is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{f_{OSC}}{[\ n^{*} \times [65536 - (\text{RCAP2H, RCAP2L})]]}$$

* n = 16 in 6 clock mode
32 in 12 clock mode

Where f_{OSC}= Oscillator Frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$\text{RCAP2H, RCAP2L} = 65536 - \left(\frac{f_{OSC}}{n^{*} \times \text{Baud Rate}}\right)$$

Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. see Table 5 for set-up of Timer 2 as a timer. Also see Table 6 for set-up of Timer 2 as a counter.

Table 5. Timer 2 as a Timer

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Table 6. Timer 2 as a Counter

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

NOTES:
1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.

Enhanced UART

The UART operates in all of the usual modes that are described in the first section of *Data Handbook IC20, 80C51-Based 8-Bit Microcontrollers*. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 7). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 8.

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the “Given” address or the “Broadcast” address. The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 9.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to b used and which bits are “don’t care”. The SADEN mask can be logically ANDed with the SADDR to create the “Given” address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR	=	1100 0000
	SADEN	=	1111 1101
	Given	=	1100 00X0
Slave 1	SADDR	=	1100 0000
	SADEN	=	1111 1110
	Given	=	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR	=	1100 0000
	SADEN	=	1111 1001
	Given	=	1100 0XX0
Slave 1	SADDR	=	1110 0000
	SADEN	=	1111 1010
	Given	=	1110 0X0X
Slave 2	SADDR	=	1110 0000
	SADEN	=	1111 1100
	Given	=	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are trended as don’t-cares. In most cases, interpreting the don’t-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are leaded with 0s. This produces a given address of all “don’t cares” as well as a Broadcast address of all “don’t cares”. This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

SCON Address = 98H Reset Value = 0000 0000B

Bit Addressable

	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
Bit:	7	6	5	4	3	2	1	0

(SMOD0 = 0/1)*

Symbol	Function
FE	Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit.
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate**
0	0	0	shift register	f_{OSC}/6 (6 clock mode) or f_{OSC}/12 (12 clock mode)
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	f_{OSC}/32 or f_{OSC}/16 (6 clock mode) or f_{OSC}/64 or f_{OSC}/32 (12 clock mode)
1	1	3	9-bit UART	variable

SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	In modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

NOTE:
*SMOD0 is located at PCON6.
**f_{OSC} = oscillator frequency

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Figure 7. SCON: Serial Port Control Register

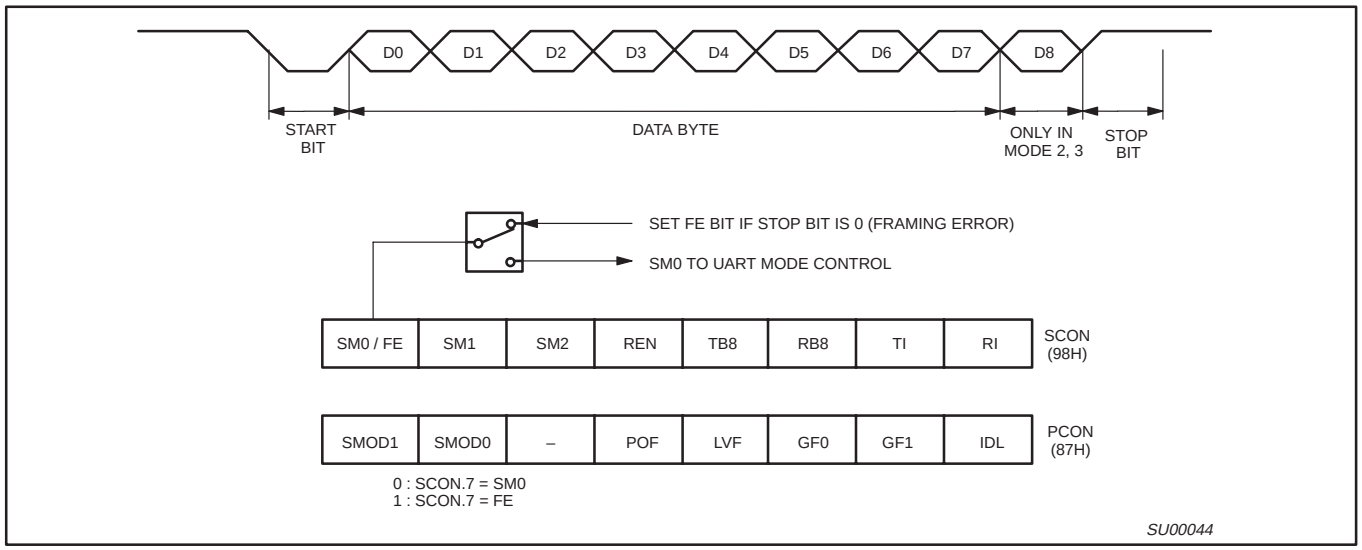

Figure 8. UART Framing Error Detection

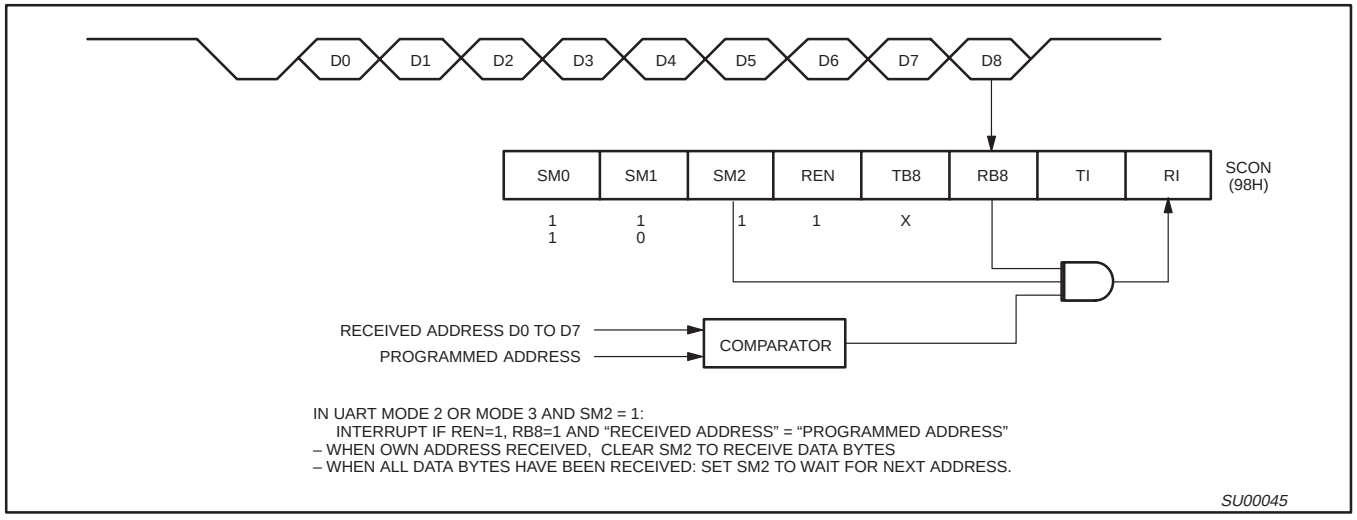

Figure 9. UART Multiprocessor Communication, Automatic Address Recognition

Interrupt Priority Structure

The P89C51RB2/RC2/RD2 has a 7 source four-level interrupt structure (see Table 7).

There are 3 SFRs associated with the four-level interrupt. They are the IE, IP, and IPH. (See Figures 10, 11, and 12.) The IPH (Interrupt Priority High) register makes the four-level interrupt structure possible. The IPH is located at SFR address B7H. The structure of the IPH register and a description of its bits is shown in Figure 12.

The function of the IPH SFR, when combined with the IP SFR, determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH.x	IP.x	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

The priority scheme for servicing the interrupts is the same as that for the 80C51, except there are four interrupt levels rather than two as on the 80C51. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

Table 7. Interrupt Table

SOURCE	POLLING PRIORITY	REQUEST BITS	HARDWARE CLEAR?	VECTOR ADDRESS
X0	1	IE0	N (L)[1] Y (T)[2]	03H
T0	2	TP0	Y	0BH
X1	3	IE1	N (L) Y (T)	13H
T1	4	TF1	Y	1BH
PCA	5	CF, CCFn n = 0–4	N	33H
SP	6	RI, TI	N	23H
T2	7	TF2, EXF2	N	2BH

NOTES:
1. L = Level activated
2. T = Transition activated

	7	6	5	4	3	2	1	0
IE (0A8H)	EA	EC	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables it.

BIT	SYMBOL	FUNCTION
IE.7	EA	Global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit.
IE.6	EC	PCA interrupt enable bit
IE.5	ET2	Timer 2 interrupt enable bit.
IE.4	ES	Serial Port interrupt enable bit.
IE.3	ET1	Timer 1 interrupt enable bit.
IE.2	EX1	External interrupt 1 enable bit.
IE.1	ET0	Timer 0 interrupt enable bit.
IE.0	EX0	External interrupt 0 enable bit.

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Figure 10. IE Registers

	7	6	5	4	3	2	1	0
IP (0B8H)	–	PPC	PT2	PS	PT1	PX1	PT0	PX0

Priority Bit = 1 assigns high priority
Priority Bit = 0 assigns low priority

BIT	SYMBOL	FUNCTION
IP.7	–	–
IP.6	PPC	PCA interrupt priority bit
IP.5	PT2	Timer 2 interrupt priority bit.
IP.4	PS	Serial Port interrupt priority bit.
IP.3	PT1	Timer 1 interrupt priority bit.
IP.2	PX1	External interrupt 1 priority bit.
IP.1	PT0	Timer 0 interrupt priority bit.
IP.0	PX0	External interrupt 0 priority bit.

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Figure 11. IP Registers

	7	6	5	4	3	2	1	0
IPH (B7H)	–	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Priority Bit = 1 assigns higher priority
Priority Bit = 0 assigns lower priority

BIT	SYMBOL	FUNCTION
IPH.7	–	–
IPH.6	PPCH	PCA interrupt priority bit
IPH.5	PT2H	Timer 2 interrupt priority bit high.
IPH.4	PSH	Serial Port interrupt priority bit high.
IPH.3	PT1H	Timer 1 interrupt priority bit high.
IPH.2	PX1H	External interrupt 1 priority bit high.
IPH.1	PT0H	Timer 0 interrupt priority bit high.
IPH.0	PX0H	External interrupt 0 priority bit high.

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Figure 12. IPH Registers

Reduced EMI Mode

The AO bit (AUXR.0) in the AUXR register when set disables the ALE output.

Reduced EMI Mode

AUXR (8EH)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	EXTRAM	AO

AUXR.1 EXTRAM
AUXR.0 AO Turns off ALE output.

Dual DPTR

The dual DPTR structure (see Figure 13) is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 that allows the program code to switch between them.

- New Register Name: AUXR1#
- SFR Address: A2H
- Reset Value: xxxxxxx0B

AUXR1 (A2H)

7	6	5	4	3	2	1	0
–	–	ENBOOT	–	GF2	0	–	DPS

Where:
DPS = AUXR1/bit0 = Switches between DPTR0 and DPTR1.

Select Reg	DPS
DPTR0	0
DPTR1	1

The DPS bit status should be saved by software when switching between DPTR0 and DPTR1.

The GF2 bit is a general purpose user-defined flag. Note that bit 2 is not writable and is always read as a zero. This allows the DPS bit to be quickly toggled simply by executing an INC AUXR1 instruction without affecting the GF2 bit.

The ENBOOT bit determines whether the BOOTROM is enabled or disabled. This bit will automatically be set if the status byte is non zero during reset or $\overline{PSEN}$ is pulled low, ALE floats high, and EA > V_{IH} on the falling edge of reset. Otherwise, this bit will be cleared during reset.

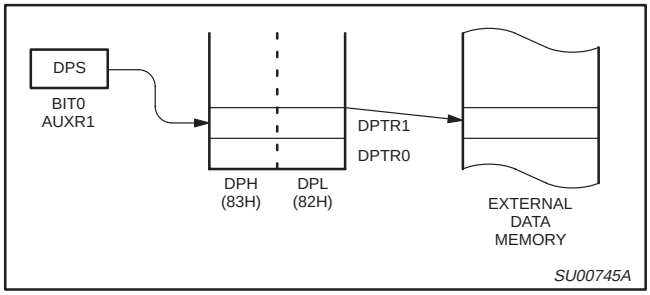

Figure 13.

DPTR Instructions

The instructions that refer to DPTR refer to the data pointer that is currently selected using the AUXR1/bit 0 register. The six instructions that use the DPTR are as follows:

INC DPTR	Increments the data pointer by 1
MOV DPTR, #data16	Loads the DPTR with a 16-bit constant
MOV A, @ A+DPTR	Move code byte relative to DPTR to ACC
MOVX A, @ DPTR	Move external RAM (16-bit address) to ACC
MOVX @ DPTR , A	Move ACC to external RAM (16-bit address)
JMP @ A + DPTR	Jump indirect relative to DPTR

The data pointer can be accessed on a byte-by-byte basis by specifying the low or high byte in an instruction which accesses the SFRs. See *Application Note AN458* for more details.

Programmable Counter Array (PCA)

The Programmable Counter Array available on the 89C51RB2/RC2/RD2 is a special 16-bit Timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3(CEX0), module 1 to P1.4(CEX1), etc. The basic PCA configuration is shown in Figure 14.

The PCA timer is a common time base for all five modules and can be programmed to run at: 1/6 the oscillator frequency, 1/2 the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P1.2). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see Figure 17):

CPS1	CPS0	PCA Timer Count Source
0	0	1/6 oscillator frequency (6 clock mode); 1/12 oscillator frequency (12 clock mode)
0	1	1/2 oscillator frequency (6 clock mode); 1/4 oscillator frequency (12 clock mode)
1	0	Timer 0 overflow
1	1	External Input at ECI pin

In the CMOD SFR are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during idle mode, WDTE which enables or disables the watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows. These functions are shown in Figure 15.

The watchdog timer function is implemented in module 4 (see Figure 24).

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (refer to Figure 18). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set, The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software. The PCA interrupt system shown in Figure 16.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (see Figure 19). The registers contain the bits that control the mode that each module will operate in. The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function. Figure 20 shows the CCAPMn settings for the various PCA functions.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

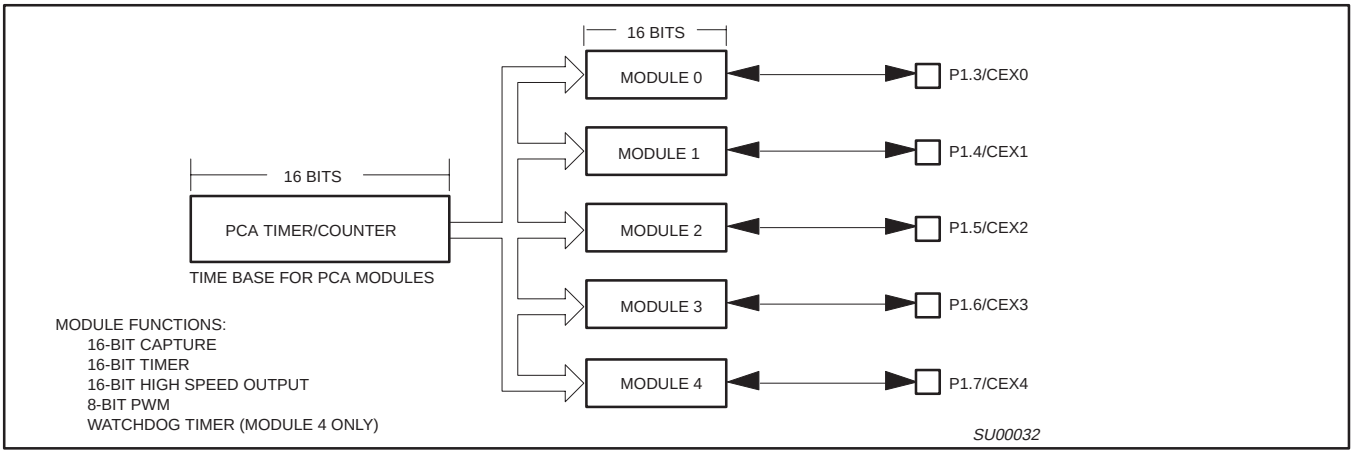

Figure 14. Programmable Counter Array (PCA)

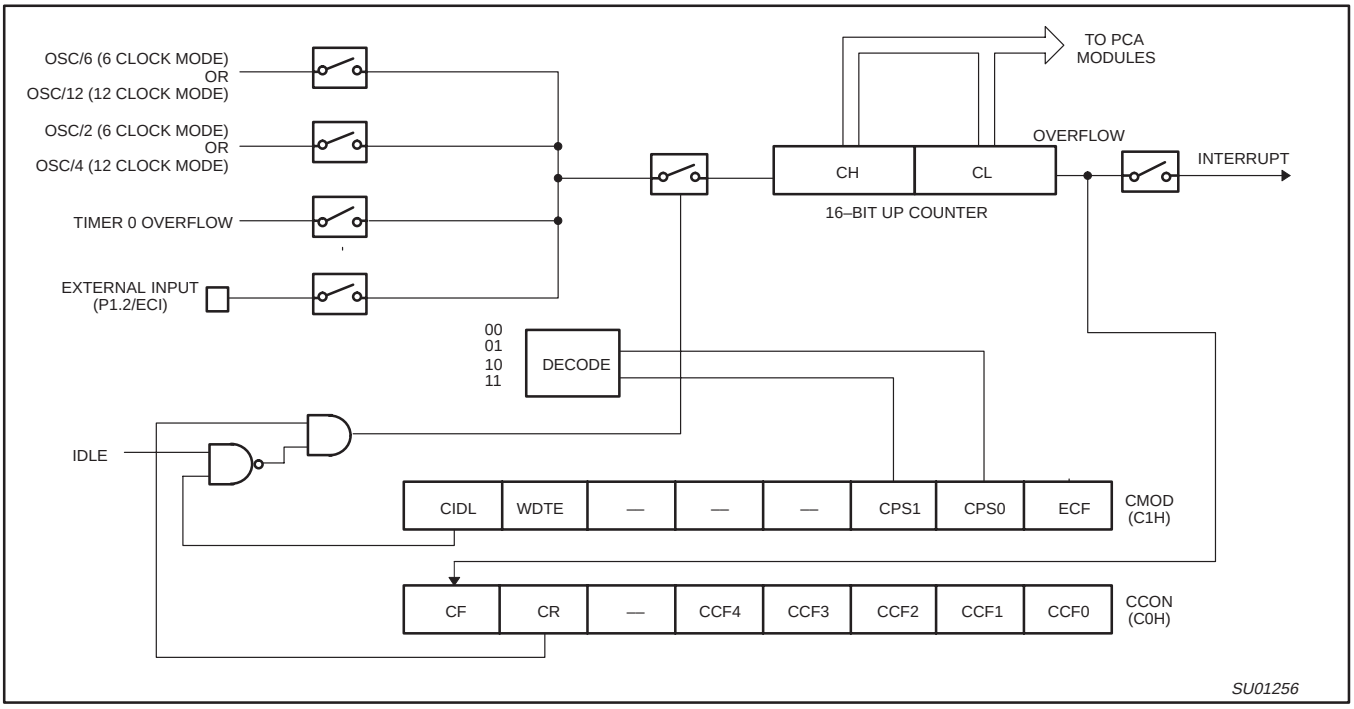

Figure 15. PCA Timer/Counter

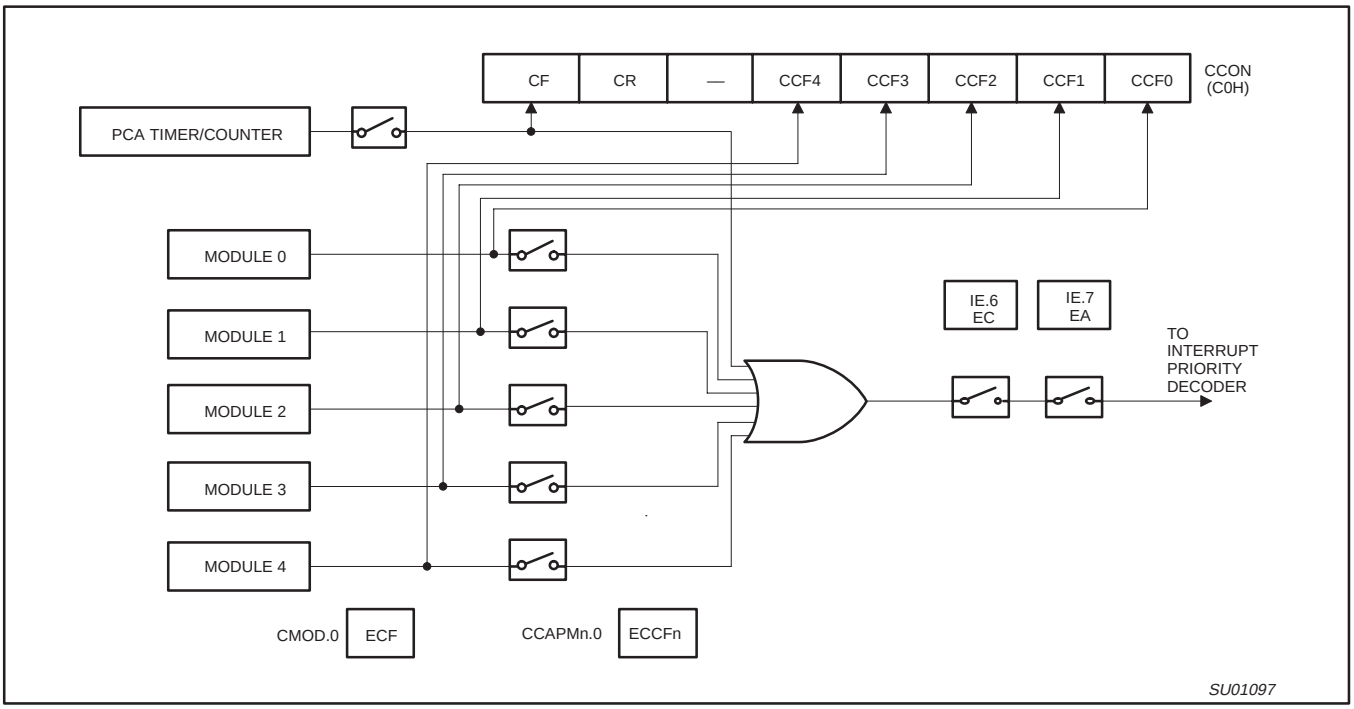

Figure 16. PCA Interrupt System

CMOD Address = D9H Reset Value = 00XX X000B

	CIDL	WDTE	–	–	–	CPS1	CPS0	ECF
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
CIDL	Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.
WDTE	Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.
–	Not implemented, reserved for future use.*
CPS1	PCA Count Pulse Select bit 1.
CPS0	PCA Count Pulse Select bit 0.

CPS1	CPS0	Selected PCA Input**	
0	0	0	Internal clock, f_{OSC}/6 in 6 clock mode (f_{OSC}/12 in 12 clock mode)
0	1	1	Internal clock, f_{OSC}/2 in 6 clock mode (f_{OSC}/4 in 12 clock mode)
1	0	2	Timer 0 overflow
1	1	3	External clock at ECI/P1.2 pin (max. rate = f_{OSC}/4 in 6 clock mode, f_{OCS}/8 in 12 clock mode)

ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.

NOTE:
* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.
** f_{OSC} = oscillator frequency

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Figure 17. CMOD: PCA Counter Mode Register

CCON Address = D8H Reset Value = 00X0 0000B

Bit Addressable

	CF	CR	–	CCF4	CCF3	CCF2	CCF1	CCF0
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
CR	PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
–	Not implemented, reserved for future use*.
CCF4	PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF3	PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF2	PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF1	PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
CCF0	PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

NOTE:
* User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

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Figure 18. CCON: PCA Counter Control Register

CCAPMn Address CCAPM0 0DAH
CCAPM1 0DBH
CCAPM2 0DCH
CCAPM3 0DDH
CCAPM4 0DEH

Reset Value = X000 0000B

Not Bit Addressable

	–	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
–	Not implemented, reserved for future use*.
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.

NOTE:
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

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Figure 19. CCAPMn: PCA Modules Compare/Capture Registers

–	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	MODULE FUNCTION
X	0	0	0	0	0	0	0	No operation
X	X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
X	1	0	0	1	0	0	X	16-bit Software Timer
X	1	0	0	1	1	0	X	16-bit High Speed Output
X	1	0	0	0	0	1	0	8-bit PWM
X	1	0	0	1	X	0	X	Watchdog Timer

Figure 20. PCA Module Modes (CCAPMn Register)

PCA Capture Mode
To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated. Refer to Figure 21.

16-bit Software Timer Mode
The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (see Figure 22).

High Speed Output Mode
In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (see Figure 23).

Pulse Width Modulator Mode
All of the PCA modules can be used as PWM outputs. Figure 24 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. the allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

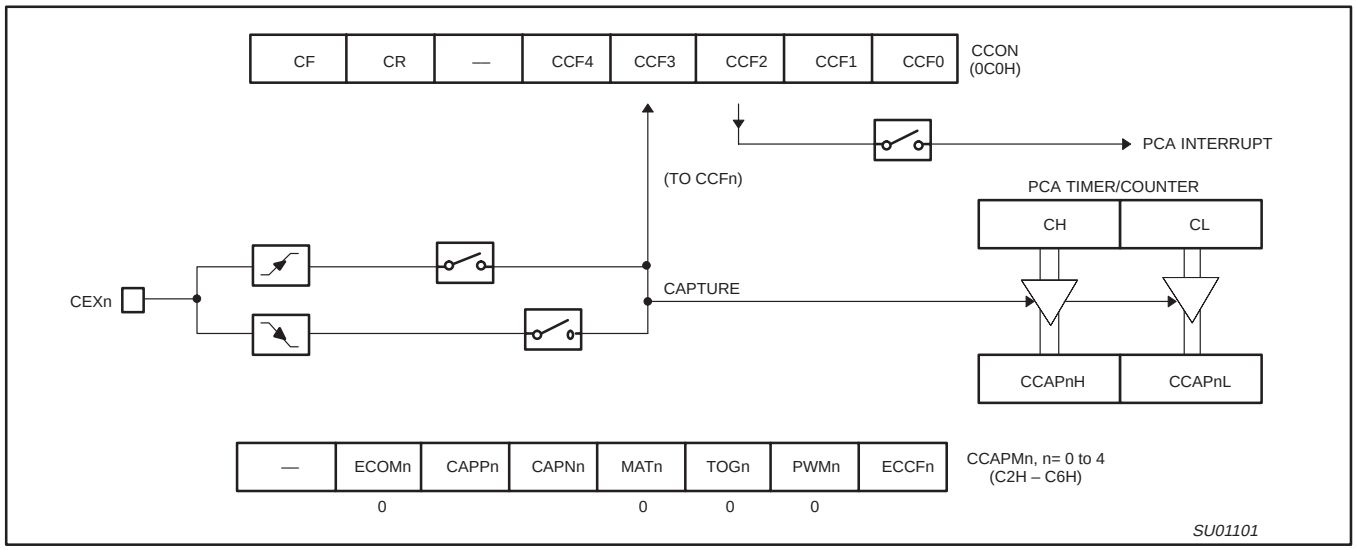

Figure 21. PCA Capture Mode

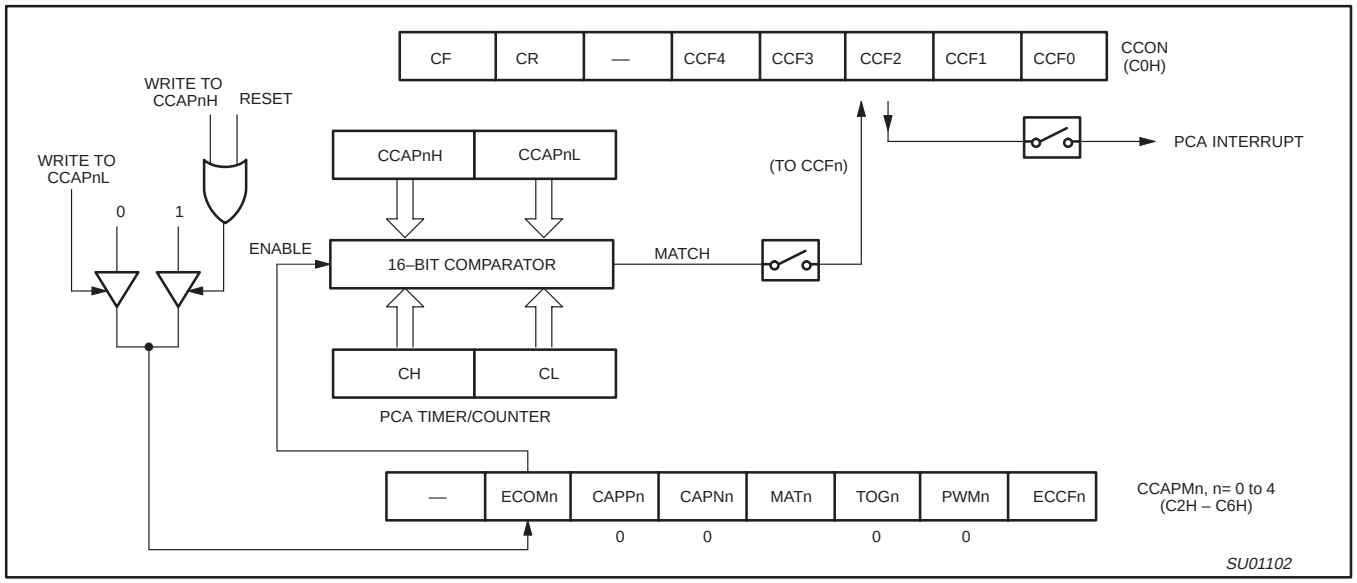

Figure 22. PCA Compare Mode

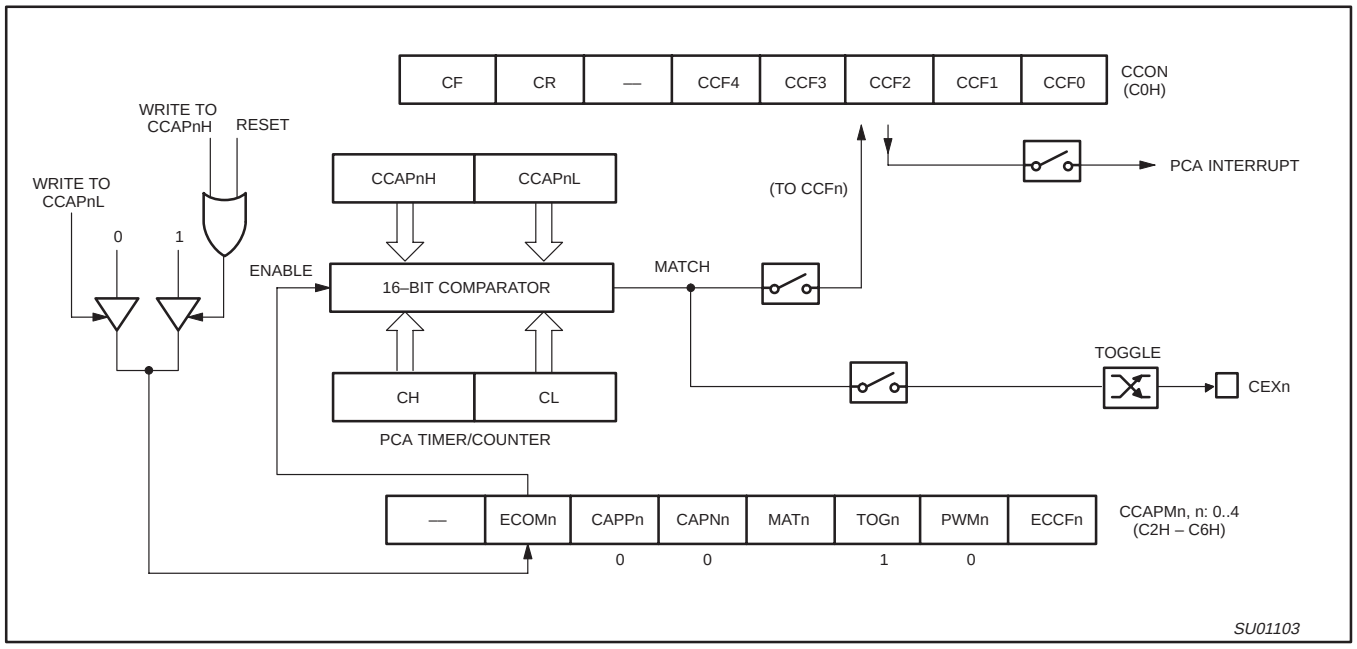

Figure 23. PCA High Speed Output Mode

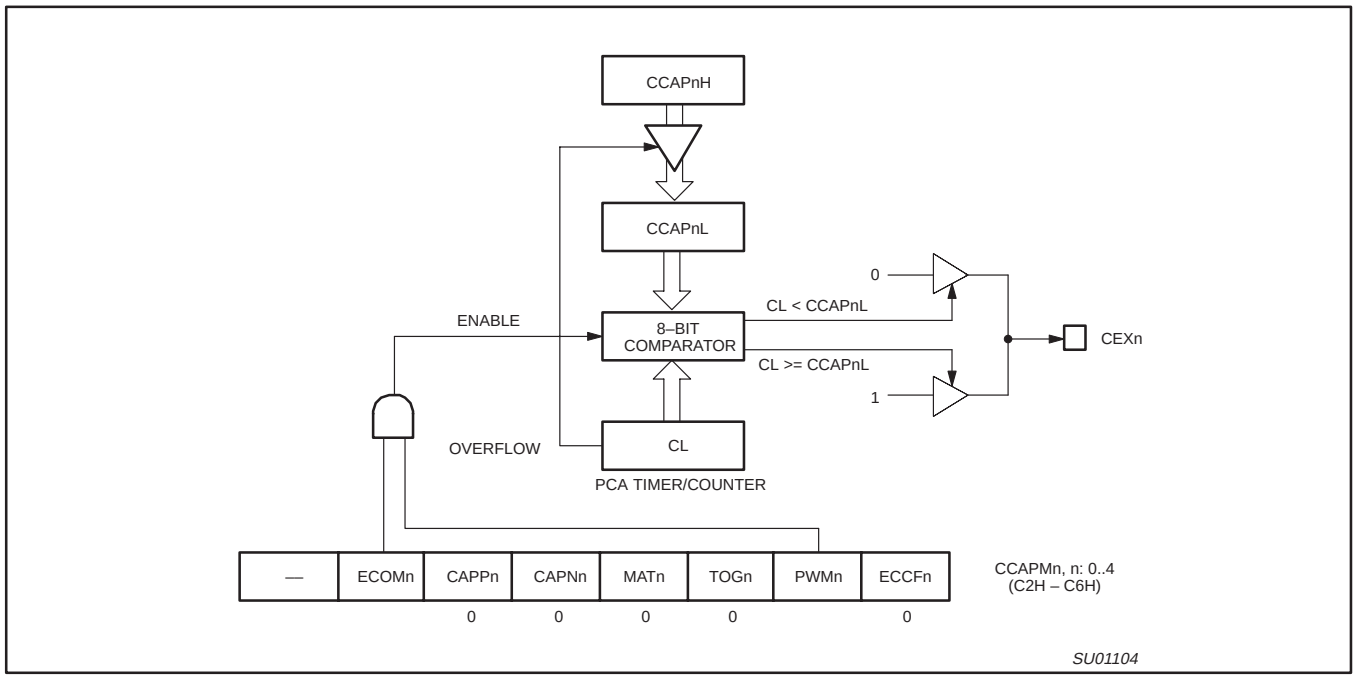

Figure 24. PCA PWM Mode

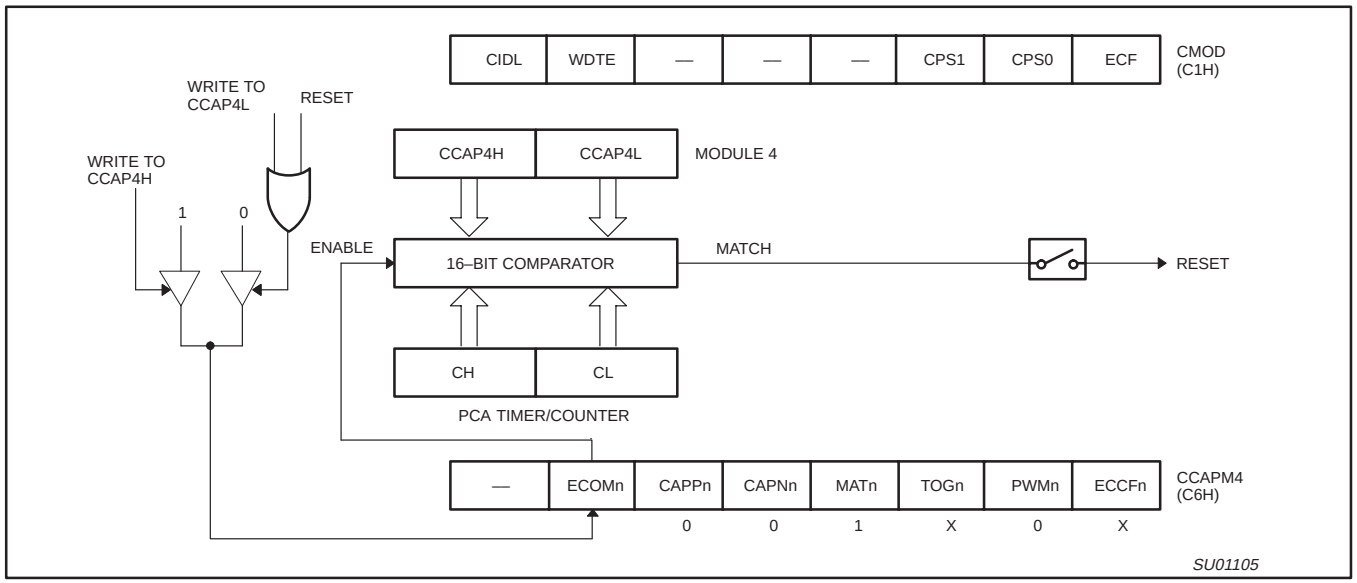

Figure 25. PCA Watchdog Timer m(Module 4 only)

PCA Watchdog Timer

An on-board watchdog timer is available with the PCA to improve the reliability of the system without increasing chip count. Watchdog timers are useful for systems that are susceptible to noise, power glitches, or electrostatic discharge. Module 4 is the only PCA module that can be programmed as a watchdog. However, this module can still be used for other modes if the watchdog is not needed.

Figure 25 shows a diagram of how the watchdog works. The user pre-loads a 16-bit value in the compare registers. Just like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match is allowed to occur, an internal reset will be generated. This will not cause the RST pin to be driven high.

In order to hold off the reset, the user has three options:

1. periodically change the compare value so it will never match the PCA timer,
2. periodically change the PCA timer value so it will never match the compare values, or
3. disable the watchdog by clearing the WDTE bit before a match occurs and then re-enable it.

The first two options are more reliable because the watchdog timer is never disabled as in option #3. If the program counter ever goes astray, a match will eventually occur and cause an internal reset. The second option is also not recommended if other PCA modules are being used. Remember, the PCA timer is the time base for **all** modules; changing the time base for other modules would not be a good idea. Thus, in most applications the first solution is the best option.

Figure 26 shows the code for initializing the watchdog timer. Module 4 can be configured in either compare mode, and the WDTE bit in CMOD must also be set. The user's software then must periodically change (CCAP4H,CCAP4L) to keep a match from occurring with the PCA timer (CH,CL). This code is given in the WATCHDOG routine in Figure 26.

This routine should not be part of an interrupt service routine, because if the program counter goes astray and gets stuck in an infinite loop, interrupts will still be serviced and the watchdog will keep getting reset. Thus, the purpose of the watchdog would be defeated. Instead, call this subroutine from the main program within 2^{16} count of the PCA timer.

```
INIT_WATCHDOG:
   MOV CCAPM4, #4CH         ; Module 4 in compare mode
   MOV CCAP4L, #0FFH        ; Write to low byte first
   MOV CCAP4H, #0FFH        ; Before PCA timer counts up to
                            ; FFFF Hex, these compare values
                            ; must be changed
   ORL CMOD, #40H           ; Set the WDTE bit to enable the
                            ; watchdog timer without changing
                            ; the other bits in CMOD
;
;*******************************************************************
;
; Main program goes here, but CALL WATCHDOG periodically.
;
;*******************************************************************
;
WATCHDOG:
   CLR EA                   ; Hold off interrupts
   MOV CCAP4L, #00          ; Next compare value is within
   MOV CCAP4H, CH           ; 255 counts of the current PCA
   SETB EA                  ; timer value
   RET
```

Figure 26. PCA Watchdog Timer Initialization Code

Expanded Data RAM Addressing

The P89C51RB2/RC2/RD2 has internal data memory that is mapped into four separate segments: the lower 128 bytes of RAM, upper 128 bytes of RAM, 128 bytes Special Function Register (SFR), and 256 bytes expanded RAM (ERAM) (768 bytes for the RD2).

The four segments are:

1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
4. The 256/768-bytes expanded RAM (ERAM, 00H – 1FFH/2FFH) are indirectly accessed by move external instruction, MOVX, and with the EXTRAM bit cleared, see Figure 27.

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction. Instructions that use direct addressing access SFR space. For example:

MOV 0A0H,#data

accesses the SFR at location 0A0H (which is P2). Instructions that use indirect addressing access the Upper 128 bytes of data RAM.

For example:

MOV @R0,#data

where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

The ERAM can be accessed by indirect addressing, with EXTRAM bit cleared and MOVX instructions. This part of memory is physically located on-chip, logically occupies the first 7936-bytes of external data memory.

With EXTRAM = 0, the ERAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. An access to ERAM will not affect ports P0, P3.6 (WR#) and P3.7 (RD#). P2 SFR is output during external addressing. For example, with EXTRAM = 0,

MOVX @R0,#data

where R0 contains 0A0H, access the ERAM at address 0A0H rather than external memory. An access to external data memory locations higher than the ERAM will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals. Refer to Figure 28.

With EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @ Ri will provide an 8-bit address multiplexed with data on Port 0 and any output port pins can be used to output higher order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a 16-bit address. Port 2 outputs the high-order eight address bits (the contents of DPH) while Port 0 multiplexes the low-order eight address bits (DPL) with data. MOVX @Ri and MOVX @DPTR will generate either read or write signals on P3.6 ($\overline{WR}$) and P3.7 ($\overline{RD}$).

The stack pointer (SP) may be located anywhere in the 256 bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the ERAM.

AUXR Address = 8EH — Reset Value = xxxx xx00B

Not Bit Addressable

	—	—	—	—	—	—	**EXTRAM**	**AO**
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
AO	Disable/Enable ALE
	AO **Operating Mode**
	0 ALE is emitted at a constant rate of $^1/_3$ the oscillator frequency (6 clock mode; $^1/_6$ f_{OSC} in 12 clock mode).
	1 ALE is active only during a MOVX or MOVC instruction.
EXTRAM	Internal/External RAM access using MOVX @Ri/@DPTR
	EXTRAM **Operating Mode**
	0 Internal ERAM access using MOVX @Ri/@DPTR
	1 External data memory access.
—	Not implemented, reserved for future use*.

NOTE:
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

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Figure 27. AUXR: Auxiliary Register

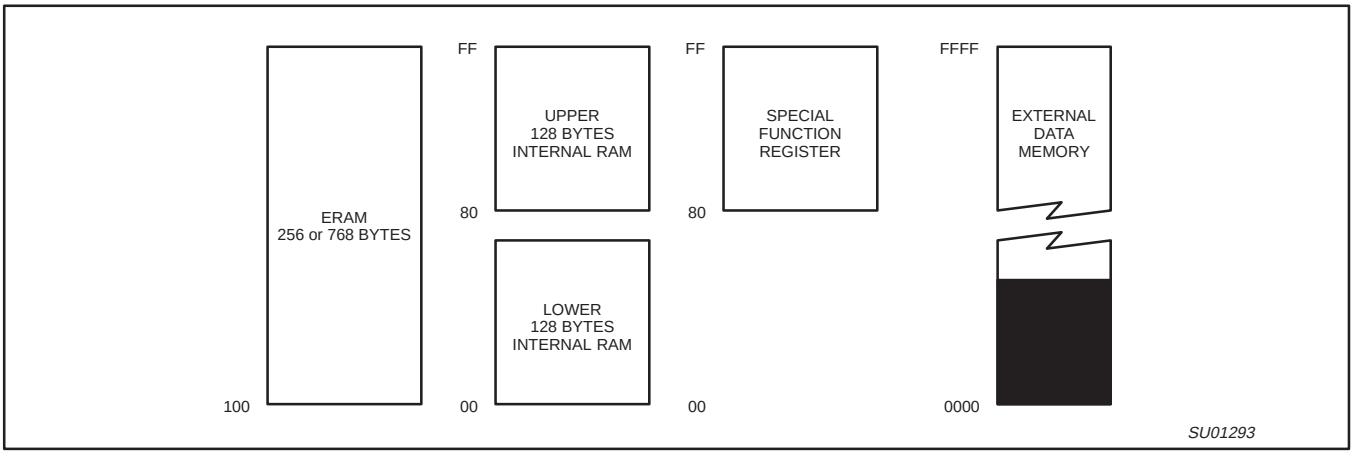


Figure 28. Internal and External Data Memory Address Space with EXTRAM = 0

HARDWARE WATCHDOG TIMER (ONE-TIME ENABLED WITH RESET-OUT FOR P89C51RB2/RC2/RD2)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer reset (WDTRST) SFR. The WDT is disabled at reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output reset HIGH pulse at the RST-pin (see the note below).

Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT, the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the reset pin (see note below). The RESET pulse duration is $98 \times T_{OSC}$ (6 clock mode; 196 in 12 clock mode), where $T_{OSC} = 1/f_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or –40 to +85	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C; V_{CC} = 5 V ± 10% or –40°C to +85°C; 5 V ±5%; V_{SS} = 0 V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
V_{IL}	Input low voltage	4.5 V < V_{CC} < 5.5 V	–0.5		$0.2V_{CC}$–0.1	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, $\overline{EA}$)		$0.2V_{CC}$+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{CC}$		V_{CC}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, 3[8]	V_{CC} = 4.5 V I_{OL} = 1.6 mA[2]			0.4	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$ [7, 8]	V_{CC} = 4.5 V I_{OL} = 3.2 mA[2]			0.45	V
V_{OH}	Output high voltage, ports 1, 2, 3 [3]	V_{CC} = 4.5 V I_{OH} = –30 µA	V_{CC} – 0.7			V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE[9], $\overline{PSEN}$[3]	V_{CC} = 4.5 V I_{OH} = –3.2 mA	V_{CC} – 0.7			V
I_{IL}	Logical 0 input current, ports 1, 2, 3	V_{IN} = 0.4 V	–1		–75	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3[6]	V_{IN} = 2.0 V See Note 4			–650	µA
I_{LI}	Input leakage current, port 0	0.45 < V_{IN} < V_{CC} – 0.3			±10	µA
I_{CC}	Power supply current (see Figure 36): Active mode (see Note 5) Idle mode (see Note 5) Power-down mode or clock stopped (see Figure 42 for conditions) Programming and erase mode	See Note 5 T_{amb} = 0°C to 70°C T_{amb} = –40°C to +85°C f_{osc} = 20 MHz		 < 1 60	 40 50 	 µA µA mA
R_{RST}	Internal reset pull-down resistor		40		225	kΩ
C_{IO}	Pin capacitance[10] (except $\overline{EA}$)				15	pF

NOTES:

1. Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.
2. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
3. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the V_{CC}–0.7 specification when the address bits are stabilizing.
4. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.
5. See Figures 39 through 42 for I_{CC} test conditions and Figure 36 for I_{CC} vs Freq.
   Active mode: $I_{CC(MAX)}$ = (2.8 × FREQ. + 8)mA for all devices, in 6 clock mode; (1.4 × FREQ. + 8)mA in 12 clock mode.
   Idle mode: $I_{CC(MAX)}$ = (1.2 × FREQ. +1.0)mA in 6 clock mode; (0.6 × FREQ. +1.0)mA in 12 clock mode.
6. This value applies to T_{amb} = 0°C to +70°C.
7. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.
8. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15 mA (*NOTE: This is 85°C specification.)
   Maximum I_{OL} per 8-bit port: 26 mA
   Maximum total I_{OL} for all outputs: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
9. ALE is tested to V_{OH1}, except when ALE is off then V_{OH} is the voltage specification.
10. Pin capacitance is characterized but not tested. Pin capacitance is less than 25 pF. Pin capacitance of ceramic package is less than 15 pF (except $\overline{EA}$ is 25 pF).

AC ELECTRICAL CHARACTERISTICS (6 CLOCK MODE)

T_{amb} = 0°C to +70°C; V_{CC} = 5 V ± 10% or –40°C to +85°C, V_{CC} = 5 V ±5%, V_{SS} = 0V[1, 2, 3]

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK[4]		20 MHz CLOCK[4]		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	29	Oscillator frequency	0	20	0	20	MHz
t_{LHLL}	29	ALE pulse width	t_{CLCL}–40		10		ns
t_{AVLL}	29	Address valid to ALE low	$0.5t_{CLCL}$–20		5		ns
t_{LLAX}	29	Address hold after ALE low	$0.5t_{CLCL}$–20		5		ns
t_{LLIV}	29	ALE low to valid instruction in		$2t_{CLCL}$–65		35	ns
t_{LLPL}	29	ALE low to $\overline{PSEN}$ low	$0.5t_{CLCL}$–20		5		ns
t_{PLPH}	29	$\overline{PSEN}$ pulse width	$1.5t_{CLCL}$–45		30		ns
t_{PLIV}	29	$\overline{PSEN}$ low to valid instruction in		$1.5t_{CLCL}$–60		15	ns
t_{PXIX}	29	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	29	Input instruction float after $\overline{PSEN}$		$0.5t_{CLCL}$–20		5	ns
t_{AVIV}	29	Address to valid instruction in		$2.5t_{CLCL}$–80		45	ns
t_{PLAZ}	29	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory							
t_{RLRH}	30, 31	$\overline{RD}$ pulse width	$3t_{CLCL}$–100		50		ns
t_{WLWH}	30, 31	$\overline{WR}$ pulse width	$3t_{CLCL}$–100		50		ns
t_{RLDV}	30, 31	$\overline{RD}$ low to valid data in		$2.5t_{CLCL}$–90		35	ns
t_{RHDX}	30, 31	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	30, 31	Data float after $\overline{RD}$		t_{CLCL}–20		5	ns
t_{LLDV}	30, 31	ALE low to valid data in		$4t_{CLCL}$–150		50	ns
t_{AVDV}	30, 31	Address to valid data in		$4.5t_{CLCL}$–165		60	ns
t_{LLWL}	30, 31	ALE low to $\overline{RD}$ or $\overline{WR}$ low	$1.5t_{CLCL}$–50	$1.5t_{CLCL}$+50	25	125	ns
t_{AVWL}	30, 31	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	$2t_{CLCL}$–75		25		ns
t_{QVWX}	30, 31	Data valid to $\overline{WR}$ transition	$0.5t_{CLCL}$–25		0		ns
t_{WHQX}	30, 31	Data hold after $\overline{WR}$	$0.5t_{CLCL}$–20		5		ns
t_{QVWH}	31	Data valid to $\overline{WR}$ high	$3.5t_{CLCL}$–130		45		ns
t_{RLAZ}	30, 31	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	30, 31	$\overline{RD}$ or $\overline{WR}$ high to ALE high	$0.5t_{CLCL}$–20	$0.5t_{CLCL}$+20	5	45	ns
External Clock							
t_{CHCX}	33	High time	20	t_{CLCL}–t_{CLCX}			ns
t_{CLCX}	33	Low time	20	t_{CLCL}–t_{CHCX}			ns
t_{CLCH}	33	Rise time		5			ns
t_{CHCL}	33	Fall time		5			ns
Shift Register							
t_{XLXL}	32	Serial port clock cycle time	$6t_{CLCL}$		300		ns
t_{QVXH}	32	Output data setup to clock rising edge	$5t_{CLCL}$–133		117		ns
t_{XHQX}	32	Output data hold after clock rising edge	t_{CLCL}–30		20		ns
t_{XHDX}	32	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	32	Clock rising edge to input data valid		$5t_{CLCL}$–133		117	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.
3. Interfacing the microcontroller to devices with float times up to 45 ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
4. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

AC ELECTRICAL CHARACTERISTICS (12 CLOCK MODE)

T_{amb} = 0°C to +70°C; VCC = 5 V ± 10% or –40°C to +85°C, V_{CC} = 5 V ±5%, V_{SS} = 0 V[1, 2, 3]

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK[4]		33 MHz CLOCK[4]		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	29	Oscillator frequency	0	33	0	33	MHz
t_{LHLL}	29	ALE pulse width	$2t_{CLCL}$–40		21		ns
t_{AVLL}	29	Address valid to ALE low	t_{CLCL}–25		5		ns
t_{LLAX}	29	Address hold after ALE low	t_{CLCL}–25		5		ns
t_{LLIV}	29	ALE low to valid instruction in		$4t_{CLCL}$–65		55	ns
t_{LLPL}	29	ALE low to $\overline{PSEN}$ low	t_{CLCL}–25		5		ns
t_{PLPH}	29	$\overline{PSEN}$ pulse width	$3t_{CLCL}$–45		45		ns
t_{PLIV}	29	$\overline{PSEN}$ low to valid instruction in		$3t_{CLCL}$–60		30	ns
t_{PXIX}	29	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	29	Input instruction float after $\overline{PSEN}$		t_{CLCL}–25		5	ns
t_{AVIV}	29	Address to valid instruction in		$5t_{CLCL}$–80		70	ns
t_{PLAZ}	29	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory							
t_{RLRH}	30, 31	$\overline{RD}$ pulse width	$6t_{CLCL}$–100		82		ns
t_{WLWH}	30, 31	$\overline{WR}$ pulse width	$6t_{CLCL}$–100		82		ns
t_{RLDV}	30, 31	$\overline{RD}$ low to valid data in		$5t_{CLCL}$–90		60	ns
t_{RHDX}	30, 31	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	30, 31	Data float after $\overline{RD}$		$2t_{CLCL}$–28		32	ns
t_{LLDV}	30, 31	ALE low to valid data in		$8t_{CLCL}$–150		90	ns
t_{AVDV}	30, 31	Address to valid data in		$9t_{CLCL}$–165		105	ns
t_{LLWL}	30, 31	ALE low to $\overline{RD}$ or $\overline{WR}$ low	$3t_{CLCL}$–50	$3t_{CLCL}$+50	40	140	ns
t_{AVWL}	30, 31	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	$4t_{CLCL}$–75		45		ns
t_{QVWX}	30, 31	Data valid to $\overline{WR}$ transition	t_{CLCL}–30		0		ns
t_{WHQX}	30, 31	Data hold after $\overline{WR}$	t_{CLCL}–25		5		ns
t_{QVWH}	31	Data valid to $\overline{WR}$ high	$7t_{CLCL}$–130		80		ns
t_{RLAZ}	30, 31	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	30, 31	$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{CLCL}–25	t_{CLCL}+25	5	55	ns
External Clock							
t_{CHCX}	33	High time	17	t_{CLCL}–t_{CLCX}			ns
t_{CLCX}	33	Low time	17	t_{CLCL}–t_{CHCX}			ns
t_{CLCH}	33	Rise time		5			ns
t_{CHCL}	33	Fall time		5			ns
Shift Register							
t_{XLXL}	32	Serial port clock cycle time	$12t_{CLCL}$		360		ns
t_{QVXH}	32	Output data setup to clock rising edge	$10t_{CLCL}$–133		167		ns
t_{XHQX}	32	Output data hold after clock rising edge	$2t_{CLCL}$–80		50		ns
t_{XHDX}	32	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	32	Clock rising edge to input data valid		$10t_{CLCL}$–133		167	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.
3. Interfacing the microcontroller to devices with float times up to 45 ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.
4. Parts are tested to 3.5 MHz, but guaranteed to operate down to 0 Hz.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{PSEN}$
Q – Output data
R – $\overline{RD}$ signal
t – Time
V – Valid
W – $\overline{WR}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} = Time for ALE low to $\overline{PSEN}$ low.

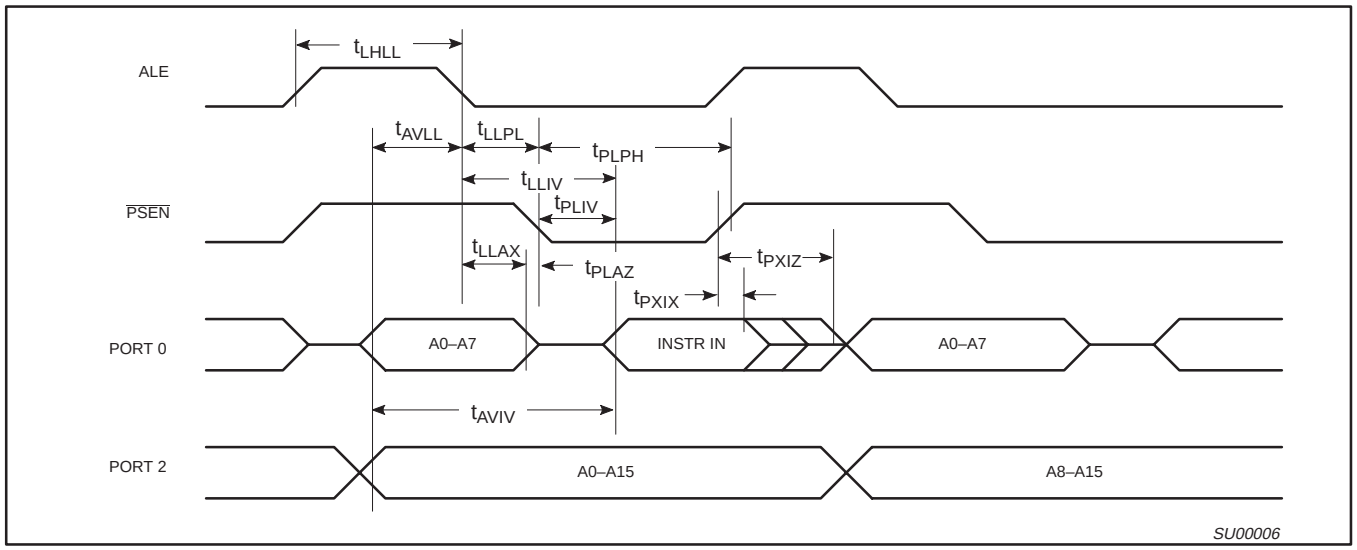


Figure 29. External Program Memory Read Cycle

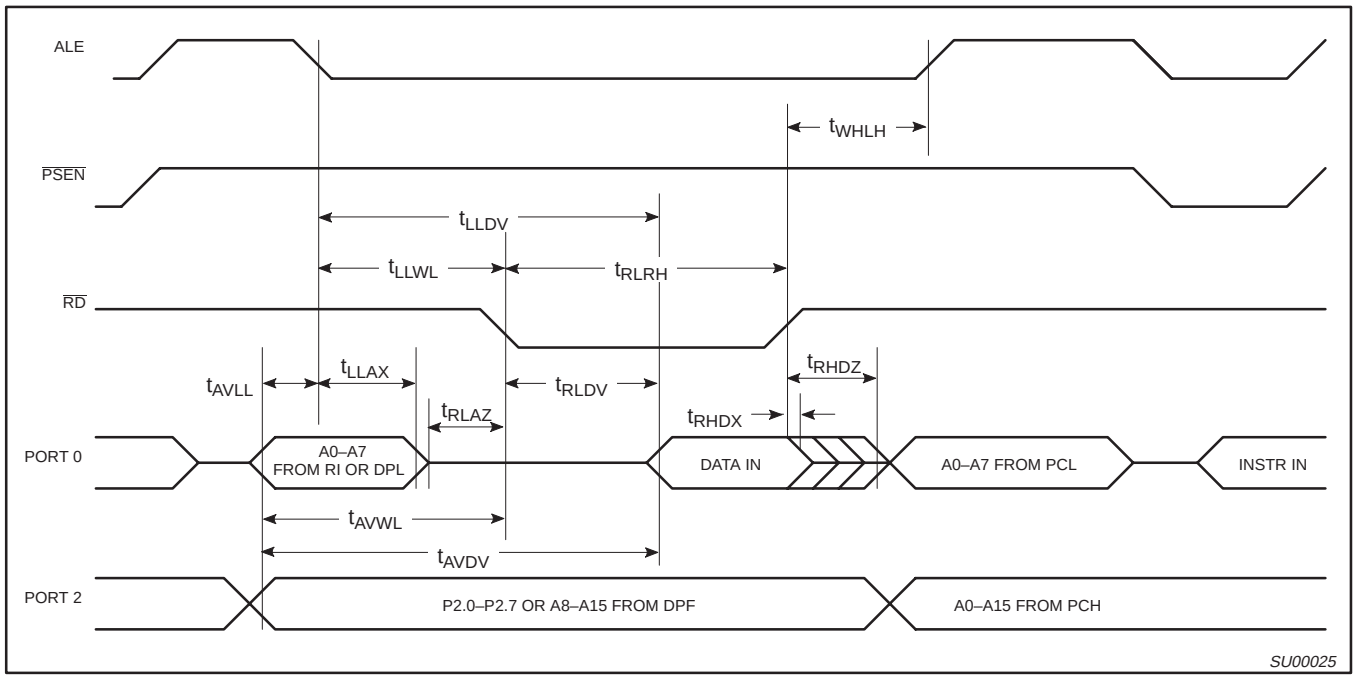


Figure 30. External Data Memory Read Cycle

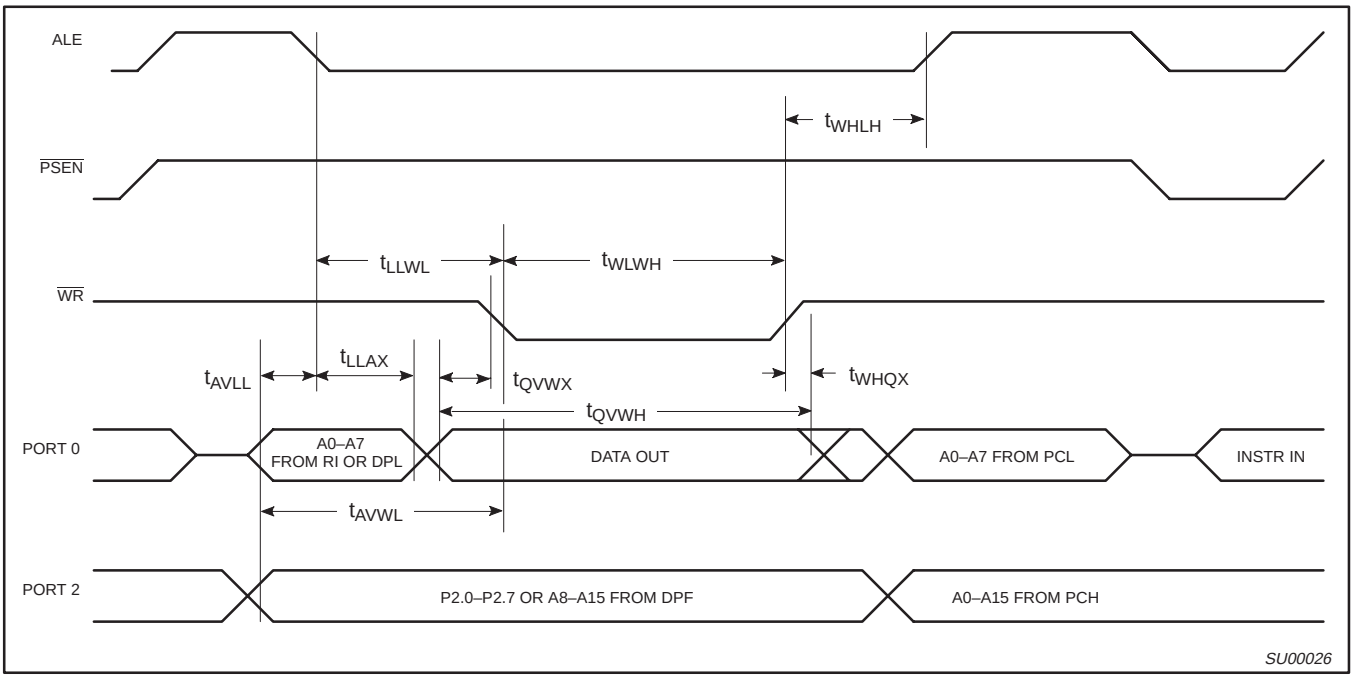


Figure 31. External Data Memory Write Cycle

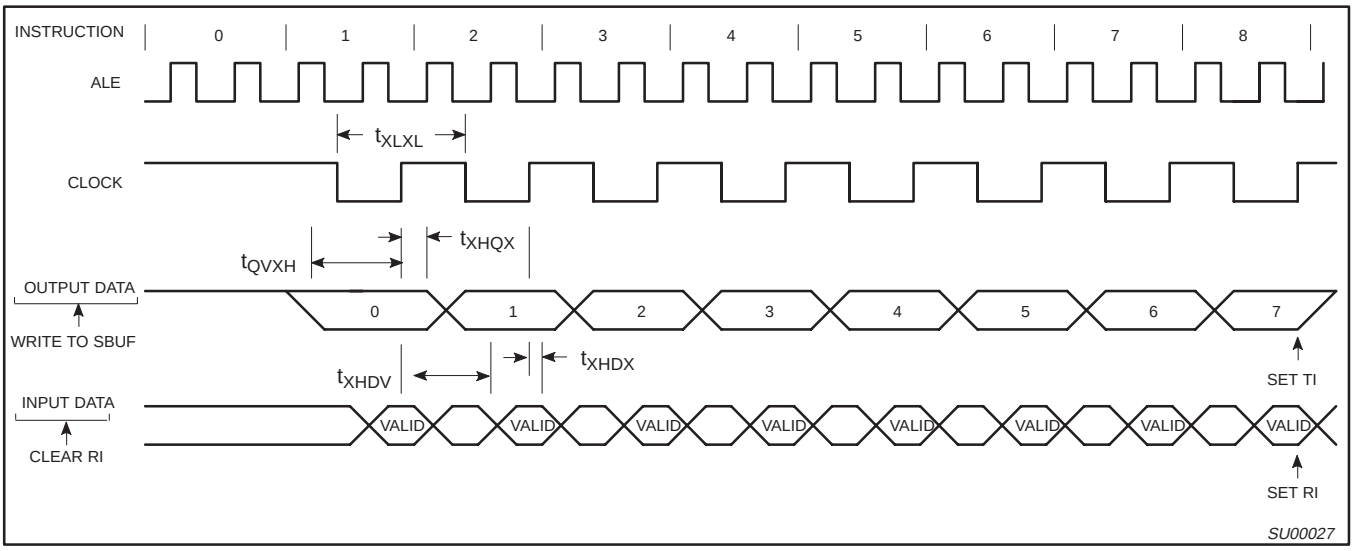


Figure 32. Shift Register Mode Timing

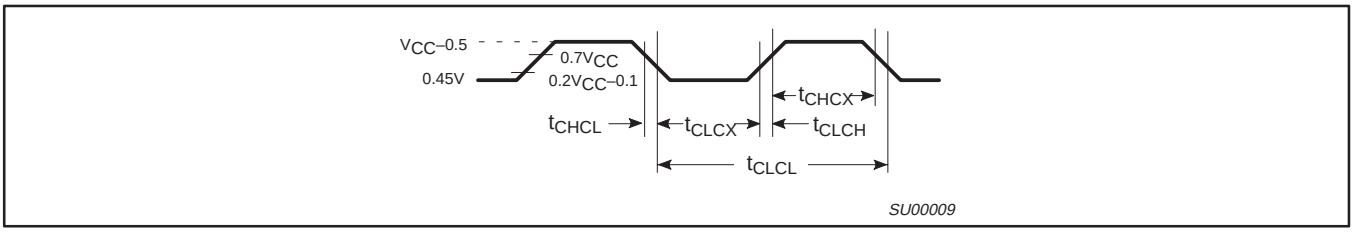


Figure 33. External Clock Drive

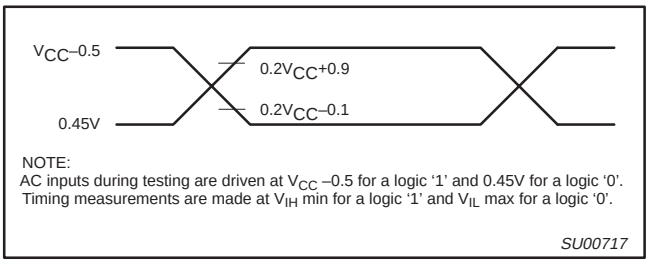


Figure 34. AC Testing Input/Output

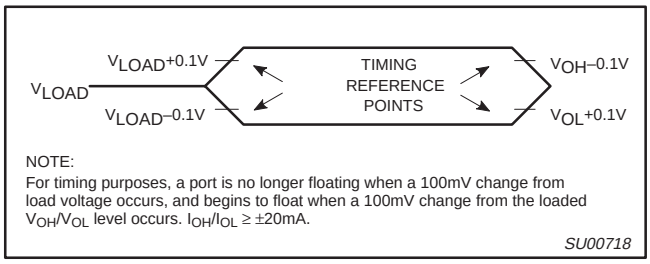


Figure 35. Float Waveform

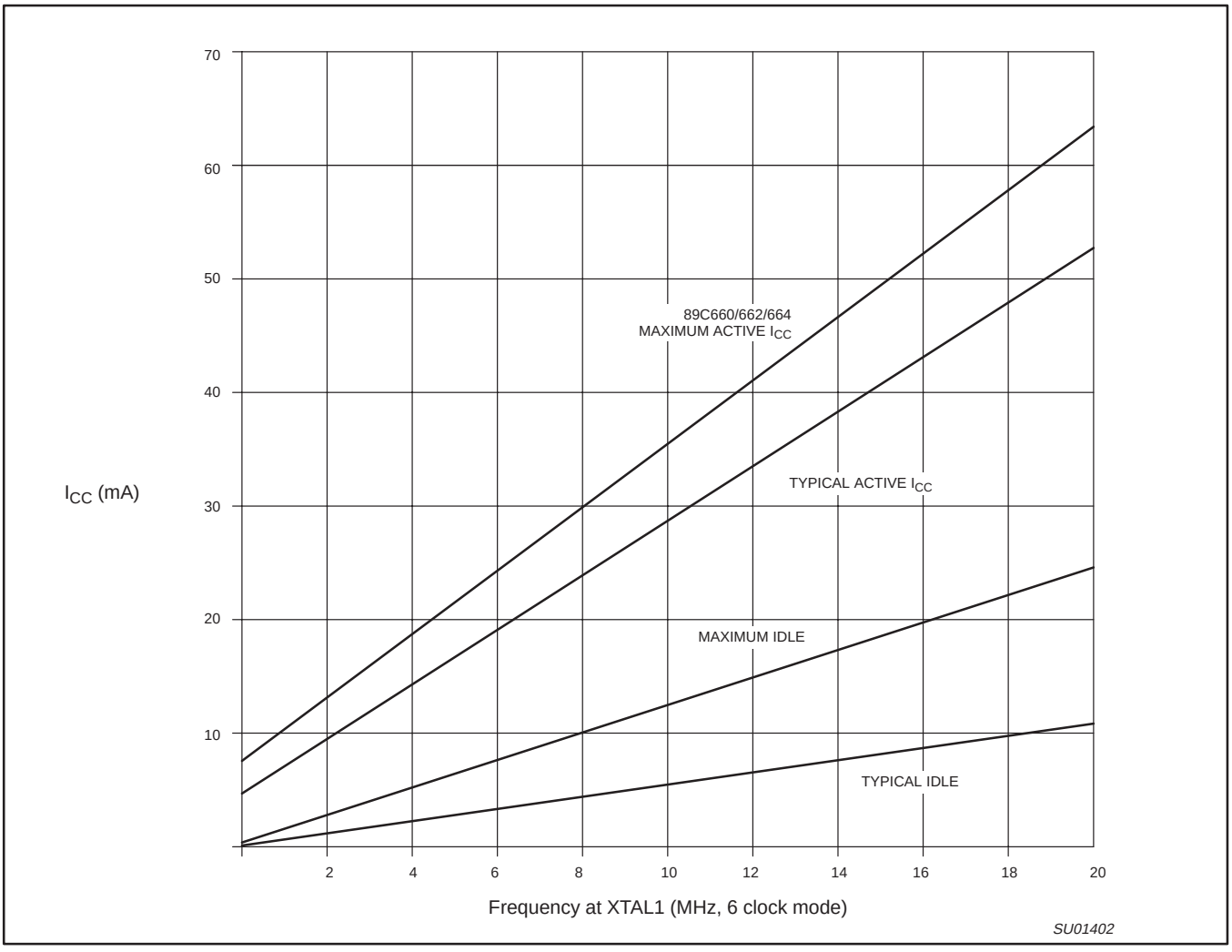
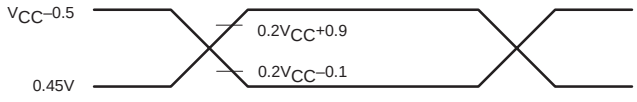


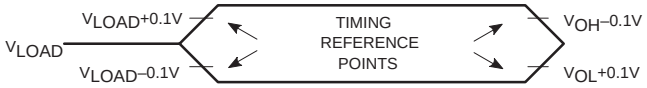
Figure 36. I_{CC} vs. FREQ
Valid only within frequency specifications of the device under test



NOTE:
AC inputs during testing are driven at V_{CC} –0.5 for a logic '1' and 0.45V for a logic '0'.
Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

SU00010

Figure 37. AC Testing Input/Output



NOTE:
For timing purposes, a port is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OH}/I_{OL} \geq \pm 20$mA.

SU00011

Figure 38. Float Waveform

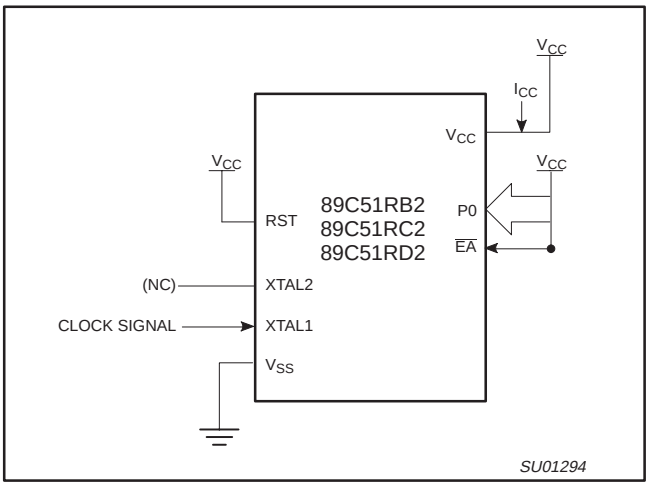


Figure 39. I_{CC} Test Condition, Active Mode. All other pins are disconnected

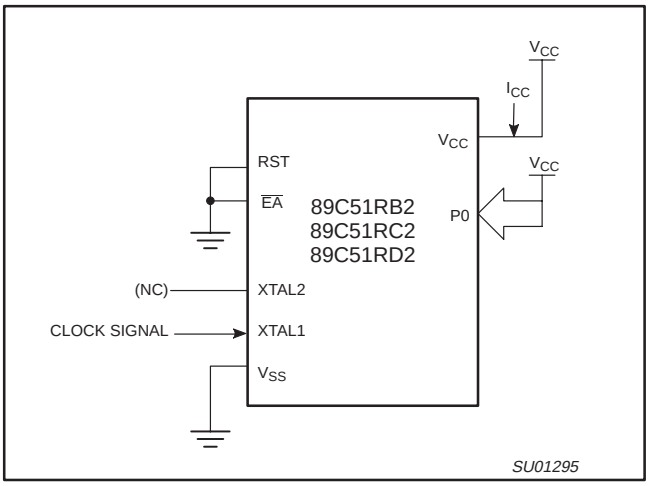


Figure 40. I_{CC} Test Condition, Idle Mode. All other pins are disconnected

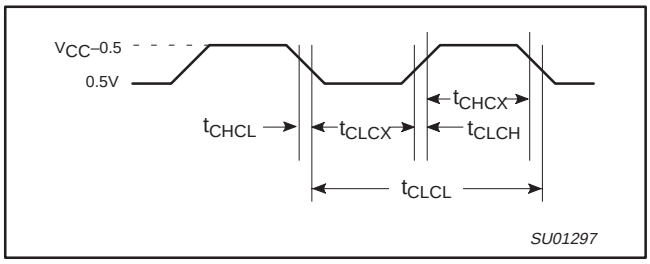


Figure 41. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. $t_{CLCL} = t_{CHCL} = 10$ ns

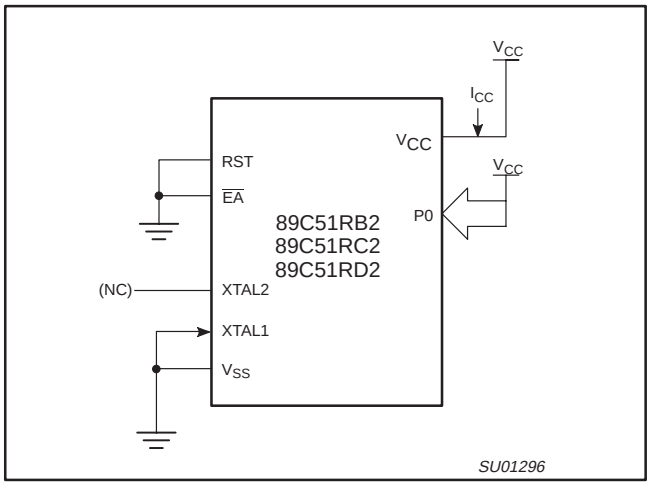


Figure 42. I_{CC} Test Condition, Power Down Mode. All other pins are disconnected; V_{CC} = 2V to 5.5V

FLASH EPROM MEMORY

GENERAL DESCRIPTION

The P89C51RB2/RC2/RD2 Flash memory augments EPROM functionality with in-circuit electrical erasure and programming. The Flash can be read and written as bytes. The Chip Erase operation will erase the entire program memory. The Block Erase function can erase any Flash block. In-system programming and standard parallel programming are both available. On-chip erase and write timing generation contribute to a user friendly programming interface.

The P89C51RB2/RC2/RD2 Flash reliably stores memory contents even after 10,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The P89C51RB2/RC2/RD2 uses a +5 V V_{PP} supply to perform the Program/Erase algorithms.

FEATURES – IN-SYSTEM PROGRAMMING (ISP) AND IN-APPLICATION PROGRAMMING (IAP)

- Flash EPROM internal program memory with Block Erase.
- Internal 1 kbyte fixed boot ROM, containing low-level in-system programming routines and a default serial loader. User program can call these routines to perform In-Application Programming (IAP). The Boot ROM can be turned off to provide access to the full 64 kbyte Flash memory.
- Boot vector allows user provided Flash loader code to reside anywhere in the Flash memory space. This configuration provides flexibility to the user.
- Default loader in Boot ROM allows programming via the serial port without the need for a user provided loader.
- Up to 64 kbytes external program memory if the internal program memory is disabled ($\overline{EA}$ = 0).
- Programming and erase voltage +5 V (+12 V tolerant).
- Read/Programming/Erase using ISP/IAP:
  - Byte Programming (20 μs).
  - Typical quick erase times:
    Block Erase (8 kbytes or 16 kbytes) in 10 seconds.
    Full Erase (64 kbytes) in 20 seconds.
- Parallel programming with 87C51 compatible hardware interface to programmer.
- In-system programming.
- Programmable security for the code in the Flash.
- 10,000 minimum erase/program cycles for each byte.
- 10-year minimum data retention.

CAPABILITIES OF THE PHILIPS 89C51 FLASH-BASED MICROCONTROLLERS

Flash organization

The P89C51RB2/RC2/RD2 contains 16KB/32KB/64KB of Flash program memory. This memory is organized as 5 separate blocks. The first two blocks are 8 kbytes in size, filling the program memory space from address 0 through 3FFF hex. The final three blocks are 16 kbytes in size and occupy addresses from 4000 through FFFF hex.

Figure 43 depicts the Flash memory configurations.

Flash Programming and Erasure

There are three methods of erasing or programming of the Flash memory that may be used. First, the Flash may be programmed or erased in the end-user application by calling low-level routines through a common entry point in the Boot ROM. The end-user application, though, must be executing code from a different block than the block that is being erased or programmed. Second, the on-chip ISP boot loader may be invoked. This ISP boot loader will, in turn, call low-level routines through the same common entry point in the Boot ROM that can be used by the end-user application. Third, the Flash may be programmed or erased using the parallel method by using a commercially available EPROM programmer. The parallel programming method used by these devices is similar to that used by EPROM 87C51, but it is not identical, and the commercially available programmer will need to have support for these devices.

Boot ROM

When the microcontroller programs its own Flash memory, all of the low level details are handled by code that is permanently contained in a 1 kbyte Boot ROM that is separate from the Flash memory. A user program simply calls the common entry point with appropriate parameters in the Boot ROM to accomplish the desired operation. Boot ROM operations include things like: erase block, program byte, verify byte, program security lock bit, etc. The Boot ROM overlays the program memory space at the top of the address space from FC00 to FFFF hex, when it is enabled. The Boot ROM may be turned off so that the upper 1 kbyte of Flash program memory are accessible for execution.

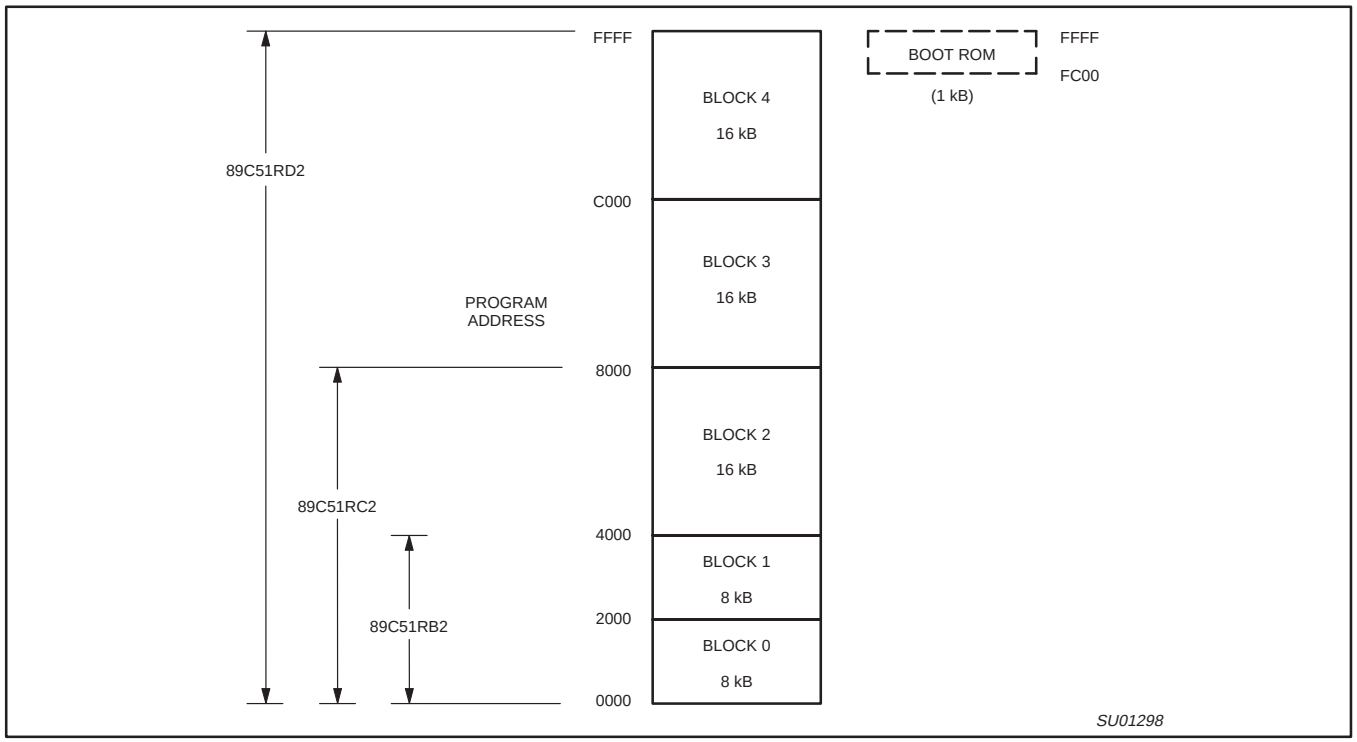


Figure 43. Flash Memory Configurations

Power-On Reset Code Execution

The P89C51RB2/RC2/RD2 contains two special Flash registers: the BOOT VECTOR and the STATUS BYTE. At the falling edge of reset, the P89C51RB2/RC2/RD2 examines the contents of the Status Byte. If the Status Byte is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Status Byte is set to a value other than zero, the contents of the Boot Vector is used as the high byte of the execution address and the low byte is set to 00H. The factory default setting is 0FCH, corresponds to the address 0FC00H for the factory masked-ROM ISP boot loader. A custom boot loader can be written with the Boot Vector set to the custom boot loader.

NOTE: When erasing the Status Byte or Boot Vector, both bytes are erased at the same time. It is necessary to reprogram the Boot Vector after erasing and updating the Status Byte.

Hardware Activation of the Boot Loader

The boot loader can also be executed by holding PSEN LOW, P2.7 high, $\overline{EA}$ greater than V_{IH} (such as +5 V), and ALE HIGH (or not connected) at the falling edge of RESET. This is the same effect as having a non-zero status byte. This allows an application to be built that will normally execute the end user's code but can be manually forced into ISP operation.

If the factory default setting for the Boot Vector (0FCH) is changed, it will no longer point to the ISP masked-ROM boot loader code. If this happens, the only way it is possible to change the contents of the Boot Vector is through the parallel programming method, provided that the end user application does not contain a customized loader that provides for erasing and reprogramming of the Boot Vector and Status Byte.

After programming the Flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

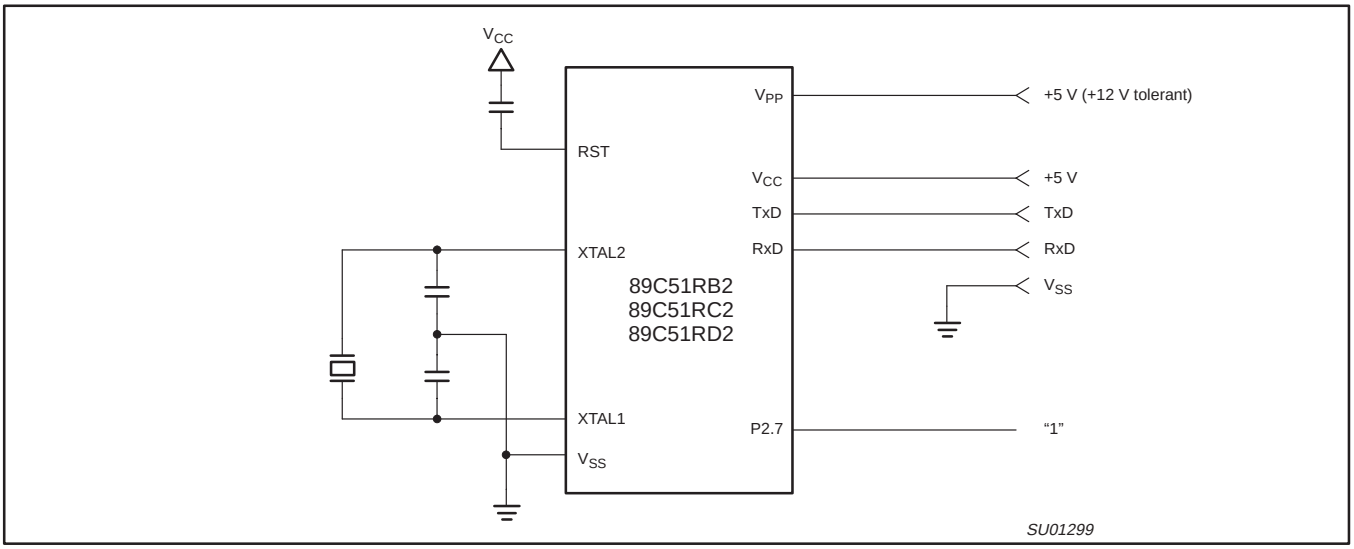


Figure 44. In-System Programming with a Minimum of Pins

In-System Programming (ISP)

The In-System Programming (ISP) is performed without removing the microcontroller from the system. The In-System Programming (ISP) facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89C51RB2/RC2/RD2 through the serial port. This firmware is provided by Philips and embedded within each P89C51RB2/RC2/RD2 device.

The Philips In-System Programming (ISP) facility has made in-circuit programming in an embedded application possible with a minimum of additional expense in components and circuit board area.

The ISP function uses five pins: TxD, RxD, V_{SS}, V_{CC}, and V_{PP} (see Figure 44). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature. The V_{PP} supply should be adequately decoupled and V_{PP} not allowed to exceed datasheet limits.

Using the In-System Programming (ISP)

The ISP feature allows for a wide range of baud rates to be used in your application, independent of the oscillator frequency. It is also adaptable to a wide range of oscillator frequencies. This is accomplished by measuring the bit-time of a single bit in a received character. This information is then used to program the baud rate in terms of timer counts based on the oscillator frequency. The ISP feature requires that an initial character (an uppercase U) be sent to the P89C51RB2/RC2/RD2 to establish the baud rate. The ISP firmware provides auto-echo of received characters.

Once baud rate initialization has been performed, the ISP firmware will only accept Intel Hex-type records. Intel Hex records consist of ASCII characters used to represent hexadecimal values and are summarized below:

:NNAAAARRDD..DDCC<crlf>

In the Intel Hex record, the "NN" represents the number of data bytes in the record. The P89C51RB2/RC2/RD2 will accept up to 16 (10H) data bytes. The "AAAA" string represents the address of the first byte in the record. If there are zero bytes in the record, this field is often set to 0000. The "RR" string indicates the record type. A record type of "00" is a data record. A record type of "01" indicates the end-of-file mark. In this application, additional record types will be added to indicate either commands or data for the ISP facility. The maximum number of data bytes in a record is limited to 16 (decimal). ISP commands are summarized in Table 8.

As a record is received by the P89C51RB2/RC2/RD2, the information in the record is stored internally and a checksum calculation is performed. The operation indicated by the record type is not performed until the entire record has been received. Should an error occur in the checksum, the P89C51RB2/RC2/RD2 will send an "X" out the serial port indicating a checksum error. If the checksum calculation is found to match the checksum in the record, then the command will be executed. In most cases, successful reception of the record will be indicated by transmitting a "." character out the serial port (displaying the contents of the internal program memory is an exception).

In the case of a Data Record (record type 00), an additional check is made. A "." character will NOT be sent unless the record checksum matched the calculated checksum and all of the bytes in the record were successfully programmed. For a data record, an "X" indicates that the checksum failed to match, and an "R" character indicates that one of the bytes did not properly program. It is necessary to send a type 02 record (specify oscillator frequency) to the P89C51RB2/RC2/RD2 before programming data.

The ISP facility was designed to that specific crystal frequencies were not required in order to generate baud rates or time the programming pulses. The user thus needs to provide the P89C51RB2/RC2/RD2 with information required to generate the proper timing. Record type 02 is provided for this purpose.

WinISP, a software utility to implement ISP programming with a PC, is available on Philips Semiconductors' website. In addition, at the website is a listing of third party commercially available serial and parallel programmers.

Table 8. Intel-Hex Records Used by In-System Programming

RECORD TYPE	COMMAND/DATA FUNCTION

00	Program Data
	`:nnaaaa00dd....ddcc`
	Where:
	`Nn = number of bytes (hex) in record`
	`Aaaa = memory address of first byte in record`
	`dd....dd = data bytes`
	`cc = checksum`
	Example:
	`:10008000AF5F67F0602703E0322CFA92007780C3FD`

01	End of File (EOF), no operation
	`:xxxxxx01cc`
	Where:
	`xxxxxx = required field, but value is a “don’t care”`
	`cc = checksum`
	Example:
	`:00000001FF`

02	Specify Oscillator Frequency
	`:01xxxx02ddcc`
	Where:
	`xxxx = required field, but value is a “don’t care”`
	`dd = integer oscillator frequency rounded down to nearest MHz`
	`cc = checksum`
	Example:
	`:0100000210ED (dd = 10h = 16, used for 16.0–16.9 MHz)`

RECORD TYPE	COMMAND/DATA FUNCTION

03	Miscellaneous Write Functions
	`:nnxxxx03ffssddcc`
	Where:
	`nn = number of bytes (hex) in record`
	`xxxx = required field, but value is a “don’t care”`
	`03 = Write Function`
	`ff = subfunction code`
	`ss = selection code`
	`dd = data input (as needed)`
	`cc = checksum`
	
	Subfunction Code = 01 (Erase Blocks)
	`ff = 01`
	`ss = block code as shown below:`
	`block 0, 0k to 8k, 00H`
	`block 1, 8k to 16k, 20H`
	`block 2, 16k to 32k, 40H`
	`block 3, 32k to 48k, 80H`
	`block 4, 48k to 64k, C0H`
	Example:
	`:0200000301C03A erase block 4`
	
	Subfunction Code = 04 (Erase Boot Vector and Status Byte)
	`ff = 04`
	`ss = don’t care`
	Example:
	`:020000030400F7 erase boot vector and status byte`
	
	Subfunction Code = 05 (Program Security Bits)
	`ff = 05`
	`ss = 00 program security bit 1 (inhibit writing to Flash)`
	`01 program security bit 2 (inhibit Flash verify)`
	`02 program security bit 3 (disable external memory)`
	Example:
	`:020000030501F5 program security bit 2`
	
	Subfunction Code = 06 (Program Status Byte or Boot Vector)
	`ff = 06`
	`ss = 00 program status byte`
	`01 program boot vector`
	Example:
	`:030000030601FCF7 program boot vector with 0FCH`
	
	Subfunction Code = 07 (Full Chip Erase)
	Erases all blocks, security bits, and sets status and boot vector to default values
	`ff = 07`
	`ss = don’t care`
	`dd = don’t care`
	Example:
	`:0100000307F5 full chip erase`

04	Display Device Data or Blank Check – Record type 04 causes the contents of the entire Flash array to be sent out the serial port in a formatted display. This display consists of an address and the contents of 16 bytes starting with that address. No display of the device contents will occur if security bit 2 has been programmed. Data to the serial port is initiated by the reception of any character and terminated by the reception of any character.
	
	General Format of Function 04
	`:05xxxx04sssseeeeffcc`
	Where:
	`05 = number of bytes (hex) in record`
	`xxxx = required field, but value is a “don’t care”`
	`04 = “Display Device Data or Blank Check” function code`
	`ssss = starting address`
	`eeee = ending address`
	`ff = subfunction`
	`00 = display data`
	`01 = blank check`
	`cc = checksum`
	Example:
	`:0500000440004FFF0069 display 4000–4FFF`

RECORD TYPE	COMMAND/DATA FUNCTION

05	Miscellaneous Read Functions
	
	General Format of Function 05
	`:02xxxx05ffsscc`
	Where:
	`02 = number of bytes (hex) in record`
	`xxxx = required field, but value is a “don’t care”`
	`05 = “Miscellaneous Read” function code`
	`ffss = subfunction and selection code`
	`0000 = read signature byte – manufacturer id (15H)`
	`0001 = read signature byte – device id # 1 (C2H)`
	`0002 = read signature byte – device id # 2`
	
	`0700 = read security bits`
	`0701 = read status byte`
	`0702 = read boot vector`
	`cc = checksum`
	Example:
	`:020000050001F8 read signature byte – device id # 1`

06	Direct Load of Baud Rate
	
	General Format of Function 06
	`:02xxxx06hhllcc`
	Where:
	`02 = number of bytes (hex) in record`
	`xxxx = required field, but value is a “don’t care”`
	`06 = ”Direct Load of Baud Rate” function code`
	`hh = high byte of Timer 2`
	`ll = low byte of Timer 2`
	`cc = checksum`
	Example:
	`:02000006F500F3`

In Application Programming Method

Several In Application Programming (IAP) calls are available for use by an application program to permit selective erasing and programming of Flash sectors. All calls are made through a common interface, PGM_MTP. The programming functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FFF0H. The oscillator frequency is an integer number rounded down to the nearest megahertz. For example, set R0 to 11 for 11.0592 MHz. Results are returned in the registers. The IAP calls are shown in Table 9.

Using the Watchdog Timer (WDT)

The 89C51Rx2 devices support the use of the WDT in IAP. The user specifies that the WDT is to be fed by setting the most significant bit of the function parameter passed in R1 prior to calling PGM_MTP. The WDT function is only supported for Block Erase when using Quick Block Erase. The Quick Block Erase is specified by performing a Block Erase with register R0 = 0. Requesting a WDT feed during IAP should only be performed in applications that use the WDT since the process of feeding the WDT will start the WDT if the WDT was not running.

Table 9. IAP calls

IAP CALL	PARAMETER
PROGRAM DATA BYTE	Input Parameters: R0 = osc freq (integer) R1 = 02h R1 = 82h (WDT feed) DPTR = address of byte to program ACC = byte to program Return Parameter ACC = 00 if pass, !00 if fail
ERASE BLOCK	Input Parameters: R0 = osc freq (integer) R0 = 0 (Quick Erase) R1 = 01h R1 = 81h (WDT feed) DPH = block code as shown below: block 0, 0k to 8k, 00H block 1, 8k to 16k, 20H block 2, 16k to 32k, 40H block 3, 32k to 48k, 80H block 4, 48k to 64k, C0H DPL = 00h Return Parameter none
ERASE BOOT VECTOR	Input Parameters: R0 = osc freq (integer) R1 = 04h R1 = 84h (WDT feed) DPH = 00h DPL = don't care Return Parameter none
PROGRAM SECURITY BIT	Input Parameters: R0 = osc freq (integer) R1 = 05h R1 = 85h (WDT feed) DPH = 00h DPL = 00h – security bit # 1 (inhibit writing to Flash) 01h – security bit # 2 (inhibit Flash verify) 02h – security bit # 3 (disable external memory) Return Parameter none
PROGRAM STATUS BYTE	Input Parameters: R0 = osc freq (integer) R1 = 06h R1 = 86h (WDT feed) DPH = 00h DPL = 00h – program status byte ACC = status byte Return Parameter ACC = status byte

IAP CALL	PARAMETER
PROGRAM BOOT VECTOR	Input Parameters: R0 = osc freq (integer) R1 = 06h R1 = 86h (WDT feed) DPH = 00h DPL = 01h – program boot vector ACC = boot vector Return Parameter ACC = boot vector
READ DEVICE DATA	Input Parameters: R1 = 03h R1 = 83h (WDT feed) DPTR = address of byte to read Return Parameter ACC = value of byte read
READ MANUFACTURER ID	Input Parameters: R0 = osc freq (integer) R1 = 00h R1 = 80h (WDT feed) DPH = 00h DPL = 00h (manufacturer ID) Return Parameter ACC = value of byte read
READ DEVICE ID # 1	Input Parameters: R0 = osc freq (integer) R1 = 00h R1 = 80h (WDT feed) DPH = 00h DPL = 01h (device ID # 1) Return Parameter ACC = value of byte read
READ DEVICE ID # 2	Input Parameters: R0 = osc freq (integer) R1 = 00h R1 = 80h (WDT feed) DPH = 00h DPL = 02h (device ID # 2) Return Parameter ACC = value of byte read
READ SECURITY BITS	Input Parameters: R0 = osc freq (integer) R1 = 07h R1 = 87h (WDT feed) DPH = 00h DPL = 00h (security bits) Return Parameter ACC = value of byte read
READ STATUS BYTE	Input Parameters: R0 = osc freq (integer) R1 = 07h R1 = 87h (WDT feed) DPH = 00h DPL = 01h (status byte) Return Parameter ACC = value of byte read
READ BOOT VECTOR	Input Parameters: R0 = osc freq (integer) R1 = 07h R1 = 87h (WDT feed) DPH = 00h DPL = 02h (boot vector) Return Parameter ACC = value of byte read

Security

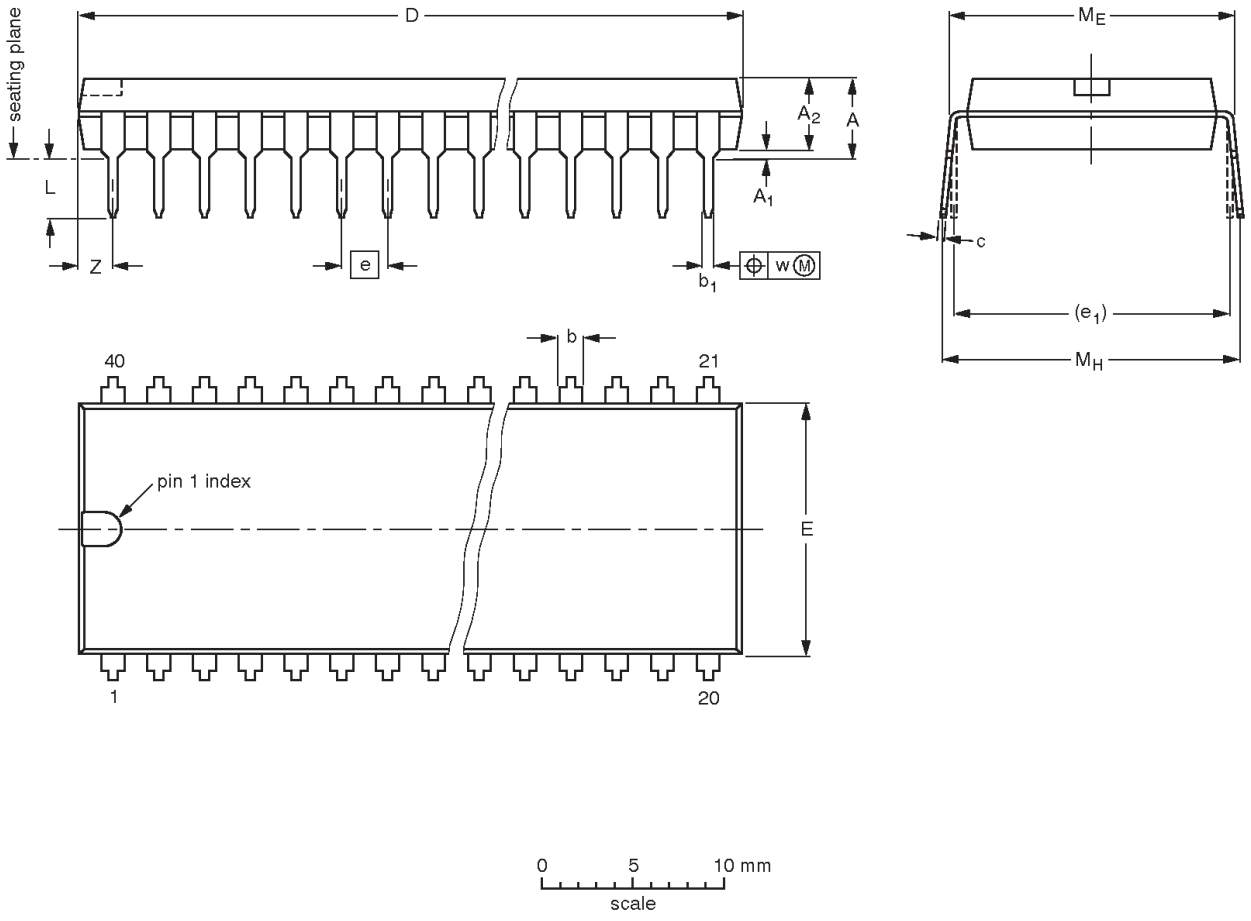
The security feature protects against software piracy and prevents the contents of the Flash from being read. The Security Lock bits are located in Flash. The P89C51RB2/RC2/RD2 has three programmable security lock bits that will provide different levels of protection for the on-chip code and data (see Table 10).

Table 10.

	SECURITY LOCK BITS[1]			PROTECTION DESCRIPTION
LEVEL	LB1	LB2	LB3	
1	0	0	0	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory.
2	1	0	0	Block erase is disabled. Erase or programming of the status byte or boot vector is disabled.
3	1	1	0	Verify of code memory is disabled.
4	1	1	1	External execution is disabled.

NOTE:
1. Security bits are independent of each other. Full-chip erase may be performed regardless of the state of the security bits.
2. Any other combination of lock bits is undefined.
3. Setting LBx doesn't prevent programming of unprogrammed bits.

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

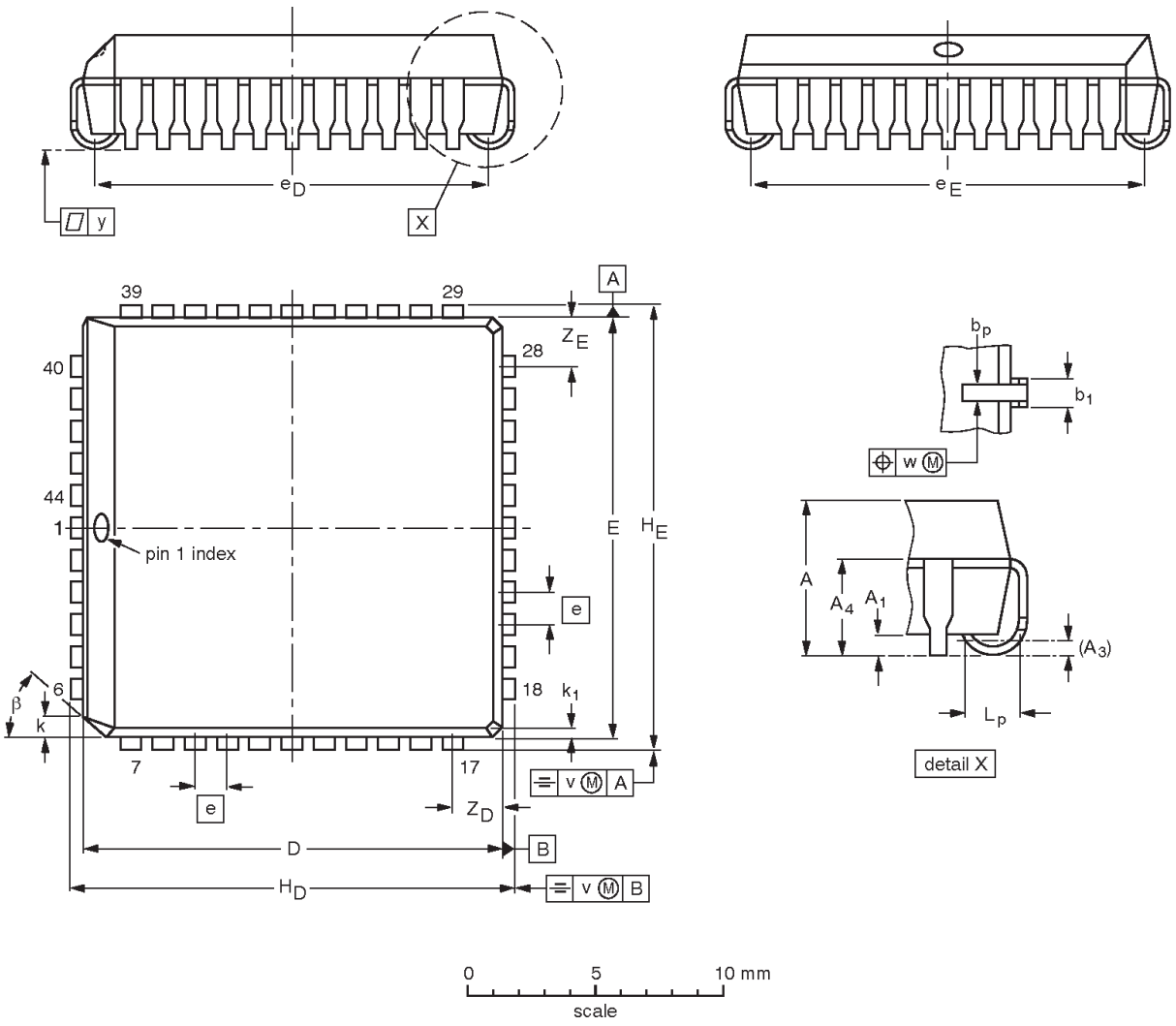
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015	SC-511-40			~~95-01-14~~ 99-12-27

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

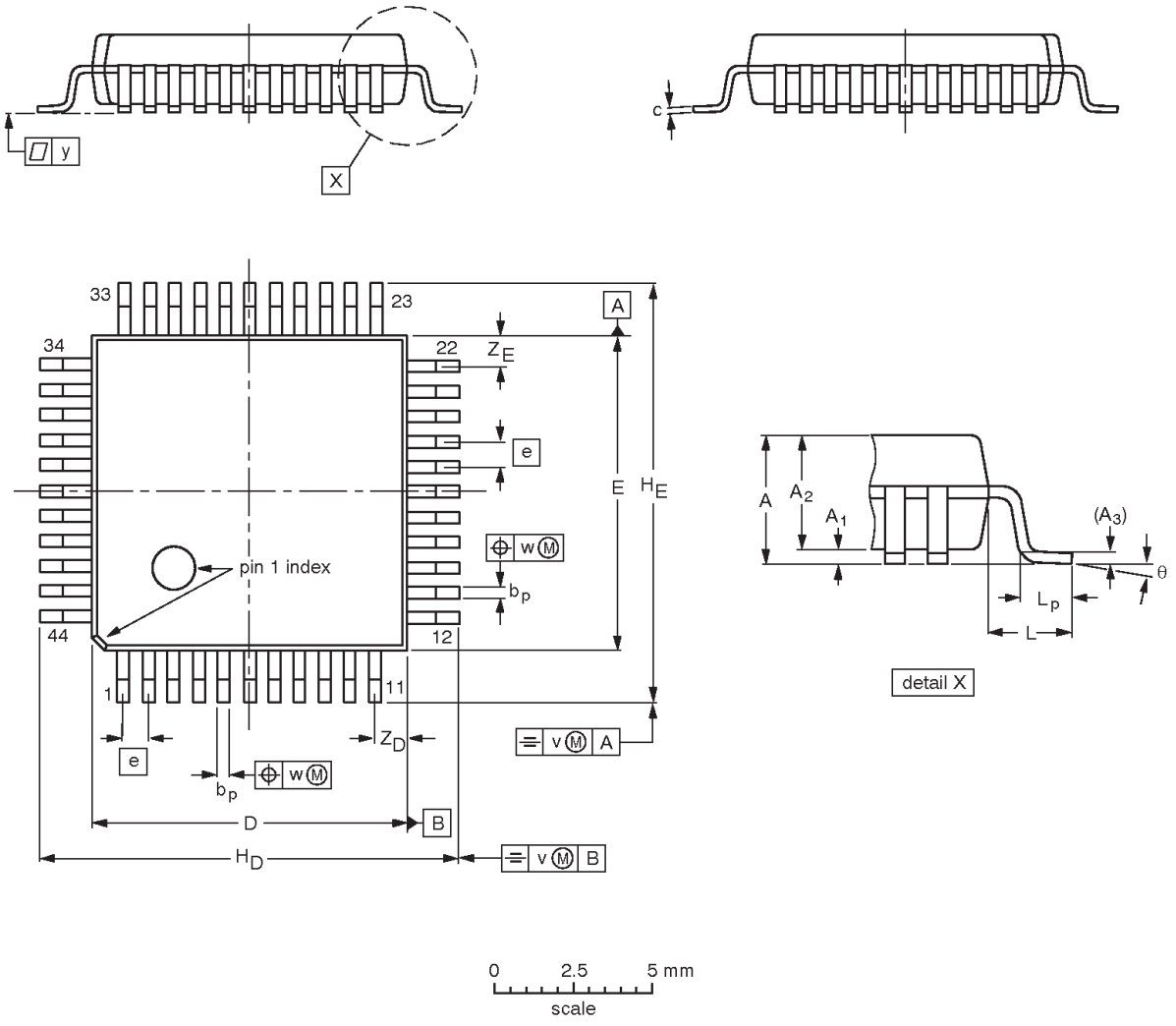
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047				~~97-12-16~~ 99-12-27

LQFP44: plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm **SOT389-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.45 1.35	0.25	0.45 0.30	0.20 0.12	10.10 9.90	10.10 9.90	0.80	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.20	0.20	0.10	1.14 0.85	1.14 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT389-1	136E08	MS-026				~~99-12-17~~ 00-01-19

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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