

# Ensuring Power Supply Sequencing in Spaceflight Systems

## Introduction

In today's complex multi-rail power systems, power sequencing and fault monitoring are essential to boost the performance and the health of the design. Intensive processing of digital loads such as ASICs, FPGAs, DSPs, and microcontrollers require multiple rails to power their circuitry. These devices may demand very specific power-up and power-down sequencing of the rails in order to guarantee reliable operation and better efficiency. Add the complexity of operating in a spaceflight environment and system designers are left with a limited number of ways to implement the power sequencing requirements.

Sequencing and monitoring all power supplies can be accomplished several ways. However, these implementations may not be suitable for spacecraft operating in the harsh deep space environment, or for satellites in Earth orbit. This white paper describes the different sequencing solutions available to power system designers, and introduces a new radiation-hardened quad power supply sequencer that can be cascaded to sequence an unlimited number of power supplies. We will also review its fault monitoring capability to boost system health and performance for commercial space applications. And, we'll examine how the total ionizing dose (TID) and single event effects (SEE) experienced during spaceflight can damage an integrated circuit.

## Methods for Implementing Sequencing

### Method A

The most basic way to implement sequencing is to utilize the power good (PG) and enable (EN) pins of the point-of-load (POL) or low dropout (LDO) regulator. Figure 1 shows the PG pin of converter "n" will be connected to the EN pin of converter "n+1". This cascading configuration is repeated for all the rails in the system. To add a delay between the PG signal asserting and the startup of the next regulator in the sequence, a capacitor is added to the EN pin of the next regulator.

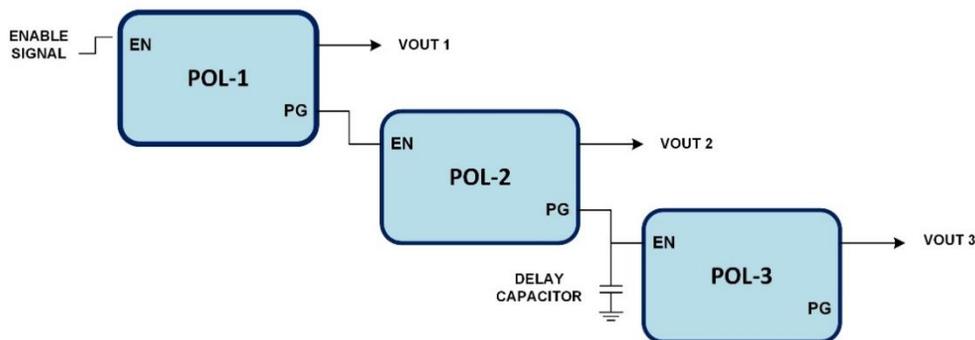


Figure 1. PGGOOD to ENABLE sequencing

This is by far the simplest method and it is essentially cost free; however, it does have major drawbacks. The biggest drawback is this method does not support power-down sequencing in the reverse order. Other drawbacks include the variation of the PG assertion level and the PG delay versus temperature. Figure 2

shows that the PG delay across the temperature range can shift by a factor of two, preventing the proper design of delays between the sequenced rails.

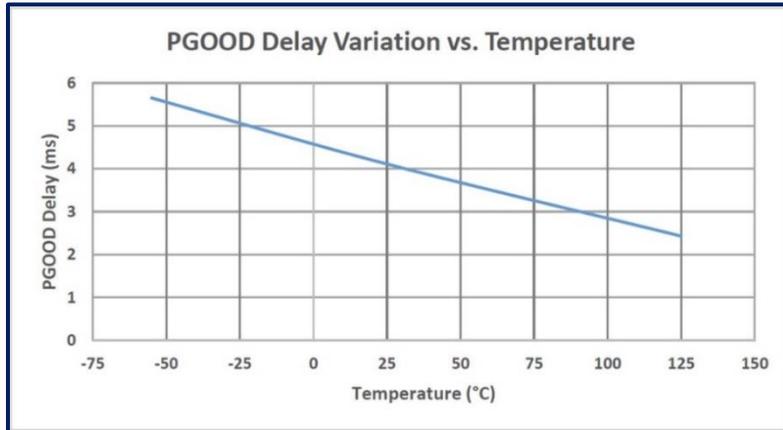


Figure 2. PGOOD variations vs. temperature

### Method B

A discrete solution implementation using comparators, resistors and capacitors can provide power-up sequencing, but this method still does not allow power down in the reverse order (Figure 3). The added complexity does include the benefits of precision voltage monitoring and the ability to delay both the power up and power down. However, the discrete design increases the solution size and the bill of materials cost.

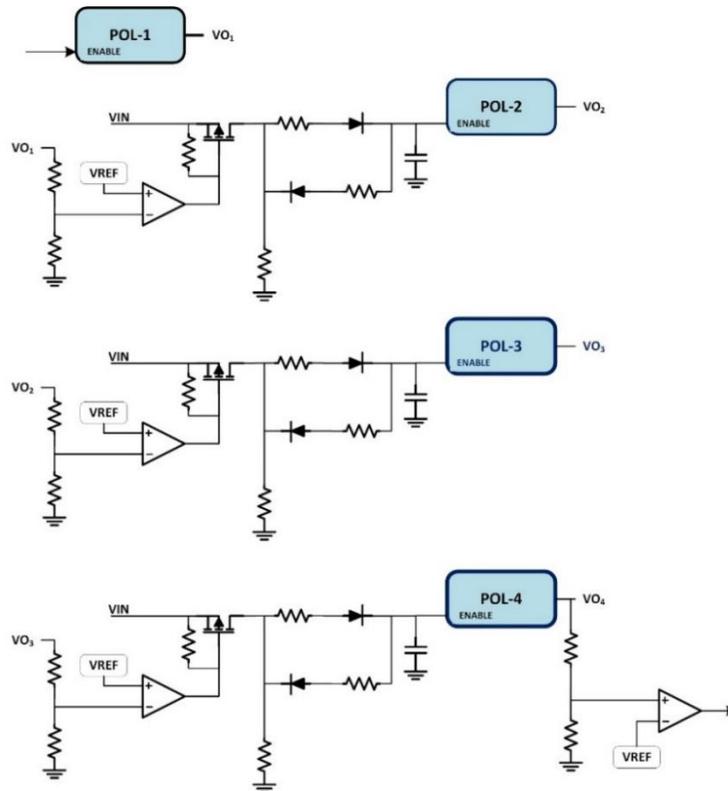


Figure 3. Discrete solution implements sequencing with delays

## Method C

The two previous methods have one common flaw, the inability to power down in the reverse order, which may be needed to ensure system reliability. For example, high-end FPGAs require that the rails for the core, auxiliary and I/O voltages power down in reverse order to avoid excessive current draw and possibly damage the costly digital load.

To meet the power-up and power-down requirements, the ISL70321SEH radiation-hardened quad power supply sequencer may be used. The benefits of using an analog power sequencer are effortless design with minimal external components, and accurate fault monitoring to ensure reliable system operation. A timing diagram showing the power-up and power-down sequencing is presented in Figure 4.

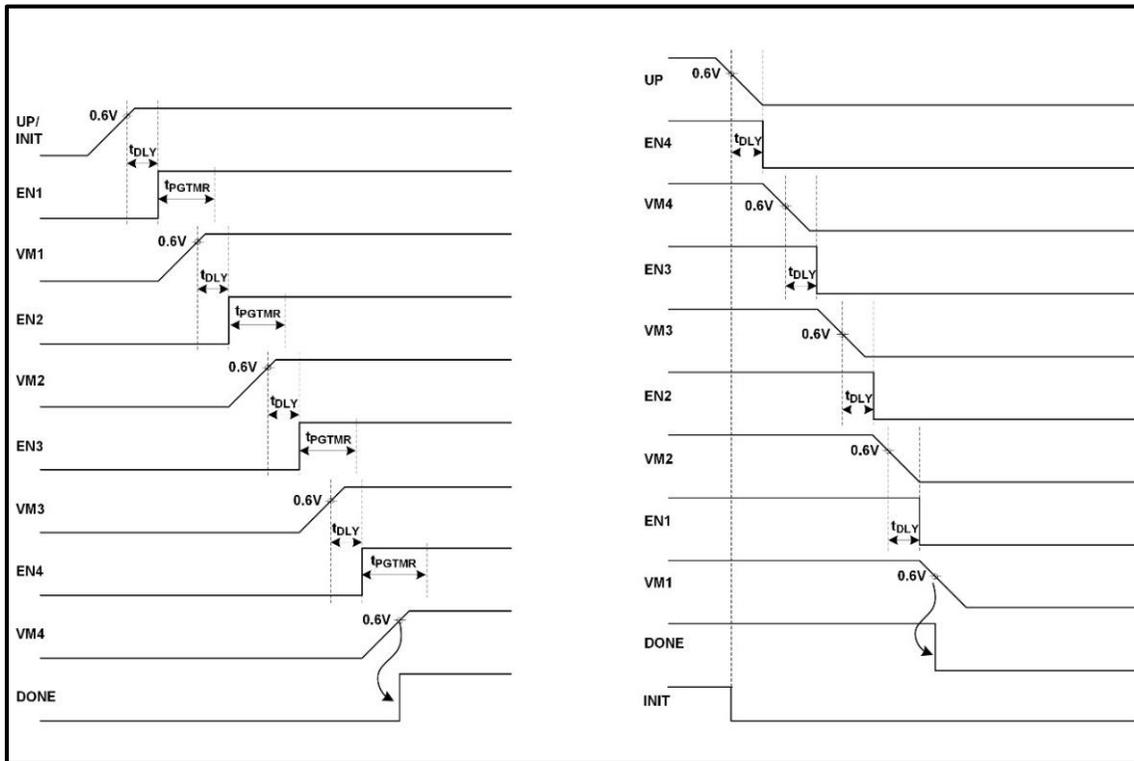
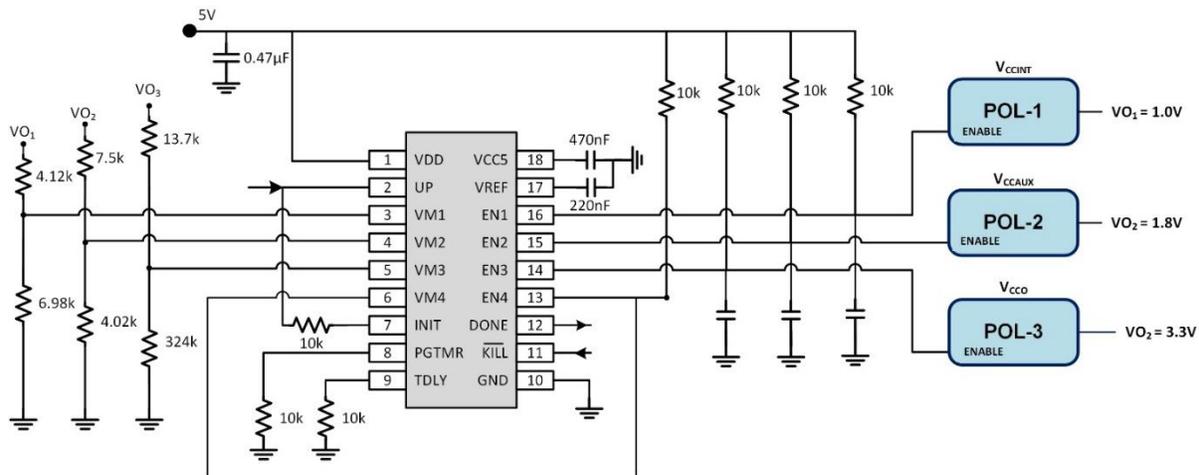


Figure 4. FPGA power supply sequencing application schematic

Figure 5 illustrates an application schematic using the ISL70321SEH to sequence the core, auxiliary and I/O voltage rails required for a typical high-performance FPGA. A resistor divider connected from the power supplies to the corresponding voltage monitor (VM) pin is all that is needed to monitor each rail, this divider also sets the turn-on and turn-off voltage of the next sequenced device. The simple open drain EN outputs make it easy to drive voltage regulators with different enable thresholds. Programmable rising and falling delays are easily achieved by use of a single external resistor. This delay can be programmed between 2ms to 20ms. A power good timer is also included to detect if a rail does not come up within a programmed window of time from 4ms to 40ms.



**Figure 5. ISL70321SEH application diagram**

In addition to sequencing, the ISL70321SEH has active monitoring of over half a dozen fault conditions to ensure reliable power system operation. These include:

- SEQUENCE ORDER FAULT - Out of sequence order
- BROWN OUT FAULT - Any VMx drops below its threshold when a sequence down is not happening
- PGOOD FAULT - VMx remains below its threshold after its ENx is released and the PGOOD timer duration has passed
- INPUT FAULT - Any VMx is high before its ENx is released
- INPUT FAULT - The UP input experiences a change in state before the first channel sequence operation is completed
- OUTPUT FAULT - DONE remains low after the DONE was released and the PGOOD timer duration has passed
- EXTERNALLY TRIGGERED FAULTS

For more complex multi-rail power systems, such as those in RF applications where the number of rails can easily exceed more than a dozen, the ISL70321SEH can easily be cascaded to sequence virtually an unlimited number of rails. Figure 6 highlights the necessary common connections to sequence 12 power supplies using three ISL70321SEH sequencers. Through the use of the UP, INIT and DONE pins, cascaded devices communicate to achieve power-up and reverse power-down sequencing of all the rails.

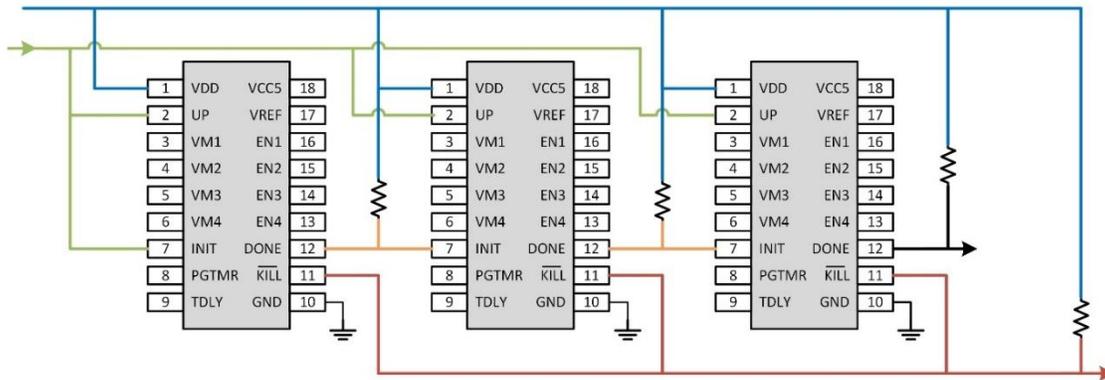


Figure 6. Sequencing 12 voltage rails

## Operating in a Space Environment

Space radiation effects on electronic devices are an important system design consideration. They can cause problems ranging from operational malfunctions to severe physical damage to the devices.

Total ionizing dose and single event effects are two most common effects that cause damage to an integrated circuit. TID effects are the result of accumulated exposure to ionizing radiation. SEE are the result of a single high energy particle that strikes the device. SEE can cause a transient on the output of a circuit. This is known as a single event transient (SET). However, they can also be destructive causing single event burnout (SEB) or single event latch-up (SEL).

The ISL70321SEH is designed to operate in the harsh space environment. Assurance TID testing on the ISL70321SEH is done to 75krad(Si) at 0.01rad(Si)/s and 100krad(Si) at 50-300rad(Si)/s under biased and grounded conditions. SEE testing results show no SEL or SEB for ions with  $LET \leq 86.4 \text{ MeV} \cdot \text{cm}^2/\text{mg}$  with  $V_{dd} \leq 14.7\text{V}$ . No SETs were detected for  $LET \leq 20 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ .

## Conclusion

With the arrival of the industry's first space QML-V qualified radiation-hardened power supply sequencer, spacecraft system design engineers will now be able to implement a simple, accurate and scalable method to achieve the proper power-up and power-down sequencing of DC/DC converters in highly dense multi-rail power systems. Armed with the knowledge that power supply performance will not falter under the harsh environment of space, designers can implement as many power supplies as needed for their spacecraft.

## Next Steps

- [Learn more about the rad-hard ISL70321SEH quad power supply sequencer](#)
- [Download the ISL70321SEH datasheet](#)
- [Download the ISL70321SEH total dose test report](#)
- [Download the ISL70321SEH SEE test report](#)

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