

A NEURAL-TYPE POOL ARITHMETIC UNIT *

S. W. Tsay and R. W. Newcomb

Microsystems Laboratory
Electrical Engineering Department
University of Maryland
College Park, MD 20742
Tel: (301) 405-3708

Abstract

A neural-type pool arithmetic unit is presented. The implementation of this arithmetic unit is based on the describing equations of neural chemical pools that occur in biological neurons where the concentration of a chemical pool depends on the synthesis (inward current) and degradation (outward current) of the chemical materials. With different arrangements of inward and outward currents, this neural type arithmetic unit can perform functions such as addition, subtraction, sign inversion, square, and square root on voltages.

1 Introduction

A neural pool represents the chemical storage in a neural cell and can be used to simulate the primary and second messenger chemical-electrical interactions in a neural system [1][2]. Because of the synthesis and degradation of the chemical materials, a neural pool can be described by the following equation:

$$C \frac{dP}{dt} = I_{in} - I_{out} \quad (1)$$

where C is the pool volume, P is the concentration of the material and I_{in} and I_{out} represent the rates of the materials flowing into and out of the pool, respectively. I_{in} and I_{out} can be modulated by some other pools' levels or by the same pool [1][2]. The equilibrium state of the pool concentration P is determined when the inward current I_{in} is equal to the outward current I_{out} .

Equation (1) can be realized as the simple circuit shown in Figure 1 where the voltage across the capacitor represents the pool concentration and the capacitance represents the pool volume.

2 Circuit Realization of Neural-Type Pool Arithmetic Unit

As mentioned in the introduction, I_{in} and I_{out} can be modulated by other signals. If the simplest modulation, linear modulation, is employed, a pool can be realized as the circuit in Fig. 2 in which I_{in} is linearly proportional to the

* Research Supported by ONR Grant No. N00014-90-J-1114.

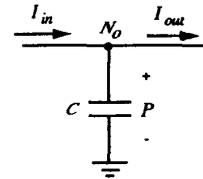


Figure 1: Basic circuit realization of pools.

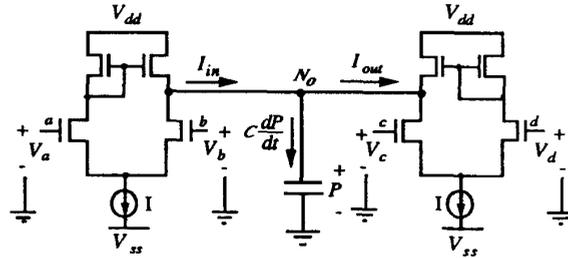


Figure 2: A pool with linear modulation on I_{in} and I_{out} .

difference $V_a - V_b$ and I_{out} is linearly proportional to $V_c - V_d$. As next discussed, the circuit of Fig. 2 realizes various arithmetic functions and, consequently, is called a "neural-type pool arithmetic unit".

2.1 Adder, Subtractor, and Sign Inverter

Three arithmetic functions, addition, subtraction, and sign inversion, can be easily obtained with the circuit of Fig. 2 where different arrangements of the nodes in Fig. 2 can result in different functions.

When we tie node b to N_o and c to GND , the inward and outward currents will be

$$I_{in} = K(V_a - P) \quad \text{and} \quad I_{out} = K'(0 - V_d) \quad (2)$$

where K and K' are constants that depend on the sizes of the transistors and on the current I_{ss} in the differential pairs in Fig. 2. If these two differential pairs are identical, K and K' will be equal and can be cancelled out. The equilibrium state of this pool is determined when $(V_a - P) = (0 - V_d)$. In

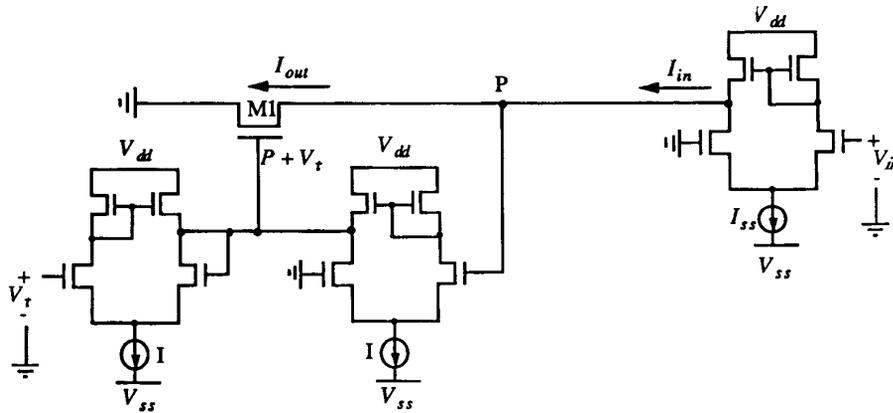


Figure 4: Simplified circuit for "Square root" function.

In equation (11) we rule out the possibility of $P = -K\sqrt{V_{in}}$ because when $V_{in} \geq 0$, the current is always flowing from right to left as indicated in Fig. 4. Thus, the drain voltage of M1, P, is always greater than the source voltage, 0 volt.

2.3 Simulation Results

The five arithmetic functions mentioned above have been simulated by PSPICE and the results are given in Figs. 5 - 9. To improve the accuracy of the results and increase the range of input voltages, we used the improved differential amplifier developed in [3] to replace all the differential amplifiers in Figs. 2, 3, and 4. All the current mirrors in the differential amplifiers were also replaced by a regulated current mirror because of the need for high output resistance [4].

3 Conclusions

A neural-type pool arithmetic unit has been introduced. This arithmetic unit is based on the structure of chemical pools in the biological neuron. Five functions, addition, subtraction, sign inversion, square, and square root have been implemented. This arithmetic unit works on analog voltages with no resistors needed. With this arithmetic unit, circuit which is equivalent to an adjustable threshold MOSFET can be made [5]. More applications are still under investigation.

References

- [1] D. K. Hartline, "Simulation of Restricted Neural Networks with Reprogrammable Neurons," *IEEE Transactions on Circuits and Systems*, Vol. 36, No. 5, May, 1989, pp. 653-660.

- [2] D. K. Hartline, "Synetsim 3.3 User's Manual," Bekey Lab., Honolulu, HI, 1990.
- [3] S. W. Tsay, N. El-Leithy, and R. Newcomb, "CMOS Realization of a Class of Hartline Neural Pools," *Proceedings of the IEEE International Symposium on Circuits and Systems*, New Orleans, May, 1990, Vol. 3, pp. 2417-2420.
- [4] R. Geiger, P. Allen, and N. Strader, "VLSI Design Techniques for Analog and Digital Circuits," McGraw-Hill, New York, 1990.
- [5] S. W. Tsay and R. W. Newcomb, "A Neural Arithmetic Unit and Adjustable Threshold MOSFET," manuscript prepared.

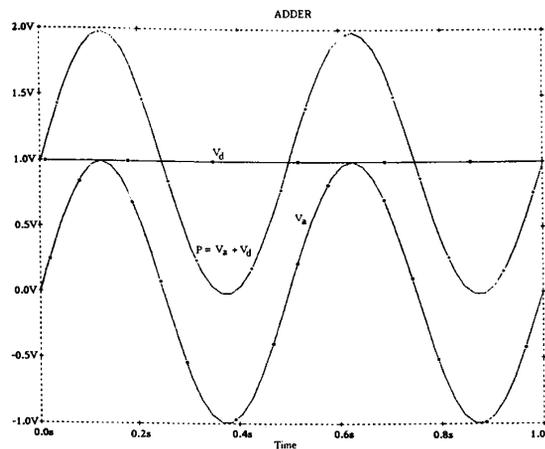


Figure 5: Simulation results for addition.

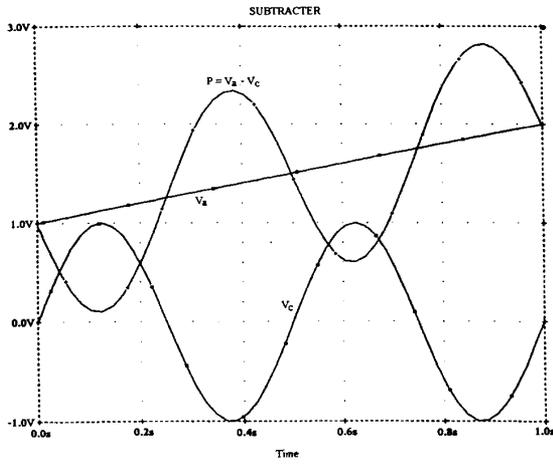


Figure 6: Simulation results for subtraction.

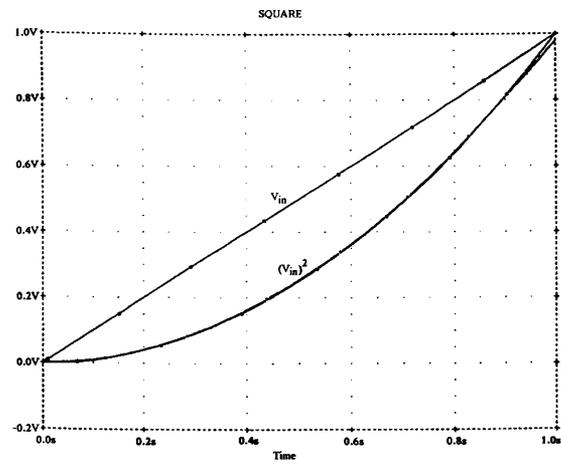


Figure 8: Simulation results for square.

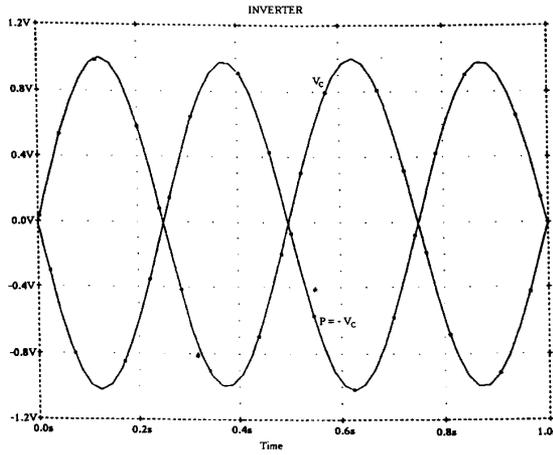


Figure 7: Simulation results for sign inversion.

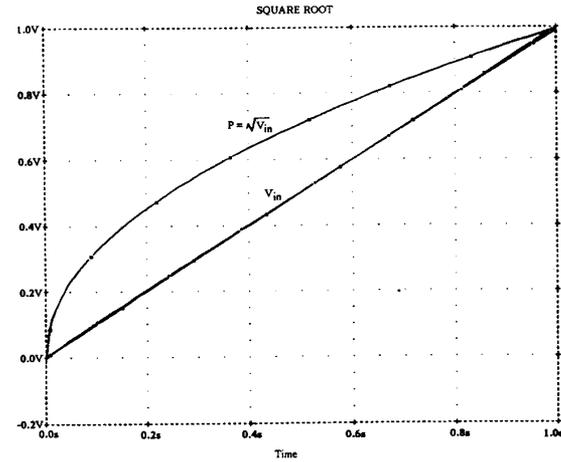


Figure 9: Simulation results for square root.