➢ FEATURES

- RF output frequency range: 33GHz to 38GHz
- Fractional-N synthesizer and Integer N synthesizer
- High resolution 24-bit fractional modulus
- Typical spurious PFD: -50dBc
- Phase noise: -78dBc/Hz@10kHz
- Lock time: < 30 μs
- Analog and digital power supplies: 3.3V/1.0V
- VCO power supply: 1.2V
- Output power: -5dBm
- Die size: 1.6×1.8mm^2

➢ APPLICATION

- Test equipment and instrumentation
- Clock generation

➢ GENETAL DESCRIPTION

The YP7011MB allows implementation of fractional-N and integer N phase-locked loop (PLL) frequency synthesizer when used with an external loop filter and an external reference clock. The wideband millimeter-wave voltage controlled oscillator (VCO) design allows frequencies from 33GHz to 38GHz to be generated.

The YP7011MB integrated VCO, prescalar, frequency divider, PFD, charge pump, fractional-N modulator and SPI interface for compact applications, and the total die size is smaller than 3mm^2.

The integrated high performance fractional-N modulator ensures the output has low in-band spur and neglected out-band spur.

Control of all on-chip register is through a standard SPI interface. Also, the chip has optimized power plan for simplified external power supply.

➢ FUNCTIONAL BLOCK DIAGRAM

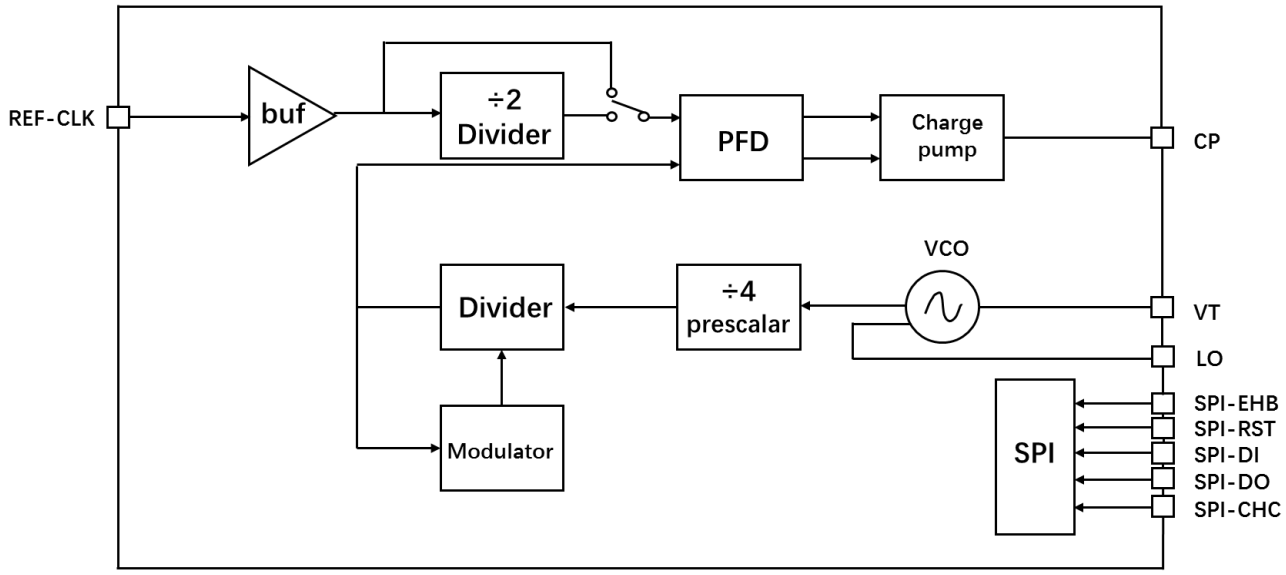

Figure 1. Functional block diagram

➢ REVISION HISTORY

8/2019 – Revision 0: Initial Version

CONTENTS

➢ SPECIFICATIONS

Table 1. Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
REFP AND REFN CHARACTERISTICS						
Input Frequency	f_{REF}	10	40	200	MHz	Ref clock
Input Sensitivity	P_{REF}	-5	0	10	dBm	divider disabled
Phase Detector Frequency				100		
CHARGE PUMP						
Charge Pump Current, Sink and Source	I_{CP}					0.5V ≤ voltage at CP pin (V_{CP}) ≤ V_{DD33} – 0.5V
High Value			3.6		mA	V_{CP} = 1.8V
Low Value			0.4		mA	
Current Matching			5		%	
LOGIC INPUTS						
Input High Voltage	V_{INH}	V_{DD33}-0.3		V_{DD33+}0.3	V	SPI_ENB, SPI_RST,
Input Low Voltage	V_{INL}	-0.3		0.3	V	SPI_DI, SPI_CLK
Input Current	I_{INH}/I_{INL}			±1	μA	
Input Capacitance	C_{IN}		5		pF	
LOGIC OUTPUTS						SPI_DO, PLL_LD
Output High Voltage	V_{OH}	V_{DD33}-0.3			V	
Output Low Voltage	V_{OL}			0.4	V	
POWER SUPPLIES						
VDD12_VCO, VDD12_PRE	V_{DD12}	1.14	1.2	1.26		
VDD10_LO1,VDD10_LO2,VDD10_DIV, VDD10_SDM, VDD10_XO, VDD	V_{DD10}	0.95	1.0	1.05	V	
VDDPST, VDD33_PFDCP, VDD33_VT	V_{DD33}	3.15	3.3	3.45		
RF OUTPUT CHARACTERISTICS						
VCO Frequency Range		33		38	GHz	
VCO Sensitivity	K_{VCO}		1.5		GHz/V	
Maintain Lock Temperature Range		-45		105	°C	
RF Output Power Variation	P_{VCO}		-5		dBm	f_{VCO} = 34.56GHz
RF Output Power Variation (over Frequency)		-14		0		
NOISE CHARACTERISTICS						
VCO Phase Noise			-50		dBc	f_{VCO} = 34.56GHz,offset @10kHz
Whole Chip Phase Noise			-80		dBc	f_{VCO} = 34.56GHz, offset @10kHz
			80		dBc	f_{VCO} = 34.56GHz, offset@100kHz

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Integer Boundary Spurs Out-band Fractional Boundary Spur (Filtered)				-60 -65	dBc dBc	Measured at 40MHz offset (f_{REF}=40MHz) Measured at 2.5MHz offset
Frequency Lock Time				30	μs	Loop bandwidth = 300kHz

➢ TIMING SPECIFICATIONS

Table 2. Timing specifications

Parameter	Symbol	Min	Typ	Max	Unit
Serial Port Interface (SPI) Timing					
SCLK Frequency	tSLCK			50	MHz
SCLK Period	tSLCK	20			ns
SCLK Pulse Width High	tPWH	10			ns
SCLK Pulse Width Low	tPWL	10			ns
SDIO Setup Time	tDS	2.5			ns
SDIO Hold Time	tDH	2.5			ns
SCLK_CLK falling Edge to SPI_DO Valid Propagation	tDV	2.5			ns
SCLK_ENB Fall to SPI_CLK Rise Setup Time	tPCS	10			ns

Timing Diagrams

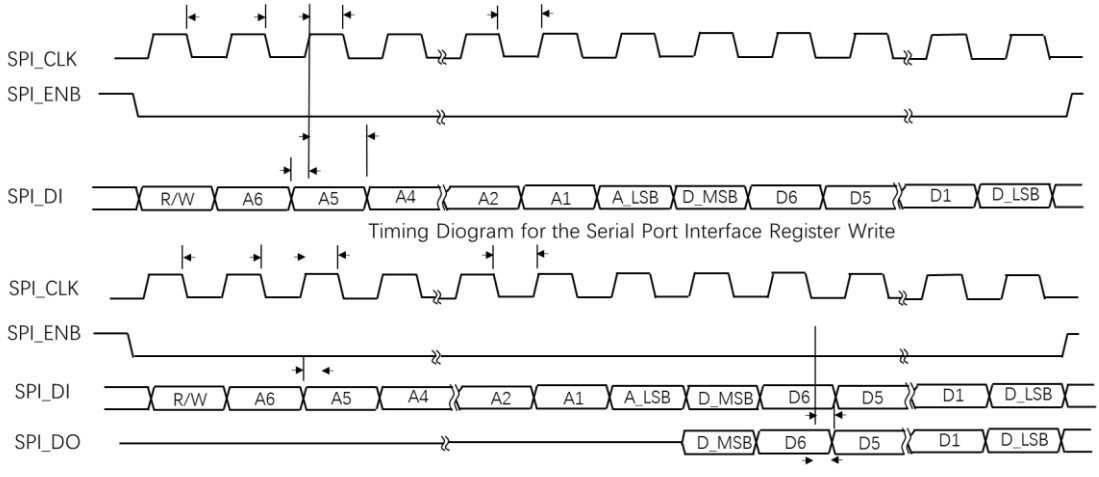

Figure 2. Timing diagrams

➢ ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute maximum ratings (T_A = 25℃)

Parameter	Rating
VDD12_VCO Rail to VSS12_VCO	-0.3V to +1.3V
VDD10_LO1 Rail to VSS10_LO1	-0.3V to +1.2V
VDD10_LO2 Rail to VSS10_LO2	-0.3V to +1.2V
VDD12_PRE Rail to VSS12_PRE	-0.3V to +1.3V
VDD10_DIV Rail to VSS10_DIV	-0.3V to +1.2V
VDD10_SDM Rail to VSS10_SDM	-0.3V to +1.2V
VDD10_XO Rail to VSS10_XO	-0.3V to +1.2V
VDD Rail to VSS	-0.3V to +1.2V
VDDPST Rail to VSSPST	-0.3V to +3.6V
VDD33_PFDCP Rail to VSS33_PFDCP	-0.3V to +3.6V
VDD33_VT Rail to VSS33_VT	-0.3V to +3.6V
CP to VSS33_PFDCP	-0.3V to VDD33_PFDCP+0.3V
VT to VSS33_VT	-0.3V to VDD33_VT+0.3V
DIV4 to VSS12_PRE	-0.3V to VSS12_PRE+0.3V
REF_CLK to VSS10_XO	-0.3V to VSS10_XO+0.3V
LD to VSS33_PFDCP	-0.3V to VDD33_PFDCP+0.3V
Digital Input and Output Voltage to VSSPST	-0.3V to VDDPST+0.3V
Operating Temperature Range	-45°C to +105°C
Storage Temperature Range	-65°C to +125°C
Maximum Junction	125°C
Electrostatic Discharge (ESD) Human Body Model	2.0kV

ESD CAUTION
 ELECTROSTATIC SENSITIVE DEVICE OBSERVE HANDLING PRECAUTIONS

➢ PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

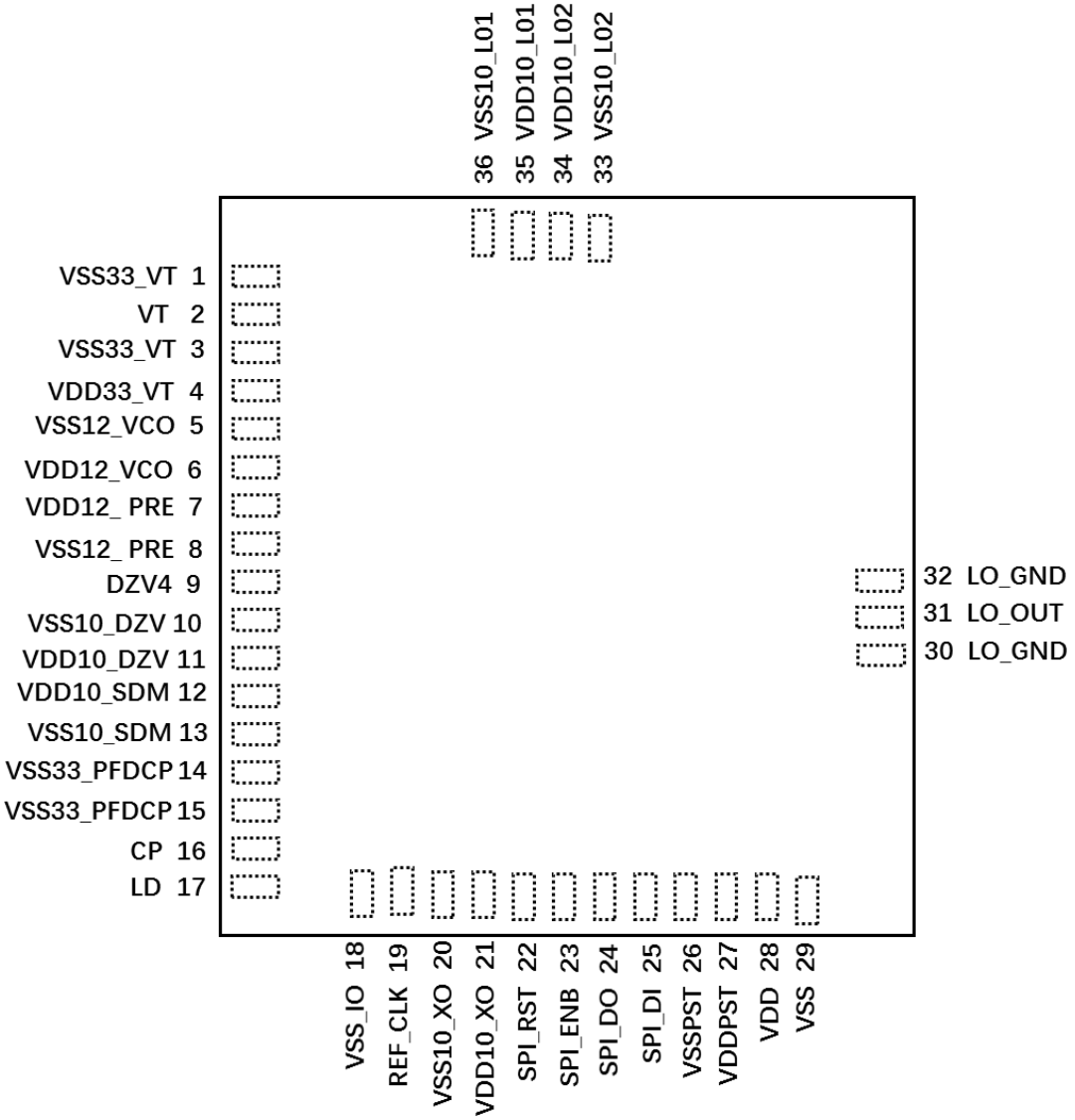

Figure 3. Pin configuration

Table 4. Function descriptions

Pin No.	Mnemonic	Description
1,3	VSS33_VT	Ground for 'VT' pad ESD.
2	VT	VCO frequency tuning input pin.
4	VDD33_VT	Power supply for 'VT' pad ESD.
5	VSS12_VCO	VCO ground.
6	VDD12_VCO	VCO power supply.
7	VDD12_PRE	Prescalar power supply.
8	VSS12_PRE	Prescalar ground.
9	DIV4	Prescalar output.
10	VSS10_DIV	Frequency divider ground.
11	VDD10_DIV	Frequency divider power supply.
12	VDD10_SDM	Frequency modulator power supply.
13	VSS10_SDM	Frequency modulator ground.
14	VSS33_PFDCP	Charge pump ground.
15	VDD33_PFDCP	Charge pump power supply.
16	CP	Charge pump output pin.
17	LD	PLL latch detect output, high level indicates PLL latched.
18	VSS_IO	Ground.
19	REF_CLK	Reference clock input, AC coupling cap is needed outside.
20	VSS10_XO	Reference buffer ground.
21	VDD10_XO	Reference buffer power supply.
22	SPI_RST	SPI reset in, active 0.
23	SPI_ENB	SPI enable, active 0.
24	SPI_DO	SPI data output.
25	SPI_DI	SPI data input.
26	VSSPST	SPI ground.
27	VDDPST	SPI power supply.
28	VDD	Power supply.
29	VSS	Ground.
30,32	LO_GND	LO signal ground.
31	LO_OUT	LO signal output.
33	VSS10_LO2	LO buffer ground.
34	VDD10_LO2	LO buffer power supply.
35	VDD10_LO1	LO buffer ground.
36	VSS10_LO1	LO buffer power supply.

➢ TYPICAL PERFORMANCE CHARACTERISTICS

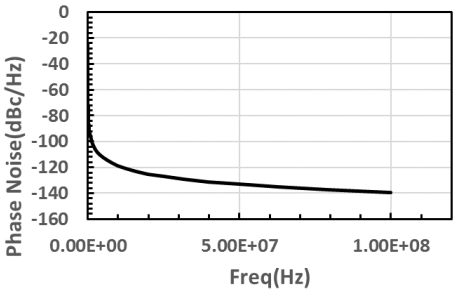

Figure 4. Open-Loop VCO Phase Noise

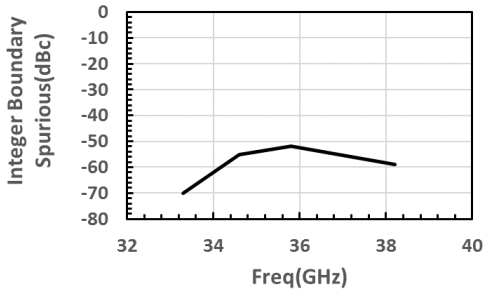

Figure 6. Integer Boundary Spurious (Loop bandwidth=200kHz)

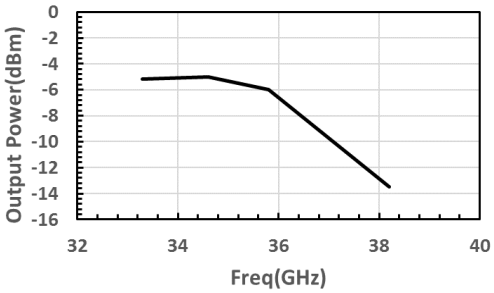

Figure 5. Output Power

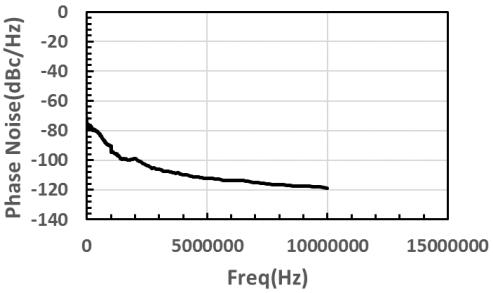

Figure 7. Close-Loop PLL Phase Noise (fLO=34.56GHz, Loop bandwidth=200kHz)

➢ REGISTER SUMMARY

Table 5. Register summary

Reg	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default	R/W
0x00	INT_P <7>	INT_P <6>	INT_P <5>	INT_P <4>	INT_P <3>	INT_P <2>	INT_P <1>	INT_P <0>	0x00	R/W
0x01	Reserved	EN_EX_PLL	SDM_RSTN	SDM_EN	Reserved	EN_REF_DIV2	IN_P <9>	INT_P <8>	0x00	R/W
0x02	INT_S <7>	INT_S <6>	INT_S <5>	INT_S <4>	INT_S <3>	INT_S <2>	INT_S <1>	INT_S <0>	0x00	R/W
0x03	FRAC <7>	FRAC <6>	FRAC <5>	FRAC <4>	FRAC <3>	FRAC <2>	FRAC <1>	FRAC <0>	0x00	R/W
0x04	FRAC <15>	FRAC <14>	FRAC <13>	FRAC <12>	FRAC <11>	FRAC <10>	FRAC <9>	FRAC <8>	0x00	R/W
0x05	FRAC <23>	FRAC <22>	FRAC <21>	FRAC <20>	FRAC <19>	FRAC <18>	FRAC <17>	FRAC <16>	0x00	R/W
0x06	ICP_OSP<2>	ICP_OSP<1>	ICP_OSP<0>	ICP_OSN<4>	ICP_OSN<3>	ICP_OSN<2>	ICP_OSN<1>	ICP_OSN<0>	0x00	R/W
0x07	PFDCP_EN	ICP_OS_EN	ICP<3>	ICP<2>	ICP<1>	ICP<0>	ICP_OSP<4>	ICP_OSP<3>	0x00	R/W

➢ REGISTER DETAIL

Table 6. Reg 0x00 detail

Bit(s)	Bit Name	Description	Default	Access
<7:0>	INT_P<7:0>	Divider P-counter setting	0x00	R/W

Table 7. Reg 0x01 detail

Bit(s)	Bit Name	Description	Default	Access
<7>	Reserved	Reserved	0x0	R/W
<6>	EN_EX_PLL	Prescalar output enable. 0: disable; 1: enable	0x0	R/W
<5>	SDM_RSTN	Divider reset. 0: reset; 1: normal operation	0x0	R/W
<4>	SDM_EN	Fractional modulator enable. 0: enable; 1: disable	0x0	R/W
<3>	Reserved	Reserved	0x0	R/W
<2>	EN_REF_DIV2	Reference clock dividing by 2 enable. 0: disable; 1: enable	0x0	R/W
<1:0>	INT_P<9:8>	Divider P-counter setting	0x0	R/W

Table 8. Reg 0x02 detail

Bit(s)	Bit Name	Description	Default	Access
<7:0>	INT_S<7:0>	Divider S-counter setting	0x00	R/W

Table 9. Reg 0x03 detail

Bit(s)	Bit Name	Description	Default	Access
<7:0>	FRAC<7:0>	Fractional dividing ratio setting	0x00	R/W

Table 10. Reg 0x04 detail

Bit(s)	Bit Name	Description	Default	Access
<7:0>	FRAC<15:8>	Fractional dividing ratio setting	0x00	R/W

Table 11. Reg 0x05 detail

Bit(s)	Bit Name	Description	Default	Access
<7:0>	FRAC<23:16>	Fractional dividing ratio setting	0x00	R/W

Table 12. Reg 0x06 detail

Bit(s)	Bit Name	Description	Default	Access
<7:5>	ICP_OSP<2:0>	Charge pump source current offset setting	0x0	R/W
<4:0>	ICP_OSN<4:0>	Charge pump sink current offset setting	0x00	R/W

Table 13. Reg 0x07 detail

Bit(s)	Bit Name	Description	Default	Access
<7>	PFDCP_EN	Charge pump and PFD enable. 0: disable; 1: enable	0x0	R/W
<6>	ICP_OS_EN	Charge pump offset current enable. 0: disable; 1: enable	0x0	R/W
<5:2>	ICP<3:0>	Charge pump current setting	0x0	R/W
<1:0>	ICP_OSP<4:3>	Charge pump source current offset setting	0x0	R/W

➢ OPERATIONS

Synthesizer output frequency

Using the following equation to set the output frequency:

$$f_{LO} = \frac{f_{REF\_CLK}}{1 + EN\_REF\_DIV2} \times (15 \times (INT\_P + 1) + INT\_S + \overline{SDM\_ENB} \times \frac{FRAC}{2^{24}}) \quad (1)$$

where:
f_{LO} is the synthesizer output frequency;
f_{REF_CLK} is input reference clock frequency;
EN_REF_DIV2 is the reference dividing by 2 enable register value;
INT_P is the P-counter register value;
INT_S is the S-counter register value;
SDM_ENB is the fractional modulator enable register value;
FRAC is the fractional division register value.

Notes:
INT_S cannot be larger than INT_P in integer mode, and cannot be larger than INT_P-4 or lower than 3 in fractional mode.

For example, in integer mode, if 34.56GHz output frequency is needed where the reference clock frequency is 40MHz, two optional settings are as following:

Table 14. Divider configuration for if f_{LO} = 34.56GHz

f_{LO} (GHz)	f_{REF_CLK} (MHz)	EN_REF_DIV2	INT_P	INT_S	SDM_ENB
34.56	40	0	0x00D	0x06	1
		1	0x01C	0x0C	

If 33.44GHz output is needed, only one settings is allowable as following:

Table 15. Divider configuration for if f_{LO} = 33.44GHz

f_{LO} (GHz)	f_{REF_CLK} (MHz)	EN_REF_DIV2	INT_P	INT_S	SDM_ENB
33.44	40	1	0x01B	0x0D	1

In fractional mode, if 34.57GHz output frequency is needed where the reference clock frequency is 40MHz, two optional settings are as following:

Table 16. Divider configuration for if f_{LO} = 34.57GHz

f_{LO} (GHz)	f_{REF_CLK} (MHz)	EN_REF_DIV2	INT_P	INT_S	FRAC	SDM_ENB
34.57	40	0	0x00D	0x06	0x100000	0
		1	0x01C	0x0C		

In fractional mode, if 33.61GHz output frequency is needed, only one setting is allowable as following:

Table 17. Divider configuration for if f_{LO} = 33.61GHz

f_{LO} (GHz)	f_{REF_CLK} (MHz)	EN_REF_DIV2	INT_P	INT_S	FRAC	SDM_ENB
33.61	40	1	0x01C	0x0F	0x200000	0

Charge pump

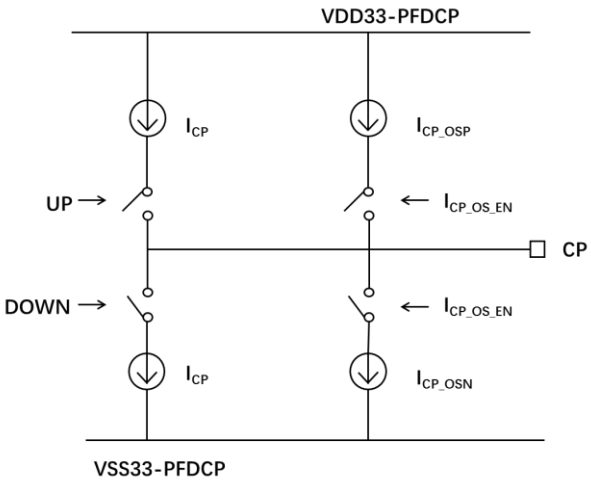

Figure 8. Charge pump diagram

Charge pump current I_{CP} can be tuned from 0.4mA to 3.4mA by I_{CP}<3:0>, tuning step is 0.2mA, as the following table shows. Large I_{CP} good for the PLL in-band phase noise, but low charge pump current is good for power saving and small filter capacitor.

Table 18. Charge pump current settings

ICP<3:0>	I_{CP} (mA)
0000	0.4
0001	0.6
0010	0.8
0011	1.0
0100	1.2
0101	1.4
0110	1.6
0111	1.8
1000	2.0
1001	2.2
1010	2.4
1011	2.6
1100	2.8

ICP<3:0>	I_{CP} (mA)
1101	3.0
1110	3.2
1111	3.4

Charge pump offset current (I_{CP_OSP}/I_{CP_OSN}) is used for tuning charge pump source/sink current edge in stable state, so as to align the asymmetric source and sink current edges caused by circuit mismatch. Better symmetric source and sink current edges is beneficial for integer boundary spurs. Also, the offset current tuning can be used to find best charge pump linearity to improve the fractional boundary spur performance. Charge pump source/sink offset current can be tuning from 0 to 620uA by I_{CP_OSP}<4:0> and I_{CP_OSN}<4:0>, respectively. The tuning step is 20uA.

Loop filter

The loop filter setting will influence the performance of the synthesizer. Larger loop bandwidth is good for VCO phase noise suppression, but worsen the spur performance. The order of the filter is better to be 4 or higher to suppress the quantization noise in fractional mode. Some recommended filter choices are as following.

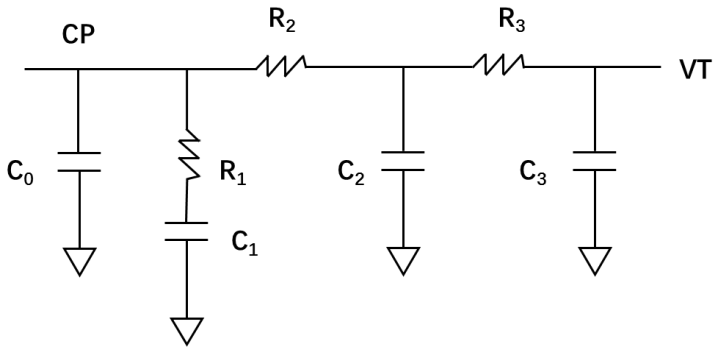

Figure 9. Recommended loop filter configuration

Table 19. Recommended loop filter parameters

f_{LO} (GHz)	EN_REF_DIV2	C0 (nF)	C1 (nF)	C2 (pF)	C3 (pF)	R1 (ohm)	R2 (kohm)	R3 (kohm)
33.28	0	0.19	9.5	83	13	280	370	4.5
34.56	0	0.19	9.1	80	13	290	380	4.7
35.84	0	0.18	8.8	77	13	300	390	4.9
37.12	0	0.17	8.5	74	12	315	400	5.0
38.24	0	0.17	8.3	72	12	325	420	5.2
33.28	1	0.096	4.7	41	6.8	565	730	9.0
34.56	1	0.093	4.6	40	6.6	590	760	9.4
35.84	1	0.089	4.4	38	6.3	610	790	9.8
37.12	1	0.086	4.2	37	6.0	630	820	10.1
38.24	1	0.084	4.1	36	5.9	650	840	10.4

Note:

The recommended values are under I_{CP}=3.4mA, loop bandwidth=300kHz condition.

External PLL configuration

The YP7011MB can use external PLL with internal VCO and prescalar to realize other desired function. The prescalar output (DIV4) pin is used for external PLL divider signal input, the frequency of which is a quarter of VCO frequency.

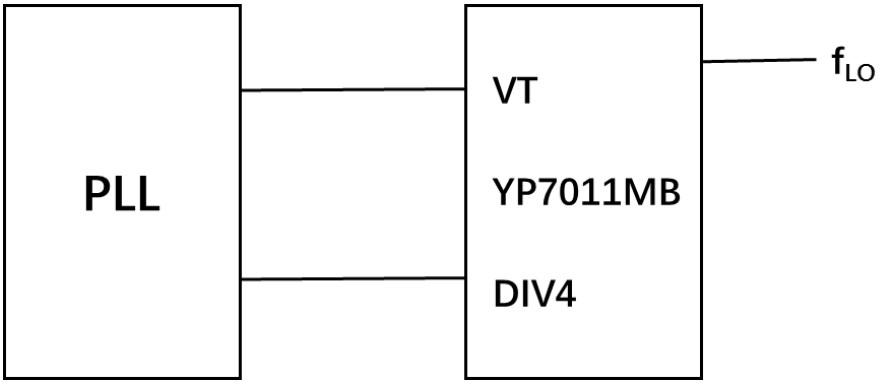

Figure 10. External PLL configuration

Power supplies

To achieve optimal VCO phase noise performance, it is recommended to connect a low noise regulator, such as ADM7150, to the VDD12_VCO and VDD12_PRE pins. 1uF decoupling capacitor is recommended for each power pin, and put as close to the pin as possible.

PCB design guidelines

The thermal pad on the PCB must be at least as large as the chip. And for shortest bonding and smallest parasitic, all the VSS pin can be bonding to the thermal pad. Take care of the RF output traces to minimize discontinuities and ensure the best signal integrity. Via placement and grounding are critical. Rogers 4350, Rogers 4003, or Rogers 3003 dielectric material is suitable for the PCB manufacture.

Output matching

The LO output pin is internally matched to 50ohm and do not require additional decoupling, so the load is recommended to matched to 50ohm for better power transmission.