

## Microchip PIC

PIC12C5XX .....	2
PIC12C67X and PIC12CE67X .....	2
PIC12F508/509 .....	3
PIC12F6XX/16F6XX.....	3
PIC16C432.....	7
PIC16C433.....	8
PIC16CR54A/C54B/CR54B/C54C/CR54C/C55A/C56ACR56A/C57C/CR57B/CR57C/C58B/CR58A/CR58B.....	8
PIC16C52/C54/C54A/C55/C56/C57/C58A .....	9
PIC16C61/71 .....	9
PIC16C62/64/65/73/74.....	9
PIC16C62A/62B/62C/63/63A/64A/65A/65B/66/67PIC16C72/72A/73A/73B/74A/74B/76/77 ....	11
PIC16C620/620A/621/621A/622/622A/712/716 .....	11
PIC16CE623/624/625 .....	11
PIC16C710/711 .....	12
PIC16C773/774.....	12
PIC16C745/765/923/924.....	13
PIC16C7XX .....	14
PIC16C925/926.....	15
PIC16F54 .....	15
PIC16F505/506 .....	16
PIC16F57 .....	17
PIC16C715.....	17
PIC16F716 .....	18
PIC16F62X .....	19
PIC16F627A/628A/648A.....	20
PIC16F8X .....	21
PIC16F7X7 .....	21
PIC16F87/88 .....	23
PIC16F87X .....	24
PIC16F87XA.....	25
PIC16F91X .....	27
*PIC12F629 *PIC16F630 .....	27
*PIC12F675 *PIC16F676 .....	27

## PIC12C5XX

Bit Number:	11	10	9	8	7	6	5	4	3	2	1	0
PIC12C5XX	—	—	—	—	—	—	—	MCLRE	CP	WDTE	FOSC1	FOSC0

bit 11-5: **Reserved:** Write as '0' for PIC12C5XX

bit 4: **MCLRE:** Master Clear Enable bit  
1 =  $\overline{\text{MCLR}}$  pin enabled  
0 =  $\overline{\text{MCLR}}$  internally connected to VDD

bit 3: **CP:** Code Protect Enable bit  
1 = Code memory unprotected  
0 = Code memory protected

bit 2: **WDTE,** WDT Enable bit  
1 = WDT enabled  
0 = WDT disabled

bit 1-0: **FOSC<1:0>**, Oscillator Selection Bit  
11 = External RC oscillator  
10 = Internal RC oscillator  
01 = XT oscillator  
00 = LP oscillator

## PIC12C67X and PIC12CE67X

Bit Number:	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CP1	CP0	CP1	CP0	CP1	CP0	MCLRE	CP1	CP0	PWRT	WDTE	FOSC2	FOSC1	FOSC0

Register: CONFIG  
Address: 2007h

bits 13-8, **CP1:CP0:** Code Protection bits<sup>(1)(2)</sup>  
6-5 11 = Code protection off  
10 = 0400h-07FFh code protected  
01 = 0200h-07FFh code protected  
00 = 0000h-07FFh code protected

bit 7 **MCLRE:** GP3/ $\overline{\text{MCLR}}$  Pin Function Select  
1 = GP3/ $\overline{\text{MCLR}}$  pin function is  $\overline{\text{MCLR}}$   
0 = GP3/ $\overline{\text{MCLR}}$  pin function is digital I/O,  $\overline{\text{MCLR}}$  internally tied to VDD

bit 4 **PWRT:** Power-up Timer Enable bit<sup>(1)</sup>  
1 = PWRT disabled  
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit  
1 = WDT enabled  
0 = WDT disabled

bit 2-0 **FOSC2:FOSC0:** Oscillator Selection bits  
111 = EXTRC oscillator/CLKOUT function on GP4/OSC2/CLKOUT pin  
110 = EXTRC oscillator/GP4 function on GP4/OSC2/CLKOUT pin  
101 = INTRC oscillator/CLKOUT function on GP4/OSC2/CLKOUT pin  
100 = INTRC oscillator/GP4 function on GP4/OSC2/CLKOUT pin  
011 = invalid selection  
010 = HS oscillator  
001 = XT oscillator  
000 = LP oscillator

## PIC12F508/509

**REGISTER 4-1: CONFIGURATION WORD – PIC12F508/509**

—	—	—	—	—	—	—	MCLRE	$\overline{\text{CP}}$	WDTE	FOSC1	FOSC0
bit 11											bit 0

bit 11-5 **Unimplemented:** Read as '1'

bit 4 **MCLRE:** Master Clear Enable bit

1 = GP3/ $\overline{\text{MCLR}}$  pin functions as  $\overline{\text{MCLR}}$

0 = GP3/ $\overline{\text{MCLR}}$  pin functions as GP3,  $\overline{\text{MCLR}}$  internally tied to VDD

bit 3  **$\overline{\text{CP}}$ :** Code Protection bit

1 = Code protection off

0 = Code protection on

bit 2 **WDTE:** Watchdog Timer Enable bit

1 = WDT enabled

0 = WDT disabled

bit 1-0 **FOSC1:FOSC0:** Oscillator Selection bits

00 = LP oscillator

01 = XT oscillator

10 = INTOSC

11 = EXTRC

## PIC12F6XX/16F6XX

- PIC12F635
- PIC12F683
- PIC16F636
- PIC16F639
- PIC16F684
- PIC16F685
- PIC16F687
- PIC16F688
- PIC16F689
- PIC16F690

**REGISTER 4-1: CONFIG<sup>(1)</sup> – CONFIGURATION WORD (ADDRESS:2007h) –  
PIC12F635/PIC16F636/PIC16F639)**

U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	WURE	FCMEN	IESO	BODEN1	BODEN0	CPD	CP	MCLRRE	PWRTRE	WDTE	FOSC2	FOSC1	FOSC0

bit 13

bit 0

bit 13 Unimplemented: Read as '1'

bit 12 **WURE:** Wake-up Reset Enable bit  
1 = Standard wake-up and continue enabled  
0 = Wake-up and Reset enabled

bit 11 **FCMEN:** Fail-Safe Clock Monitor Enable bit  
1 = Fail-Safe Clock Monitor enabled  
0 = Fail-Safe Clock Monitor disabled

bit 10 **IESO:** Internal-External Switch Over bit  
1 = Internal External Switchover mode enabled  
0 = Internal External Switchover mode disabled

bit 9-8 **BODEN<1:0>:** Brown-out Detect Enable bits  
11 = BOD enabled and SBODEN bit disabled  
10 = BOD enabled while running and disabled in Sleep. SBODEN bit disabled.  
01 = SBODEN in the PCON register controls BOD function  
00 = BOD and SBODEN disabled

bit 7 **CPD:** Data Code Protection bit<sup>(2)</sup>  
1 = Data memory is not protected  
0 = Data memory is external read-protected

bit 6 **CP:** Code Protection bit<sup>(3)</sup>  
1 = Program memory is not code-protected  
0 = Program memory is external read and write-protected

bit 5 **MCLRRE:** MCLR Pin Function Select bit<sup>(5)</sup>  
1 = MCLR pin is MCLR function and weak internal pull-up is enabled  
0 = MCLR pin is alternate function, MCLR function is internally disabled

bit 4 **PWRTRE:** Power-up Timer Enable bit<sup>(4)</sup>  
1 = PWRT disabled  
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit  
1 = WDT enabled  
0 = WDT disabled and can be enabled using SWDTEN in the WDTCON register

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits  
000 = LP oscillator: Low-power crystal on RA5/T1CKI/OSC1/CLKIN and RA4/T1G/OSC2/CLKOUT  
001 = XT oscillator: Crystal/resonator on RA5/T1CKI/OSC1/CLKIN and RA4/T1G/OSC2/CLKOUT  
010 = HS oscillator: High-speed crystal/resonator on RA5/T1CKI/OSC1/CLKIN and RA4/T1G/OSC2/CLKOUT  
011 = EC: I/O function on RA4/T1G/OSC2/CLKOUT, CLKIN on RA5/T1CKI/OSC1/CLKIN  
100 = INTOSCIO oscillator: I/O function on RA4/T1G/OSC2/CLKOUT, I/O function on RA5/T1CKI/OSC1/CLKIN  
101 = INTOSC oscillator: CLKOUT function on RA4/T1G/OSC2/CLKOUT, I/O function on RA5/T1CKI/OSC1/CLKIN  
110 = EXTRCIO oscillator: I/O function on RA4/T1G/OSC2/CLKOUT, RC on RA5/T1CKI/OSC1/CLKIN  
111 = EXTRC oscillator: CLKOUT function on RA4/T1G/OSC2/CLKOUT, RC on RA5/T1CKI/OSC1/CLKIN

- Note**
- 1: This Configuration Word register applies to PIC12F635/PIC16F636/PIC16F639 devices only.
  - 2: The entire data memory will be erased when the code protection is turned off.
  - 3: The entire program memory will be erased when the code protection is turned off.
  - 4: Enabling Brown-out Detect does not automatically enable Power-up Timer.
  - 5: When MCLR is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

**REGISTER 4-2: CONFIG<sup>(1)</sup> – CONFIGURATION WORD (ADDRESS:2007h) –  
PIC12F6XX/16F6XX (NOT INCLUDING PIC12F635/PIC16F636/PIC16F639)**

U-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	—	FCMEN	IESO	BODEN1	BODEN0	CPD	CP	MCLRRE	PWRTRE	WDTE	FOSC2	FOSC1	FOSC0

bit 13 bit 0

bit 13-12 **Unimplemented:** Read as '1'

bit 11 **FCMEN:** Fail-Safe Clock Monitor Enable bit  
1 = Fail-Safe Clock Monitor enabled  
0 = Fail-Safe Clock Monitor disabled

bit 10 **IESO:** Internal-External Switch Over bit  
1 = Internal External Switchover mode enabled  
0 = Internal External Switchover mode disabled

bit 9-8 **BODEN<1:0>:** Brown-out Detect Enable bits<sup>(4)</sup>  
11 = BOD enabled and SBODEN bit disabled  
10 = BOD enabled while running and disabled in Sleep. SBODEN bit disabled.  
01 = SBODEN in the PCON register controls BOD function  
00 = BOD and SBODEN disabled

bit 7 **CPD:** Code Protection Data bit<sup>(2)</sup>  
1 = Data memory is not protected  
0 = Data memory is external read-protected

bit 6 **CP:** Code Protection bit<sup>(3)</sup>  
1 = Program memory is not code-protected  
0 = Program memory is external read and write-protected

bit 5 **MCLRRE:** MCLR Pin Function Select<sup>(5)</sup> bit  
1 = MCLR pin is MCLR function and weak internal pull-up is enabled  
0 = MCLR pin is alternate function, MCLR function is internally disabled

bit 4 **PWRTRE:** Power-up Timer Enable bit<sup>(4)</sup>  
1 = PWRT disabled  
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit  
1 = WDT enabled  
0 = WDT disabled and can be enabled using SWDTEN in the WDTCON register

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits  
000 = LP oscillator: Low-power crystal on RA5/T1CKI/OSC1/CLKIN and RA4/T1G/OSC2/CLKOUT<sup>(6)</sup>  
001 = XT oscillator: Crystal/resonator on RA5/T1CKI/OSC1/CLKIN and RA4/T1G/OSC2/CLKOUT<sup>(6)</sup>  
010 = HS oscillator: High-speed crystal/resonator on RA5/T1CKI/OSC1/CLKIN and RA4/T1G/OSC2/CLKOUT<sup>(6)</sup>  
011 = EC: I/O function on RA4/T1G/OSC2/CLKOUT<sup>(6)</sup>, CLKIN on RA5/T1CKI/OSC1/CLKIN  
100 = INTOSCIO oscillator: I/O function on RA4/T1G/OSC2/CLKOUT<sup>(6)</sup>, I/O function on RA5/T1CKI/OSC1/CLKIN  
101 = INTOSC oscillator: CLKOUT function on RA4/T1G/OSC2/CLKOUT<sup>(6)</sup>, I/O function on RA5/T1CKI/OSC1/CLKIN  
110 = EXTRCIO oscillator: I/O function on RA4/T1G/OSC2/CLKOUT<sup>(6)</sup>, RC on RA5/T1CKI/OSC1/CLKIN  
111 = EXTRC oscillator: CLKOUT function on RA4/T1G/OSC2/CLKOUT<sup>(6)</sup>, RC on RA5/T1CKI/OSC1/CLKIN

**Note** 1: This Configuration Word register applies to PIC12F6XX/16F6XX (not including PIC12F635/PIC16F636/PIC16F639) only.

2: The entire data memory will be erased when the code protection is turned off.

3: The entire program memory will be erased when the code protection is turned off.

4: Enabling Brown-out Detect does not automatically enable Power-up Timer.

5: When MCLR is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.

6: For PIC16F685/PIC16F687/PIC16F689/PIC16F690, the pin is RA4/AN3/T1G/OSC2/CLKOUT.

**REGISTER 4-4: CALIB<sup>(1)</sup> – CALIBRATION WORD (ADDRESS: 2008h)–  
PIC16F685/PIC16F687/PIC16F689/PIC16F690<sup>(2),(3),(4)</sup>**

U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	FCAL6	FCAL5	FCAL4	FCAL3	FCAL2	FCAL1	FCAL0	POR2	POR1	POR0	BOD2	BOD1	BOD0

bit 13 bit 0

bit 13 **Unimplemented:** Read as '0'

bit 12-6 **FCAL<6:0>:** Internal Oscillator Calibration bits  
0111111 = Maximum frequency  
.  
.  
0000001  
0000000 = Center frequency  
1111111  
.  
.  
1000000 = Minimum frequency

bit 5-3 **POR<2:0>:** POR Calibration bits  
111 = Maximum POR voltage  
110  
101  
100 = Center POR voltage  
000 = Center POR voltage  
001  
010  
011 = Minimum POR voltage

bit 2-0 **BOD<2:0>**: BOD Calibration bits  
 111 = Maximum BOD voltage  
 110  
 101  
 100 = Center BOD voltage  
 000 = Center BOD voltage  
 001  
 010  
 011 = Minimum BOD voltage

- Note 1:** This Calibration Word register applies to PIC16F685/PIC16F687/PIC16F689/PIC16F690 devices only.  
**Note 2:** This location does not participate in bulk erase operations if the procedure in Figure 3-20 is used.  
**Note 3:** Calibration bits are reserved for factory calibration. These values can and will change across the entire range, therefore, specific values and available adjustment range can not be specified.  
**Note 4:** The calibration bits must be read, preserved, then replaced by the user during Program Memory Bulk Erase operation with PC = 2008h.

**REGISTER 4-5: CALIB1 – CALIBRATION WORD 1 (ADDRESS: 2008H) –  
 PIC12F635/PIC16F636/PIC16F639)<sup>(1)</sup>**

U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	FCAL6	FCAL5	FCAL4	FCAL3	FCAL2	FCAL1	FCAL0	POR2	POR1	POR0	BOD2	BOD1	BOD0	
bit 13														bit 0

bit 13 **Unimplemented:** Read as '0'

bit 12-6 **FCAL<6:0>**: Internal Oscillator Calibration bits  
 0111111 = Maximum frequency  
 •  
 •  
 0000001  
 0000000 = Center frequency. Oscillator is running at the calibrated frequency  
 1111111  
 •  
 •  
 1000000 = Minimum frequency

bit 5-3 **POR<2:0>**: POR Calibration bits  
 111 = Maximum POR voltage  
 110  
 101  
 100 = Center POR voltage  
 000 = Center POR voltage  
 001  
 010  
 011 = Minimum POR voltage

bit 2-0 **BOD<2:0>**: BOD Calibration bits  
 111 = Maximum BOD voltage  
 110  
 101  
 100 = Center BOD voltage  
 000 = Center BOD voltage  
 001  
 010  
 011 = Minimum BOD voltage

- Note 1:** This location does not participate in bulk erase operation, unless PC = 2008h.

**REGISTER 4-6: CALIB2 – CALIBRATION WORD 2 (ADDRESS: 2009h) –  
PIC12F635/PIC16F636/PIC16F639)<sup>(1)</sup>**

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	—	—	—	—	—	—	—	WUR2	WUR1	WUR0	LVD2	LVD1	LVD0
bit 13									bit 0				

bit 13-6 **Unimplemented:** Read as '0'

bit 5-3 **WUR<2:0>:** WUR Calibration bits

111 = Maximum WUR voltage  
110  
101  
100 = Center WUR voltage  
000 = Center WUR voltage  
001  
010  
011 = Minimum WUR voltage

bit 2-0 **LVD<2:0>:** LVD Calibration bits

111 = Maximum LVD voltage  
110  
101  
100 = Center LVD voltage  
000 = Center LVD voltage  
001  
010  
011 = Minimum LVD voltage

**Note 1:** This location does not participate in bulk erase operation, unless PC = 2009h.

## PIC16C432

Bit Number:

	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIC16C432	CP1	CP0	CP1	CP0	CP1	CP0	—	BODEN	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0
	— = Reserved, write as '1' for PIC16C432													

bit 13-8, **CP1:CP0:** Code Protection bits  
5-4:

Device	CP1	CP0	Code Protection
PIC16C432	0	0	All memory protected
	0	1	Upper 3/4 memory protected
	1	0	Upper 1/2 memory protected
	1	1	Code protection off

bit 6: **BODEN:** Brown-out Enable bit  
1 = Enabled  
2 = Disabled

bit 3: **PWRTE/PWRTE:** Power-up Timer Enable bit  
0 = Power-up timer enabled  
1 = Power-up timer disabled

bit 2: **WDTE:** WDT Enable Bit  
1 = WDT enabled  
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator Selection bit  
11 = RC oscillator  
10 = HS oscillator  
01 = XT oscillator  
00 = LP oscillator

**Note 1:** Enabling Brown-out Reset automatically enables the Power-up Timer (PWRT), regardless of the value of bit PWRTE. Ensure the Power-up Timer is enabled any time Brown-out Reset is enabled.

# PIC16C433

Bit Number:													
13	12	11	10	9	8	7	6	5	4	3	2	1	0
CP1	CP0	CP1	CP0	CP1	CP0	MCLR <sup>E</sup>	CP1	CP0	PWRT <sup>E</sup>	WDTE	FOSC2	FOSC1	FOSC0

Register: CONF1
Address: 200h

bit 13-8, 6-5: **CP1:CP0:** Code Protection bits<sup>(1, 2)</sup>

- 11 = Code protection off
- 10 = 0400h-07FFh code protected
- 01 = 0200h-07FFh code protected
- 00 = 0000h-07FFh code protected

bit 7: **MCLR<sup>E</sup>:** GP3/MCLR Pin Function Select

- 1 = GP3/MCLR pin function is MCLR
- 0 = GP3/MCLR pin function is digital I/O, MCLR internally tied to VDD

bit 4: **PWRT<sup>E</sup>:** Power-up Timer Enable bit

- 1 = PWRT disabled
- 0 = PWRT enabled

bit 3: **WDTE:** Watchdog Timer Enable bit

- 1 = WDT enabled
- 0 = WDT disabled

bit 2-0: **FOSC2:FOSC0:** Oscillator Selection bits

- 111 = EXTRC oscillator / CLKOUT function on GP4/OSC2/CLKOUT pin
- 110 = EXTRC oscillator / GP4 function on GP4/OSC2/CLKOUT pin
- 101 = INTRC oscillator / CLKOUT function on GP4/OSC2/CLKOUT pin
- 100 = INTRC oscillator / GP4 function on GP4/OSC2/CLKOUT pin
- 011 = Invalid selection
- 010 = HS oscillator
- 001 = XT oscillator
- 000 = LP oscillator

**Note 1:** All of the CP1:CP0 pairs have to be given the same value to enable the code protection scheme listed.

**2:** 07FFh is always uncode protected on the PIC16C433. This location contains the RETLW xx calibration instruction for the INTRC.

**PIC16CR54A/C54B/CR54B/C54C/CR54C/C55A/C56ACR56A/C57C/CR57B/CR57C/C58B/  
CR58A/CR58B**

**FIGURE 2-1: CONFIGURATION WORD FOR PIC16CR54A/C54B/CR54B/C54C/CR54C/C55A/C56A/CR56A/C57C/CR57B/CR57C/C58B/CR58A/CR58B**

CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTE	FOSC1	FOSC0	Register: CONFIG
bit11	10	9	8	7	6	5	4	3	2	1	bit0	Address: FFFh

bit 11-3: **CP**: Code protection bits  
 1 = Code protection off  
 0 = Code protection on

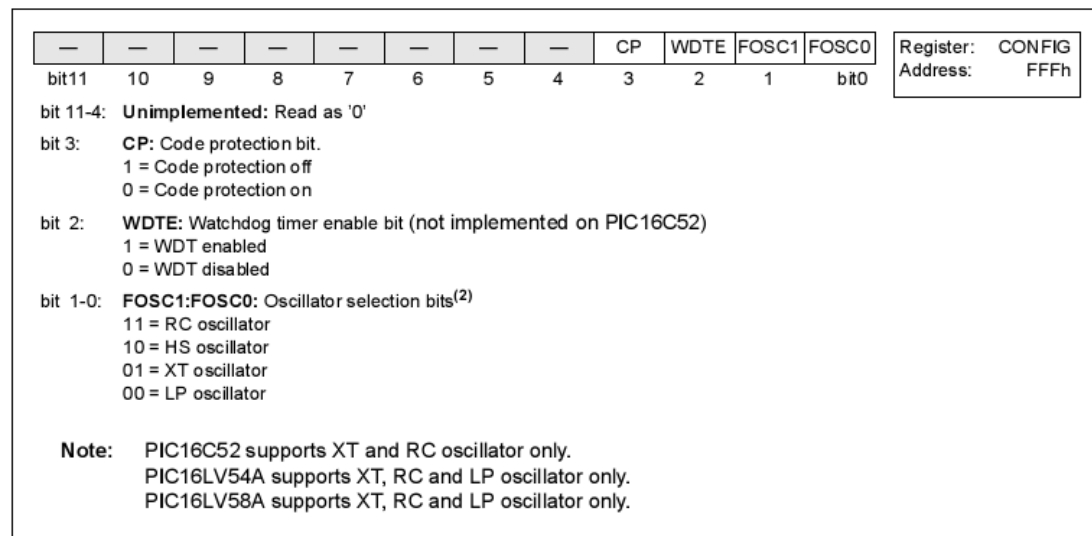
bit 2: **WDTE**: Watchdog timer enable bit  
 1 = WDT enabled  
 0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator selection bits  
 11 = RC oscillator  
 10 = HS oscillator  
 01 = XT oscillator  
 00 = LP oscillator



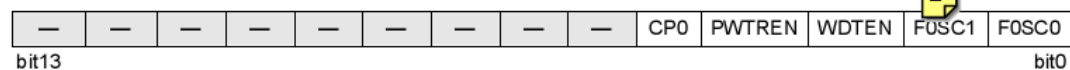
## PIC16C52/C54/C54A/C55/C56/C57/C58A

FIGURE 2-2: CONFIGURATION WORD FOR PIC16C52/C54/C54A/C55/C56/C57/C58A



## PIC16C61/71

REGISTER 3-1: CONFIGURATION WORD FOR PIC16C61/71 (ADDRESS 2007h)



- bit 13-5: **Unimplemented:** Read as '1'
- bit 4: **CP0:** Code Protection bit  
1 = Code protection off  
0 = All memory code protected
- bit 3: **PWTREN:** Power-up Timer Enable bit  
1 = PWRT enabled  
0 = PWRT disabled
- bit 2: **WDTEN:** Watchdog Timer Enable bit  
1 = WDT enabled  
0 = WDT disabled
- bit 1-0: **FOSC1:FOSC0:** Oscillator Selection bits  
11 = RC oscillator  
10 = HS oscillator  
01 = XT oscillator  
00 = LP oscillator

## PIC16C62/64/65/73/74

**REGISTER 3-2: CONFIGURATION WORD FOR PIC16C62/64/65/73/74 (ADDRESS 2007h)**



—	—	—	—	—	—	—	—	CP1	CP0	PWTREN	WDTEN	FOSC1	FOSC0
bit13								bit0					

bit 13-6      **Unimplemented:** Read as '1'

bit 5-4      **CP<1:0>:** Code Protection bits  
              11 = Code protection off  
              10 = Upper 1/2 memory code protected  
              01 = Upper 3/4 memory code protected  
              00 = All memory is protected

bit 3        **PWTREN:** Power-up Timer Enable bit<sup>(2)</sup>  
              1 = PWRT enabled  
              0 = PWRT disabled

bit 2        **WDTEN:** Watchdog Timer Enable bit  
              1 = WDT enabled  
              0 = WDT disabled

bit 1-0      **FOSC1:FOSC0:** Oscillator Selection bits  
              11 = RC oscillator  
              10 = HS oscillator  
              01 = XT oscillator  
              00 = LP oscillator

**Note 1:** Enabling Brown-out Reset automatically enables Power-up Timer (PWRT), regardless of the value of bit PWTREN. Ensure the Power-up Timer is enabled any time Brown-out Reset is enabled.

PIC16C62A/62B/62C/63/63A/64A/65A/65B/66/67PIC16C72/72A/73A/73B/74A/74B/76/77

PIC16C620/620A/621/621A/622/622A/712/716

PIC16CE623/624/625

REGISTER 3-3: CONFIGURATION WORD FOR: PIC16C62A/62B/62C/63/63A/64A/65A/65B/66/67  
PIC16C72/72A/73A/73B/74A/74B/76/77  
PIC16C620/620A/621/621A/622/622A/712/716  
PIC16CE623/624/625  
(ADDRESS 2007h)



CP1	CP0	CP1	CP0	CP1	CP0	—	BOREN	CP1	CP0	PWRTREN	WDTEN	FOSC1	FOSC0
bit13													bit0

bit 13-8 **CP<1:0>: Code Protection bits<sup>(1)</sup>**  
bit 5-4 **For all devices EXCEPT PIC16C620, PIC16C621, PIC16CE623 and PIC16CE624:**  
11 = Code protection off  
10 = Upper 1/2 of program memory code protected  
01 = Upper 3/4 of program memory code protected  
00 = All memory is protected  
**For the PIC16C621 and PIC16CE624:**  
1x = Code protection off  
01 = Upper 1/2 of program memory code protected  
00 = All program memory is code protected  
**For the PIC16C620 and PIC16CE623:**  
1x, 01 = Code protection off  
00 = All program memory is code protected

bit 7 **Unimplemented: Read as '1'**

bit 6 **BOREN: Brown-out Reset Enable bit<sup>(2)</sup>**  
1 = BOR enabled  
0 = BOR disabled

bit 3 **PWRTREN: Power-up Timer Enable bit<sup>(2)</sup>**  
1 = PWRT disabled  
0 = PWRT enabled

bit 2 **WDTEN: Watchdog Timer Enable bit**  
1 = WDT enabled  
0 = WDT disabled

bit 1-0 **FOSC1:FOSC0: Oscillator Selection bits**  
11 = RC oscillator  
10 = HS oscillator  
01 = XT oscillator  
00 = LP oscillator

**Note 1:** All of the CP<1:0> bit pairs have to be given the same value to enable the code protection scheme listed.

**2:** Enabling Brown-out Reset automatically enables Power-up Timer (PWRT), regardless of the value of bit PWRTREN. Ensure the Power-up Timer is enabled any time Brown-out Reset is enabled.

## PIC16C710/711

**REGISTER 3-4: CONFIGURATION WORD, PIC16C710/711 (ADDRESS 2007h)** 

CP0	CP0	CP0	CP0	CP0	CP0	CP0	BOREN	CP0	CP0	PWRTREN	WDTEN	F0SC1	F0SC0
bit13													bit0

bit 13-7 **CP0**: Code Protection bits<sup>(1)</sup>  
 bit 5-4 1 = Code protection off  
 0 = All program memory is code protected, but 00h - 3Fh is writable

bit 6 **BOREN**: Brown-out Reset Enable bit<sup>(2)</sup>  
 1 = BOR enabled  
 0 = BOR disabled

bit 3 **PWRTREN**: Power-up Timer Enable bit<sup>(2)</sup>  
 1 = PWRT disabled  
 0 = PWRT enabled

bit 2 **WDTEN**: Watchdog Timer Enable bit  
 1 = WDT enabled  
 0 = WDT disabled

bit 1-0 **F0SC1:F0SC0**: Oscillator Selection bits  
 11 = RC oscillator  
 10 = HS oscillator  
 01 = XT oscillator  
 00 = LP oscillator

**Note 1:** All of the CP0 bits have to be given the same value to enable the code protection scheme listed.

**2:** Enabling Brown-out Reset automatically enables Power-up Timer (PWRT), regardless of the value of bit PWRTREN. Ensure the Power-up Timer is enabled any time Brown-out Reset is enabled.

## PIC16C773/774

**REGISTER 3-5: CONFIGURATION WORD, PIC16C773/774 (ADDRESS 2007h)** 

CP1	CP0	BORV1	BORV0	CP1	CP0	—	BOREN	CP1	CP0	PWRTREN	WDTEN	F0SC1	F0SC0
bit13													bit0

bit 13-7 **CP<1:0>**: Code Protection bits<sup>(1)</sup>  
 bit 9-8 11 = Code protection off  
 bit 5-4 10 = Upper 1/2 of program memory code protected  
 01 = Upper 3/4 of program memory code protected  
 00 = All program memory is code protected

bit 11-10 **BORV <1:0>**: Brown-out Reset Voltage bits  
 11 = VBOR set to 2.5V  
 10 = VBOR set to 2.7V  
 01 = VBOR set to 4.2V  
 00 = VBOR set to 4.5V

bit 6 **BOREN**: Brown-out Reset Enable bit<sup>(2)</sup>  
 1 = BOR enabled  
 0 = BOR disabled

bit 3 **PWRTREN**: Power-up Timer Enable bit<sup>(2)</sup>  
 1 = PWRT disabled  
 0 = PWRT enabled

bit 2 **WDTEN**: Watchdog Timer Enable bit  
 1 = WDT enabled  
 0 = WDT disabled

bit 1-0      **FOSC1:FOSC0:** Oscillator Selection bits  
                  11 = RC oscillator  
                  10 = HS oscillator  
                  01 = XT oscillator  
                  00 = LP oscillator

**Note 1:** All of the CP<1:0> bits pairs have to be given the same value to enable the code protection scheme listed.

**2:** Enabling Brown-out Reset automatically enables Power-up Timer (PWRT), regardless of the value of bit PWTREN. Ensure the Power-up Timer is enabled any time Brown-out Reset is enabled.

## PIC16C745/765/923/924

**REGISTER 3-6:      CONFIGURATION WORD FOR: PIC16C745/765/923/924  
 (ADDRESS 2007h)**



CP1	CP0	CP1	CP0	CP1	CP0	—	—	CP1	CP0	PWTREN	WDTEN	FOSC1	FOSC0
bit13													bit0

bit 13-8      **CP<1:0>:** Code Protection bits<sup>(1)</sup>  
 bit 5-4      11 = Code protection off  
                  10 = Upper 1/2 of program memory code protected  
                  01 = Upper 3/4 of program memory code protected  
                  00 = All program memory is code protected

bit 7-6      **Unimplemented:** Read as '1'

bit 3      **PWTREN:** Power-up Timer Enable bit<sup>(2)</sup>  
                  1 = PWRT disabled  
                  0 = PWRT enabled

bit 2      **WDTEN:** Watchdog Timer Enable bit  
                  1 = WDT enabled  
                  0 = WDT disabled

bit 1-0      **FOSC1:FOSC0:** Oscillator Selection bits  
                  For PIC16745/765:  
                  11 = E external clock with 4K PLL  
                  10 = H HS oscillator with 4K PL enabled  
                  01 = EC external clock with CLKOUT on OSC2  
                  00 = HS oscillator  
                  For PIC16923/924:  
                  11 = RC oscillator  
                  10 = HS oscillator  
                  01 = XT oscillator  
                  00 = LP oscillator

**Note 1:** All of the CP<1:0> bits pairs have to be given the same value to enable the code protection scheme listed.

## PIC16C7XX

- PIC16C717
- PIC16C770
- PIC16C771
- PIC16C781
- PIC16C782

FIGURE 3-1: CONFIGURATION WORD FOR PIC16C7XX DEVICE (CONFIG: 2007h)

$\overline{CP}$	$\overline{CP}$	BORV1	BORV0	$\overline{CP}$	$\overline{CP}$	—	BODEN	MCLRE	$\overline{PWRT\overline{E}}$	WDTE	FOSC2	FOSC1	FOSC0
bit13	12	11	10	9	8	7	6	5	4	3	2	1	bit0

bit 13-12:  $\overline{CP}$ : Program Memory Code Protection bits

bit 9-8: 1 = Code protection off  
0 = All program memory is protected<sup>(2)</sup>

bit 11-10: BORV<1:0>: Brown-out Reset Voltage bits

00 = VBOR set to 4.5V  
01 = VBOR set to 4.2V  
10 = VBOR set to 2.7V  
11 = VBOR set to 2.5V

bit 7: Unimplemented: Read as '1'

bit 6: BODEN: Brown-out Detect Reset Enable bit<sup>(1)</sup>

1 = Brown-out Detect Reset enabled  
0 = Brown-out Detect Reset disabled

bit 5: MCLRE: RA5/ $\overline{MCLR}$  Pin Function Select

1 = RA5/ $\overline{MCLR}$  pin function is  $\overline{MCLR}$   
0 = RA5/ $\overline{MCLR}$  pin function is digital input,  $\overline{MCLR}$  internally tied to VDD

bit 4:  $\overline{PWRT\overline{E}}$ : Power-up Timer Enable bit<sup>(1)</sup>

1 = PWRT disabled  
0 = PWRT enabled

bit 3: WDTE: Watchdog Timer Enable bit

1 = WDT enabled  
0 = WDT disabled

bit 2-0: FOSC<2:0>: Oscillator Selection bits<sup>(3)</sup>

000 = LP oscillator: Ceramic resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN  
001 = XT oscillator: Crystal on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN  
010 = HS oscillator: High frequency crystal on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN  
011 = EC: I/O function on RA6/OSC2/CLKOUT pin, CLKIN function on RA7/OSC1/CLKIN  
100 = INTRC oscillator: I/O function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN  
101 = INTRC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN  
110 = ER oscillator: I/O function on RA6/OSC2/CLKOUT pin, Resistor on RA7/OSC1/CLKIN<sup>(4)</sup>  
111 = ER oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, Resistor on RA7/OSC1/CLKIN<sup>(4)</sup>

**Note 1:** PIC16C771/770: Enabling Brown-out Reset automatically enables the Power-up Timer (PWRT), regardless of the value of bit  $\overline{PWRT\overline{E}}$ . Ensure the Power-up Timer is enabled any time Brown-out Reset is enabled.

PIC16C781/782: Brown-out Reset and Power-up Timer (PWRT) operate independently.

**2:** All of the CP bits must be given the same value to enable code protection.

**3:** When the internal oscillator is selected (INTRC or ER), and the part is in RESET, the oscillator is disabled and CLKOUT is held low.

**4:** PIC16C717/770/771 has ER modes; PIC16C781/782 has external RC modes.

## PIC16C925/926

**REGISTER 3-7: CONFIGURATION WORD FOR PIC16C925/926 (ADDRESS 2007h)**

—	—	—	—	—	—	—	BOREN	CP1	CP0	PWRTREN	WDTEN	FOSC1	FOSC0
bit13													bit0

bit 13-7 **Unimplemented:** Read as '1'

bit 6 **BOREN:** Brown-out Reset Enable bit<sup>(1)</sup>  
 1 = BOR enabled  
 0 = BOR disabled

bit 5-4 **CP<1:0>:** Program Memory Code Protection bits

For PIC16C926:

11 = Code protection off  
 10 = Lower 1/2 of program memory code protected (0000h-0FFFh)  
 01 = All but last 256 bytes of program memory code protected (0000h-1EFFh)  
 00 = All memory is protected

For PIC16C925:

11 = Code protection off  
 10 = Lower 1/2 of program memory code protected (0000h-07FFh)  
 01 = All but last 256 bytes of program memory code protected (0000h-0EFFh)  
 00 = All program memory is protected

**Note:** For PIC16C925, address values of 1000h to 1FFFh wrap around to 0000h to 0FFFh.

bit 3 **PWRTREN:** Power-up Timer Enable bit<sup>(1)</sup>  
 1 = PWRT disabled  
 0 = PWRT enabled

bit 2 **WDTEN:** Watchdog Timer Enable bit  
 1 = WDT enabled  
 0 = WDT disabled

bit 1-0 **FOSC1:FOSC0:** Oscillator Selection bits  
 11 = RC oscillator  
 10 = HS oscillator  
 01 = XT oscillator  
 00 = LP oscillator

**Note 1:** Enabling Brown-out Reset automatically enables Power-up Timer (PWRT), regardless of the value of bit PWRTREN. Ensure the Power-up Timer is enabled any time Brown-out Reset is enabled.

## PIC16F54

—	—	—	—	—	—	—	—	—	CP	WDTE	FOSC1	FOSC0
bit 11												bit 0

bit 11-4: **Unimplemented:** Read as '1'

bit 3: **CP:** Code Protection bit.  
 1 = Code protection off  
 0 = Code protection on

bit 2: **WDTE:** Watchdog Timer Enable bit  
 1 = WDT enabled  
 0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator Selection bits  
 00 = LP oscillator  
 01 = XT oscillator  
 10 = HS oscillator  
 11 = RC oscillator

## PIC16F505/ 506

**REGISTER 4-1: CONFIGURATION WORD – PIC16F505**

—	—	—	—	—	—	MCLRE	$\overline{\text{CP}}$	WDTE	FOSC2	FOSC1	FOSC0
bit 11											bit 0

bit 11-6 **Unimplemented:** Read as '1'

bit 5 **MCLRE:** Master Clear Enable bit

1 = RB3/ $\overline{\text{MCLR}}$  pin functions as  $\overline{\text{MCLR}}$

0 = RB3/ $\overline{\text{MCLR}}$  pin functions as RB3,  $\overline{\text{MCLR}}$  internally tied to VDD

bit 4  **$\overline{\text{CP}}$ :** Code Protection bit

1 = Code protection off

0 = Code protection on

bit 3 **WDTE:** Watchdog Timer Enable bit

1 = WDT enabled

0 = WDT disabled

bit 2-0 **FOSC2:FOSC0:** Oscillator Selection bits

000 = LP oscillator

001 = XT oscillator

010 = HS oscillator

011 = EC oscillator with RB4 function on RB4/OSC2/CLKOUT

100 = INTOSC with RB4 function on RB4/OSC2/CLKOUT

101 = INTOSC with CLKOUT function on RB4/OSC2/CLKOUT

110 = EXTRC with RB4 function on RB4/OSC2/CLKOUT

111 = EXTRC with CLKOUT function on RB4/OSC2/CLKOUT

**REGISTER 4-1: CONFIGURATION WORD – PIC16F506**

—	—	—	—	IOSCFS	MCLRE	$\overline{\text{CP}}$	WDTE	FOSC2	FOSC1	FOSC0
bit 11										bit 0

bit 11-7 **Unimplemented:** Read as '1'

bit 6 **IOSCFS:** Internal Oscillator Frequency Select bit

1 = 8 MHz

0 = 4 MHz

bit 5 **MCLRE:** Master Clear Enable bit

1 =  $\overline{\text{MCLR}}/\text{VPP}/\text{RB3}$  pin functions as  $\overline{\text{MCLR}}$

0 =  $\overline{\text{MCLR}}/\text{VPP}/\text{RB3}$  pin functions as RB3,  $\overline{\text{MCLR}}$  internally tied to VDD

bit 4  **$\overline{\text{CP}}$ :** Code Protection bit

1 = Code protection off

0 = Code protection on

bit 3 **WDTE:** Watchdog Timer Enable bit

1 = WDT enabled

0 = WDT disabled

bit 2-0 **FOSC2:FOSC0:** Oscillator Selection bits

000 = LP oscillator

001 = XT oscillator

010 = HS oscillator

011 = EC oscillator with RB4 function on RB4/OSC2/CLKOUT

100 = INTOSC with RB4 function on RB4/OSC2/CLKOUT

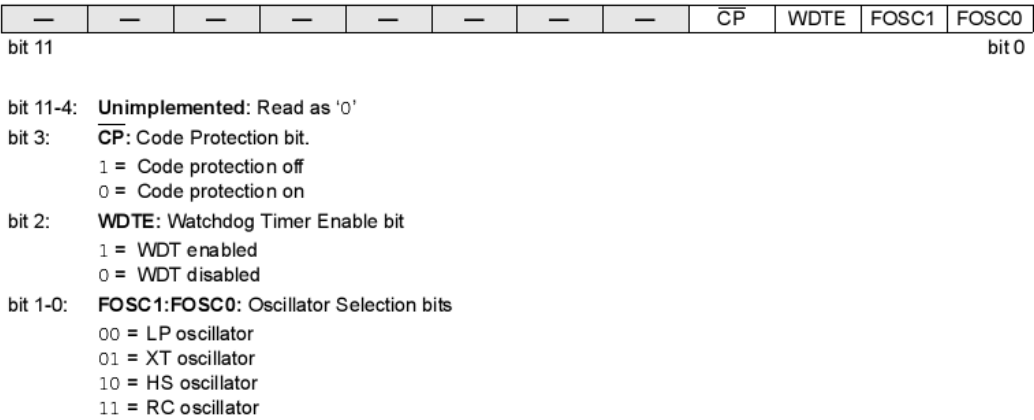
101 = INTOSC with CLKOUT function on RB4/OSC2/CLKOUT

110 = EXTRC with RB4 function on RB4/OSC2/CLKOUT

111 = EXTRC with CLKOUT function on RB4/OSC2/CLKOUT

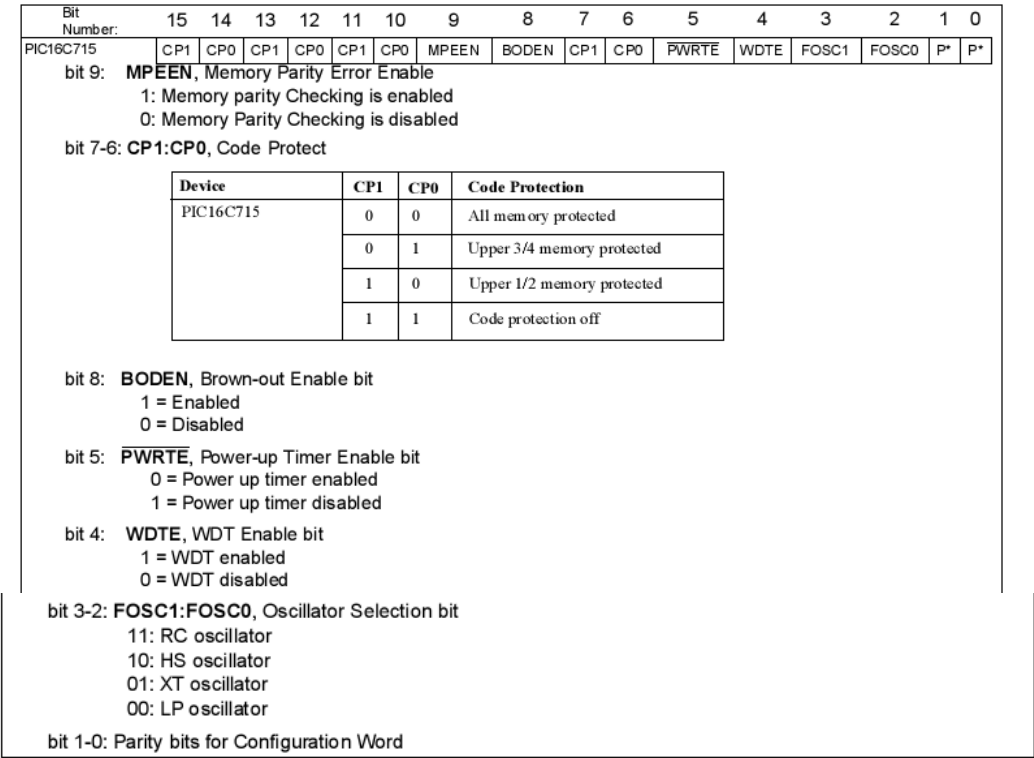


PIC16F57



PIC16C715

FIGURE 3-1: CONFIGURATION WORD BIT MAP



\* Parity bits are clocked in/out but not checked.

## PIC16F716

**REGISTER 3-1: CONFIGURATION WORD**

R/P-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1	U-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{CP}}$	—	—	—	—	—	BORV	BOREN	—	—	$\overline{\text{PWRTE}}$	WDTE	FOSC1	FOSC0
bit 13													bit 0

- bit 13  **$\overline{\text{CP}}$** : Flash Program Memory Code Protection bit<sup>(2)</sup>  
 1 = Code protection off  
 0 = All program memory code protected
- bit 12-8 **Unimplemented**: Read as '1'
- bit 7 **BORV**: Brown-out Reset Voltage bit  
 1 =  $V_{BOR}$  set to 4.0V  
 0 =  $V_{BOR}$  set to 2.5V
- bit 6 **BOREN**: Brown-out Reset Enable bit <sup>(1)</sup>  
 1 = BOR Reset enabled  
 0 = BOR Reset disabled
- bit 5-4 **Unimplemented**: Read as '1'
- bit 3  **$\overline{\text{PWRTE}}$** : Power-up Timer Enable bit<sup>(1)</sup>  
 1 = PWRT disabled  
 0 = PWRT enabled
- bit 2 **WDTE**: Watchdog Timer Enable bit  
 1 = WDT enabled  
 0 = WDT disabled
- bit 1-0 **FOSC1:FOSC0**: Oscillator Selection bits  
 11 = RC oscillator  
 10 = HS oscillator: High speed crystal/resonator on OSC2/CLKOUT and OSC1/CLKIN  
 01 = XT oscillator: Crystal/resonator on OSC2/CLKOUT and OSC1/CLKIN  
 00 = LP oscillator: Low power crystal on OSC2/CLKOUT and OSC1/CLKIN

## PIC16F62X

**REGISTER 3-1: CONFIGURATION WORD FOR PIC16F627/628 (ADDRESS: 2007h)**

CP1	CP0	CP1	CP0	—	CPD	LVP	BOREN	MCLRE	FOSC2	PWRTEN	WDTEN	FOSC1	FOSC0
bit 13													bit 0

bit 13-10 **CP1:CP0:** Code Protection bits <sup>(2)</sup>

**Code protection for 2K program memory**

11 = Program memory code protection off

10 = 0400h-07FFh code protected

01 = 0200h-07FFh code protected

00 = 0000h-07FFh code protected

**Code protection for 1K program memory**

11 = Program memory code protection off

10 = Program memory code protection off

01 = 0200h-03FFh code protected

00 = 0000h-03FFh code protected

bit 9 **Unimplemented:** Read as '1'

bit 8 **CPD:** Data Code Protection bit <sup>(3)</sup>

1 = Data memory code protection off

0 = Data memory code protected

bit 7 **LVP:** Low Voltage Programming Enable bit

1 = RB4/PGM pin has PGM function, Low Voltage Programming enabled

0 = RB4/PGM is digital input, HV on MCLR must be used for programming

bit 6 **BODEN:** Brown-out Detect Reset Enable bit <sup>(1)</sup>

1 = BOD Reset enabled

0 = BOD Reset disabled

bit 5 **MCLRE:** RA5/MCLR Pin Function Select bit

1 = RA5/MCLR pin function is MCLR

0 = RA5/MCLR pin function is digital input, MCLR internally tied to VDD

bit 3 **PWRTEN:** Power-up Timer Enable bit <sup>(1)</sup>

1 = PWRT disabled

0 = PWRT enabled

bit 2 **WDTEN:** Watchdog Timer Enable bit

1 = WDT enabled

0 = WDT disabled

bit 4, 1-0 **FOSC2:FOSC0:** Oscillator Selection bits <sup>(4)</sup>

111 = ER oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, Resistor on RA7/OSC1/CLKIN

110 = ER oscillator: I/O function on RA6/OSC2/CLKOUT pin, Resistor on RA7/OSC1/CLKIN

101 = INTRC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN

100 = INTRC oscillator: I/O function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN

011 = ExtCLK: I/O function on RA6/OSC2/CLKOUT pin, CLKIN on RA7/OSC1/CLKIN

010 = HS oscillator: High speed crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN

001 = XT oscillator: Crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN

000 = LP oscillator: Low power crystal on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN

**Note 1:** Enabling Brown-out Detect Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit PWRTEN. Ensure the Power-up Timer is enabled any time Brown-out Reset is enabled.

**2:** All of the CP1:CP0 pairs have to be given the same value to enable the code protection scheme listed. The entire program EEPROM will be erased if the code protection is reset.

**3:** The entire data EEPROM will be erased when the code protection is turned off. The calibration memory is not erased.

**4:** When MCLR is asserted in INTRC or ER mode, the internal clock oscillator is disabled.

# PIC16F627A/628A/648A

## REGISTER 3-1: CONFIGURATION WORD FOR PIC16F627A/PIC16F628A/PIC16F648A (ADDRESS: 2007h)

R/P-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{CP}}$	—	—	—	—	$\overline{\text{CPD}}$	LVP	BOREN	MCLR	FOSC2	$\overline{\text{PWRT}}\overline{\text{E}}$	WDTE	FOSC1	FOSC0
bit 13					bit 0								

- bit 13  $\overline{\text{CP}}$ : FLASH Program Memory Code Protection bit  
(PIC16F648A)  
1 = Code protection off  
0 = 0000h to 0FFFh code protected  
(PIC16F628A)  
1 = Code protection off  
0 = 0000h to 07FFh code protected  
(PIC16F627A)  
1 = Code protection off  
0 = 0000h to 03FFh code protected
- bit 12-9 Unimplemented: Read as '1'
- bit 8  $\overline{\text{CPD}}$ : Data Code Protection bit<sup>(2)</sup>  
1 = Data memory code protection off  
0 = Data memory code protected
- bit 7 LVP: Low Voltage Programming Enable bit  
1 = RB4/PGM pin has PGM function, low voltage programming enabled  
0 = RB4/PGM is digital I/O, HV on MCLR must be used for programming
- bit 6 BOREN: Brown-out Reset Enable bit<sup>(1)</sup>  
1 = BOR enabled  
0 = BOR disabled
- bit 5 MCLR: RA5/MCLR Pin Function Select bit  
1 = RA5/MCLR pin function is MCLR  
0 = RA5/MCLR pin function is digital I/O, MCLR internally tied to V<sub>DD</sub>
- bit 3  $\overline{\text{PWRT}}\overline{\text{E}}$ : Power-up Timer Enable bit<sup>(1)</sup>  
1 = PWRT disabled  
0 = PWRT enabled
- bit 2 WDTE: Watchdog Timer Enable bit  
1 = WDT enabled  
0 = WDT disabled
- bit 4, 1-0 FOSC<2:0>: Oscillator Selection bits<sup>(3)</sup>  
111 = RC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, Resistor & Capacitor on RA7/OSC1/CLKIN  
110 = RC oscillator: I/O function on RA6/OSC2/CLKOUT pin, Resistor & Capacitor on RA7/OSC1/CLKIN  
101 = INTOSC internal oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN  
100 = INTOSC internal oscillator: I/O function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN  
011 = EXTCLK: I/O function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN  
010 = HS oscillator: High speed crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN  
001 = XT oscillator: Crystal/resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN  
000 = LP oscillator: Low power crystal on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN

- Note** 1: Enabling Brown-out Reset does not automatically enable the Power-up Timer (PWRT).  
2: Only a Bulk Erase will reset the configuration word, including the CP bits.  
3: While MCLR is asserted in INTOSC mode, the internal clock oscillator is disabled.

## PIC16F8X

For PIC16F83/84/84A:

CP	CP	CP	CP	CP	CP	CP	CP	CP	CP	PWRTEN	WDTEN	FOSC1	FOSC0
----	----	----	----	----	----	----	----	----	----	--------	-------	-------	-------

FOR PIC16CR83/84:

CP	CP	CP	CP	CP	CP	DP	CP	CP	CP	PWRTEN	WDTEN	FOSC1	FOSC0
----	----	----	----	----	----	----	----	----	----	--------	-------	-------	-------

bit13

bit0

- bit 13-8,  
bit 6-4      **CP:** Code Protection bits<sup>(1)</sup>  
                 1 = Code protection off  
                 0 = Code protection on
- bit 7      For PIC16F83/84/84A:  
            **CP:** Code Protection bits<sup>(1)</sup>  
            1 = Code protection off  
            0 = Code protection on  
For PIC16CR83/84:  
            **DP:** Data Memory Code Protection bit  
            1 = Code protection off  
            0 = Data memory is code protected
- bit 3      **PWRTEN:** Power-up Timer Enable bit  
            1 = PWRT disabled  
            0 = PWRT enabled
- bit 2      **WDTEN:** Watchdog Timer Enable bit  
            1 = WDT enabled  
            0 = WDT disabled
- bit 1-0      **FOSC1:FOSC0:** Oscillator Selection bits  
            11 = RC oscillator  
            10 = HS oscillator  
            01 = XT oscillator  
            00 = LP oscillator

**Note 1:** All of the CP bits have to be given the same value to enable the code protection scheme listed.

## PIC16F7X7

- PIC16F737
- PIC16F747
- PIC16F767
- PIC16F777

### REGISTER 3-1: CONFIGURATION WORD 1 (2007h) REGISTER FOR PIC16F7X7

CP	CCPMX	RESV	-	-	BORV1	BORV0	BOREN	MCLRE	F0SC2	PWRTEN	WDTEN	F0SC1	F0SC0
bit 13													bit 0

- bit 13 **CP**: Flash Program Memory Code Protection bits  
1 = Code protection off  
0 = 0000h to 1FFFh code protected for 767,777 and 0000h to 0FFFh for 737,747 (all protected)
- bit 12 **CCPMX**:  
1 = CCP2 is on RC1  
0 = CCP2 is on RB3
- bit 11 **Reserved**: Set to '1' for normal operation
- bit 10-9 **Unimplemented**: Read as '1'
- bit 8-7 **BORV<1:0>**: Brown-out Reset Voltage bits  
11 = VBOR set to 2.0V  
10 = VBOR set to 2.7V  
01 = VBOR set to 4.2V  
00 = VBOR set to 4.5V
- bit 6 **BOREN**: Brown-out Reset Enable bit  
BOREN combines with BORSEN to control when BOR is enabled and how it is controlled  
BOREN:BORSEN  
11 = BOR enabled and always on  
10 = BOR enabled during operation and disabled during SLEEP by hardware  
01 = BOR controlled by software bit SBORSEN  
00 = BOR disabled
- bit 5 **MCLRE**: RE3/MCLR Pin Function Select bit  
1 = RE3/MCLR pin function is MCLR  
0 = RE3/MCLR pin function is digital input only, MCLR gated to '1'
- bit 3 **PWRTEN**: Power-up Timer Enable bit  
1 = PWRT disabled  
0 = PWRT enabled
- bit 2 **WDTEN**: Watchdog Timer Enable bit  
1 = WDT enabled  
0 = WDT disabled
- bit 4, 1-0 **F0SC2:F0SC0**: Oscillator Selection bits  
111 = EXTRC oscillator; CLKO function on RA6/OSC2/CLKO  
110 = EXTRC oscillator; Port I/O function on RA6/OSC2/CLKO  
101 = INTRC oscillator; CLKO function on RA6/OSC2/CLKO and Port I/O function on RA7/OSC1  
100 = INTRC oscillator; Port I/O function on RA7/OSC1 and RA6/OSC2/CLKO  
011 = EXTCLK; Port I/O function on RA6/OSC2/CLKO  
010 = HS oscillator  
001 = XT oscillator  
000 = LP oscillator

### REGISTER 3-2: CONFIGURATION WORD 2 (2008h) REGISTER FOR PIC16F7X7

-	-	-	-	-	-	-	BORSEN	-	-	-	-	IESO	FCMEN
bit 13													bit 0

- bit 13-7 **Unimplemented**: Read as '1'
- bit 6 **BORSEN**: Brown-out Reset Software Enable bit  
Refer to the BOREN bit in Configuration Word 1 (Register 3-1) for the function of this bit
- bit 5-2 **Unimplemented**: Read as '1'
- bit 1 **IESO**: Internal External Switch Over bit  
1 = Internal External Switch Over mode enabled  
0 = Internal External Switch Over mode disabled
- bit 0 **FCMEN**: Fail Clock Monitor Enable bit  
1 = Fail-Safe Clock Monitor enabled  
0 = Fail-Safe Clock Monitor disabled

## PIC16F87/88

**REGISTER 4-1: CONFIGURATION WORD 1 (2007h) REGISTER**

CP	CCPMX	DEBUG	WRT1	WRT0	CPD	LVP	BOREN	MCLRE	FOSC2	PWRTEN	WDTEN	FOSC1	FOSC0
bit 13													bit 0

- bit 13 **CP**: Flash Program Memory Code Protection bits  
1 = Code protection off  
0 = 0000h to 0FFFh code protected (all protected)
- bit 12 **CCPMX**: CCP Mux bit  
1 = CCP1 function on RB0  
0 = CCP1 function on RB3
- bit 11 **DEBUG**: In-Circuit Debugger Mode bit  
1 = In-Circuit Debugger disabled, RB6 and RB7 are general purpose I/O pins  
0 = In-Circuit Debugger enabled, RB6 and RB7 are dedicated to the debugger
- bit 10-9 **WRT1:WRT0**: Flash Program Memory Write Enable bits  
11 = Write protection off  
10 = 0000h to 00FFh write-protected, 0100h to 0FFFh may be modified by EECON control  
01 = 0000h to 07FFh write-protected, 0800h to 0FFFh may be modified by EECON control  
00 = 0000h to 0FFFh write-protected
- bit 8 **CPD**: Data EE Memory Code Protection bit  
1 = Code protection off  
0 = Data EE memory code-protected
- bit 7 **LVP**: Low-voltage Programming Enable bit  
1 = RB3/PGM pin has PGM function, Low-voltage Programming enabled  
0 = RB3 is digital I/O, HV on  $\overline{\text{MCLR}}$  must be used for programming
- bit 6 **BOREN**: Brown-out Reset Enable bit  
1 = BOR enabled  
0 = BOR disabled
- bit 5 **MCLRE**: RA5/ $\overline{\text{MCLR}}$  Pin Function Select bit  
1 = RA5/ $\overline{\text{MCLR}}$  pin function is  $\overline{\text{MCLR}}$   
0 = RA5/ $\overline{\text{MCLR}}$  pin function is digital I/O,  $\overline{\text{MCLR}}$  internally tied to VDD
- bit 3 **PWRTEN**: Power-up Timer Enable bit  
1 = PWRT disabled  
0 = PWRT enabled
- bit 2 **WDTEN**: Watchdog Timer Enable bit  
1 = WDT enabled  
0 = WDT disabled
- bit 4, 1-0 **FOSC2:FOSC0**: Oscillator Selection bits  
111 = EXTRC oscillator; CLK0 function on RA6/OSC2/CLKO  
110 = EXTRC oscillator; port I/O function on RA6/OSC2/CLKO  
101 = INTRC oscillator; CLK0 function on RA6/OSC2/CLKO  
100 = INTRC oscillator; port I/O function on RA6/OSC2/CLKO  
011 = EXTCLK; port I/O function on RA6/OSC2/CLKO  
010 = HS oscillator  
001 = XT oscillator  
000 = LP oscillator

**REGISTER 4-2: CONFIGURATION WORD 2 (2008h) REGISTER**

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	IESO	FCMEN
—	—	—	—	—	—	—	—	—	—	—	—		
bit 13													bit 0

- bit 13-2 Unimplemented: Read as '1'
- bit 1 **IESO**: Internal External Switch Over bit  
1 = Internal External Switch Over mode enabled  
0 = Internal External Switch Over mode disabled
- bit 0 **FCMEN**: Fail-Safe Clock Monitor Enable bit  
1 = Fail-Safe Clock Monitor enabled  
0 = Fail-Safe Clock Monitor disabled

## PIC16F87X

- PIC16F870
- PIC16F871
- PIC16F872
- PIC16F873
- PIC16F874
- PIC16F876
- PIC16F877

**REGISTER 3-1: CONFIG: CONFIGURATION WORD FOR PIC16F873/874/876/877  
(ADDRESS 2007h)**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/P-1	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
CP1	CP0	RESV	—	WRT	CPD	LVP	BODEN	CP1	CP0	PWRT $\overline{E}$	WDTE	FOSC1	FOSC0
bit 13							bit 0						

bit 13-12	<b>CP1:CP0: FLASH Program Memory Code Protection bits<sup>(2)</sup></b>
bit 5-4	<b>4 K Devices:</b> 11 = Code protection off 10 = 0F00h to 0FFFh code protected 01 = 0800h to 0FFFh code protected 00 = 0000h to 0FFFh code protected <b>8 K Devices:</b> 11 = Code protection off 10 = 1F00h to 1FFFh code protected 01 = 1000h to 1FFFh code protected 00 = 0000h to 1FFFh code protected
bit 11	<b>Reserved:</b> Set to '1' for normal operation
bit 10	<b>Unimplemented:</b> Read as '1'
bit 9	<b>WRT:</b> FLASH Program Memory Write Enable bit 1 = Unprotected program memory may be written to by EECON control 0 = Unprotected program memory may not be written to by EECON control
bit 8	<b>CPD:</b> Data EE Memory Code Protection bit 1 = Code protection off 0 = Data EE memory code protected
bit 7	<b>LVP:</b> Low Voltage ICSP Programming Enable bit 1 = RB3/PGM pin has PGM function, low voltage programming enabled 0 = RB3 is digital I/O, HV on MCLR must be used for programming
bit 6	<b>BODEN:</b> Brown-out Reset Enable bit <sup>(2)</sup> 1 = BOR enabled 0 = BOR disabled
bit 3	<b>PWRT<math>\overline{E}</math>:</b> Power-up Timer Enable bit 1 = PWRT disabled 0 = PWRT enabled
bit 2	<b>WDTE:</b> Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled
bit 1-0	<b>FOSC1:FOSC0:</b> Oscillator Selection bits 11 = RC oscillator 10 = HS oscillator 01 = XT oscillator 00 = LP oscillator

- Note** 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT), regardless of the value of bit  $\overline{PWRT\overline{E}}$ . Ensure the Power-up Timer is enabled any time Brown-out Reset is enabled.
- 2: All of the CP1:CP0 pairs have to be given the same value to enable the code protection scheme listed.



# PIC16F87XA

## REGISTER 3-1: CONFIGURATION WORD REGISTER

R/P-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1
CP	—	DEBUG	WRT1	WRT0	CPD	LVP	BOREN	—	—	PWRTEN	WDTEN	FOSC1	FOSC0

bit 13 bit 0

bit 13 **CP:** FLASH Program Memory Code Protection bit

(PIC16F877A/876A):

1 = Code protection off

0 = 0000h to 1FFFh code protected

(PIC16F874A/873A):

1 = Code protection off

0 = 0000h to 0FFFh code protected

1000h to 1FFFh wraps to 0000h to 0FFFh

bit 12 **Unimplemented:** Read as '1'

bit 11 **DEBUG:** Background Debugger Mode bit

1 = Background debugger functions not enabled

0 = Background debugger functional

bit 10-9 **WRT<1:0>:** FLASH Program Memory Write Enable bits

(PIC16F877A/876A):

11 = Write protection off

10 = 0000h to 00FFh write protected, 0100h to 1FFFh may be modified by EECON control

01 = 0000h to 07FFh write protected, 0800h to 1FFFh may be modified by EECON control

00 = 0000h to 0FFFh write protected, 1000h to 1FFFh may be modified by EECON control

(PIC16F874A/873A):

11 = Write protection off

10 = 0000h to 00FFh write protected, 0100h to 0FFFh may be modified by EECON control

01 = 0000h to 03FFh write protected, 0400h to 0FFFh may be modified by EECON control

00 = 0000h to 07FFh write protected, 0800h to 1FFFh may be modified by EECON control

bit 8 **CPD:** Data EE Memory Code Protection bit

1 = Code protection off

0 = Data EE memory code protected

bit 7 **LVP:** Low Voltage Programming Enable bit

1 = RB3/PGM pin has PGM function, low voltage programming enabled

0 = RB3 is digital I/O, HV on MCLR must be used for programming

bit 6 **BOREN:** Brown-out Reset Enable bit

1 = BOR enabled

0 = BOR disabled

bit 5-4 **Unimplemented:** Read as '1'

bit 3 **PWRTEN:** Power-up Timer Enable bit

1 = PWRT disabled

0 = PWRT enabled

bit 2 **WDTEN:** Watchdog Timer Enable bit

1 = WDT enabled

0 = WDT disabled

bit 1-0 **FOSC<1:0>:** Oscillator Selection bits

11 = RC oscillator

10 = HS oscillator

01 = XT oscillator

00 = LP oscillator

# REGISTER 3-2: CONFIG: CONFIGURATION WORD FOR PIC16F870/871/872 (ADDRESS 2007h)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/P-1	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
CP1	CP0	RESV	—	WRT	CPD	LVP	BODEN	CP1	CP0	PWRT $\overline{\text{E}}$	WDTE	FOSC1	FOSC0
bit 13													bit 0

bit 13-12	CP1:CP0: FLASH Program Memory Code Protection bits <sup>(2)</sup>
bit 5-4	11 = Code protection off 10 = Not supported 01 = Not supported 00 = 0000h to 07FFh code protected
bit 11	Reserved: Set to '1' for normal operation
bit 10	Unimplemented: Read as '1'
bit 9	WRT: FLASH Program Memory Write Enable bit 1 = Unprotected program memory may be written to by EECON control 0 = Unprotected program memory may not be written to by EECON control
bit 8	CPD: Data EE Memory Code Protection bit 1 = Code protection off 0 = Data EE memory code protected
bit 7	LVP: Low Voltage ICSP Programming Enable bit 1 = RB3/PGM pin has PGM function, low voltage programming enabled 0 = RB3 is digital I/O, HV on MCLR must be used for programming
bit 6	BODEN: Brown-out Reset Enable bit <sup>(2)</sup> 1 = BOR enabled 0 = BOR disabled
bit 3	PWRT $\overline{\text{E}}$ : Power-up Timer Enable bit 1 = PWRT disabled 0 = PWRT enabled
bit 2	WDTE: Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled
bit 1-0	FOSC1:FOSC0: Oscillator Selection bits 11 = RC oscillator 10 = HS oscillator 01 = XT oscillator 00 = LP oscillator

- Note** 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT), regardless of the value of bit  $\overline{\text{PWRT}}\text{E}$ . Ensure the Power-up Timer is enabled any time Brown-out Reset is enabled.
- 2: All of the CP1:CP0 pairs have to be given the same value to enable the code protection scheme listed.

## PIC16F91X

The PIC16F91X has several configuration bits. These bits can be programmed (reads '0'), or left unchanged (reads '1'), to select various device configurations.

### REGISTER 4-1: CONFIG – CONFIGURATION WORD (ADDRESS:2007h)

U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	DEBUG	FCMEN	IESO	BODEN1	BODEN0	CPD	CP	MCLRRE	PWRTRE	WDTE	FOSC2	FOSC1	FOSC0	
bit 13														bit 0

- bit 13 Unimplemented: Read as '1'
- bit 12 **DEBUG**: In-Circuit Debugger Mode bit  
 1 = In-Circuit Debugger disabled, RB6 and RB7 are general purpose I/O pins  
 0 = In-Circuit Debugger enabled, RB6 and RB7 are dedicated to the debugger
- bit 11 **FCMEN**: Fail-Safe Clock Monitor Enable bit  
 1 = Fail-Safe Clock Monitor enabled  
 0 = Fail-Safe Clock Monitor disabled
- bit 10 **IESO**: Internal-External Switch Over bit  
 1 = Internal External Switch Over mode enabled  
 0 = Internal External Switch Over mode disabled
- bit 9-8 **BODEN<1:0>**: Brown-out Reset Enable bits  
 11 = BOD enabled and SBODEN bit disabled  
 10 = BOD enabled while running and disabled in Sleep. SBODEN bit disabled.  
 01 = SBODEN in the PCON register controls BOD function  
 00 = BOD and SBODEN disabled
- bit 7 **CPD**: Code Protection Data bit  
 1 = Data memory is not protected  
 0 = Data memory is external read protected
- bit 6 **CP**: Code Protection bit  
 1 = Program memory is not code-protected  
 0 = Program memory is external read and write protected
- bit 5 **MCLRRE**: MCLR Pin Function Select bit  
 1 = MCLR pin is MCLR function and weak internal pull-up is enabled  
 0 = MCLR pin is alternate function, MCLR function is internally disabled
- bit 4 **PWRTRE**: Power-up Timer Enable bit<sup>(1)</sup>  
 1 = PWRT disabled  
 0 = PWRT enabled
- bit 3 **WDTE**: Watchdog Timer Enable bit  
 1 = WDT enabled  
 0 = WDT disabled and can be enabled using SWDTEN in the WDTCON register
- bit 2-0 **FOSC<2:0>**: Oscillator Selection bits  
 000 = LP oscillator: Low-power crystal on OSC1/CLKI/T1OSI/RA7 and OSC2/CLKO/T1OSO/RA6  
 001 = XT oscillator: Crystal/resonator on OSC1/CLKI/T1OSI/RA7 and OSC2/CLKO/T1OSO/RA6  
 010 = HS oscillator: High-speed crystal/resonator on OSC1/CLKI/T1OSI/RA7 and OSC2/CLKO/T1OSO/RA6  
 011 = EC: I/O function on OSC2/CLKO/T1OSO/RA6, CLKIN on RA5/T1CKI/OSC1/CLKIN  
 100 = INTOSCIO oscillator: I/O function on OSC2/CLKO/T1OSO/RA6, I/O function on OSC1/CLKI/T1OSI/RA7  
 101 = INTOSC oscillator: CLKOUT function on OSC2/CLKO/T1OSO/RA6, I/O function on OSC1/CLKI/T1OSI/RA7  
 110 = EXTRCIO oscillator: I/O function on OSC2/CLKO/T1OSO/RA6, RC on OSC1/CLKI/T1OSI/RA7  
 111 = EXTRC oscillator: CLKOUT function on OSC2/CLKO/T1OSO/RA6, RC on OSC1/CLKI/T1OSI/RA7

\*PIC12F629 \*PIC16F630

\*  
 \*PIC12F675 \*PIC16F676

**REGISTER 3-1: CONFIGURATION WORD FOR PIC12F629/75/PIC16F630/76**

R/P-1	R/P-1	U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
BG1	BG0	—	—	—	CPD	CP	BODEN	MCLRE	PWRTÉ	WDTE	FOSC2	FOSC1	FOSC0
bit 13					bit 0								

- bit 13-12 **BG<1:0>**: Band Gap Calibration bits<sup>(2)</sup>  
00 = Lowest band gap voltage  
...  
11 = Highest band gap voltage
- bit 11-9 **Unimplemented**: Read as '0'
- bit 8 **CPD**: Code Protection Data bit  
1 = Data memory is not protected  
0 = Data memory is external read protected
- bit 7 **CP**: Code Protection bit  
1 = Program memory is not code-protected  
0 = Program memory is code-protected
- bit 6 **BODEN**: Brown-out Detect Reset Enable bit<sup>(1)</sup>  
1 = BOD Reset enabled  
0 = BOD Reset disabled
- bit 5 **MCLRE**: MCLR Pin Function Select bit  
1 = MCLR pin is MCLR function  
0 = MCLR pin is alternate function, MCLR function is internally disabled
- bit 4 **PWRTÉ**: Power-up Timer Enable bit<sup>(1)</sup>  
1 = PWRT disabled  
0 = PWRT enabled
- bit 3 **WDTE**: Watchdog Timer Enable bit  
1 = WDT enabled  
0 = WDT disabled
- bit 2-0 **FOSC<2:0>**: Oscillator Selection bits<sup>(3)</sup>  
000 = LP oscillator: Low-power crystal on GP5/T1CKI/OSC1/CLKIN and GP4/T1G/OSC2/CLKOUT  
001 = XT oscillator: Crystal/resonator on GP5/T1CKI/OSC1/CLKIN and GP4/T1G/OSC2/CLKOUT  
010 = HS oscillator: High-speed crystal/resonator on GP5/T1CKI/OSC1/CLKIN and GP4/T1G/OSC2/CLKOUT  
011 = EC: I/O function on GP4/T1G/OSC2/CLKOUT, CLKIN on GP5/T1CKI/OSC1/CLKIN  
100 = INTOSC oscillator: I/O function on GP4/T1G/OSC2/CLKOUT, I/O function on GP5/T1CKI/OSC1/CLKIN  
101 = INTOSC oscillator: CLKOUT function on GP4/T1G/OSC2/CLKOUT, I/O function on GP5/T1CKI/OSC1/CLKIN  
110 = RC oscillator: I/O function on GP4/T1G/OSC2/CLKOUT, RC on GP5/T1CKI/OSC1/CLKIN  
111 = RC oscillator: CLKOUT function on GP4/T1G/OSC2/CLKOUT, RC on GP5/T1CKI/OSC1/CLKIN
- Note 1:** Enabling Brown-out Detect Reset Enable does not automatically enable the Power-up Timer Enable (PWRTÉ).
- 2:** The Band Gap Calibration bits must be read and preserved, then replaced by the user during any bulk erase operation.
- 3:** GP4 and GP5 apply to PIC12F629/675 only. For PIC16F630/676, use RA4 and RA5, respectively.

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown