REGISTER 3-1: CONFIGURATION WORD REGISTER

R/P-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1
CP	—	DEBUG	WRT1	WRT0	CPD	LVP	BOREN	—	—	PWRTEN	WDTEN	FOSC1	FOSC0
bit 13													bit 0

bit 13 **CP:** FLASH Program Memory Code Protection bit
(PIC16F877A/876A):
1 = Code protection off
0 = 0000h to 1FFFh code protected
(PIC16F874A/873A):
1 = Code protection off
0 = 0000h to 0FFFh code protected
1000h to 1FFFh wraps to 0000h to 0FFFh

bit 12 **Unimplemented:** Read as '1'

bit 11 **DEBUG:** Background Debugger Mode bit
1 = Background debugger functions not enabled
0 = Background debugger functional

bit 10-9 **WRT<1:0>:** FLASH Program Memory Write Enable bits
(PIC16F877A/876A):
11 = Write protection off
10 = 0000h to 00FFh write protected, 0100h to 1FFFh may be modified by EECON control
01 = 0000h to 07FFh write protected, 0800h to 1FFFh may be modified by EECON control
00 = 0000h to 0FFFh write protected, 1000h to 1FFFh may be modified by EECON control
(PIC16F874A/873A):
11 = Write protection off
10 = 0000h to 00FFh write protected, 0100h to 0FFFh may be modified by EECON control
01 = 0000h to 03FFh write protected, 0400h to 0FFFh may be modified by EECON control
00 = 0000h to 07FFh write protected, 0800h to 1FFFh may be modified by EECON control

bit 8 **CPD:** Data EE Memory Code Protection bit
1 = Code protection off
0 = Data EE memory code protected

bit 7 **LVP:** Low Voltage Programming Enable bit
1 = RB3/PGM pin has PGM function, low voltage programming enabled
0 = RB3 is digital I/O, HV on MCLR must be used for programming

bit 6 **BOREN:** Brown-out Reset Enable bit
1 = BOR enabled
0 = BOR disabled

bit 5-4 **Unimplemented:** Read as '1'

bit 3 **PWRTEN:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 2 **WDTEN:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC<1:0>:** Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

REGISTER 3-2: CONFIG: CONFIGURATION WORD FOR PIC16F870/871/872 (ADDRESS 2007h)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/P-1	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
CP1	CP0	RESV	—	WRT	CPD	LVP	BODEN	CP1	CP0	$\overline{\text{PWRTE}}$	WDTE	F0SC1	F0SC0
bit 13													bit 0

bit 13-12, bit 5-4 **CP1:CP0:** FLASH Program Memory Code Protection bits[2]
- 11 = Code protection off
- 10 = Not supported
- 01 = Not supported
- 00 = 0000h to 07FFh code protected

bit 11 **Reserved:** Set to '1' for normal operation

bit 10 **Unimplemented:** Read as '1'

bit 9 **WRT:** FLASH Program Memory Write Enable bit
- 1 = Unprotected program memory may be written to by EECON control
- 0 = Unprotected program memory may not be written to by EECON control

bit 8 **CPD:** Data EE Memory Code Protection bit
- 1 = Code protection off
- 0 = Data EE memory code protected

bit 7 **LVP:** Low Voltage ICSP Programming Enable bit
- 1 = RB3/PGM pin has PGM function, low voltage programming enabled
- 0 = RB3 is digital I/O, HV on $\overline{\text{MCLR}}$ must be used for programming

bit 6 **BODEN:** Brown-out Reset Enable bit[2]
- 1 = BOR enabled
- 0 = BOR disabled

bit 3 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit
- 1 = PWRT disabled
- 0 = PWRT enabled

bit 2 **WDTE:** Watchdog Timer Enable bit
- 1 = WDT enabled
- 0 = WDT disabled

bit 1-0 **FOSC1:FOSC0:** Oscillator Selection bits
- 11 = RC oscillator
- 10 = HS oscillator
- 01 = XT oscillator
- 00 = LP oscillator

Note 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT), regardless of the value of bit $\overline{\text{PWRTE}}$. Ensure the Power-up Timer is enabled any time Brown-out Reset is enabled.

2: All of the CP1:CP0 pairs have to be given the same value to enable the code protection scheme listed.