

# Phase-shift generation and monitoring by a simple circuit

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A simple circuit for generating phase shifts along with a monitoring scheme is described. The circuit reported here produces a squarewave signal with fixed phase shift relative to the incoming signal. The amount of this phase shift can be monitored by the input voltage of a voltage-controlled oscillator. By varying the free-running frequency of the voltage-controlled oscillator the phase shift of the output signal can be varied for a range of  $0^\circ$ – $180^\circ$  corresponding to a voltage change of  $-1.2$  to  $1.2$  V. The produced phase shift is a linear function of the voltage setting that can be controlled with a high accuracy. The reported circuit can be used in phase sensitive detection systems operating based on a shifted squarewave reference signal. © 1996 American Institute of Physics. [S0034-6748(96)04304-3]

## I. INTRODUCTION

In many applications such as lock-in amplifiers a phase shifter is required in order to produce a reference triggering input signal.<sup>1,2</sup> The first consideration may be the use of a simple RC circuit to shift the phase. There are two major problems in using such circuits with the discrete elements. The first is that the relationship between phase shift and component values is nonlinear, and the second concern is that defining the precise value of the phase shift requires additional equipment.

An alternative solution is the use of a phase sensitive element triggered by a phase-coupled input signal that is described in this article. Here, the phase shifting is accomplished in a closed loop by an active phase locked loop (PLL).<sup>3,4</sup> The components of the loop are a phase detector, low pass filter, and a voltage-controlled oscillator (VCO). In order to monitor the produced phase shift, the output voltage of the phase shifter circuit was digitized by an analog to digital converter (A/D).

## II. CIRCUIT DESCRIPTION

The block diagram of the proposed circuit is shown in Fig. 1. When a square-wave input signal with frequency of  $f_i$  and phase  $\theta_i$  is fed into the X terminal, after the transient state, the VCO output (Y) has the same frequency that may have a phase difference with the other input X. The magnitude of the phase shift is directly related to the  $(f_i - f_0)$ , where  $f_0$  is the free running frequency of the PLL, so it can be shown

$$\Delta\theta = \frac{\pi}{2} - \frac{(f_i - f_0)}{K_0 \cdot K_d \cdot A \cdot f_0}, \quad (1)$$

where  $\Delta\theta$  is the phase difference between the input and the output signals of the VCO,  $K_0$  is the conversion coefficient of the VCO,  $K_d$  is the conversion coefficient of the phase detector (PD), and  $A$  is the gain of the loop amplifier. If  $K_0$ ,  $K_d$ ,  $f_i$ , and  $A$  remain constant during the operation, then by changing  $f_0$  we can generate an appropriate phase shift  $\Delta\theta$ .

In PLL there is another relationship between the input voltage and the output frequency of the VCO, which can be written as

$$f_i - f_0 = -K_0 \cdot f_0 \cdot V, \quad (2)$$

where  $V$  is the input voltage of the VCO. By substituting Eq. (2) into Eq. (1) we obtain a linear relationship between the input voltage of the VCO and the phase difference such as

$$\Delta\theta = \frac{\pi}{2} \left( 1 + \frac{2V}{\pi \cdot K_d \cdot A} \right). \quad (3)$$

Hence one can monitor the phase shift by measuring the input of the VCO ( $V$ ). The given calculations are only valid for the lock condition of the PLL. The dynamic parameters of the loop filter determine the natural frequency of the PLL and the transient response of it. In the lock situation, however, the transfer function of the loop filter can be assumed to be equal to unity, because the transient condition has been completed. The natural frequency of the PLL shows the maximum operating frequency in which the VCO phase jitters is reduced by the loop specification.<sup>5</sup> This frequency can be controlled by the dynamic parameters of the loop filter and above the natural frequency of the PLL the phase accuracy is spoiled by the VCO phase jitters.

Figure 2 shows the schematic diagram of the proposed circuit for the phase shifting and monitoring. The main components of this circuit are LM565 as PLL, LM311 as a comparator, and an 8-bit analog to digital converter (ADC). We have used the comparator in order to show the lock condi-

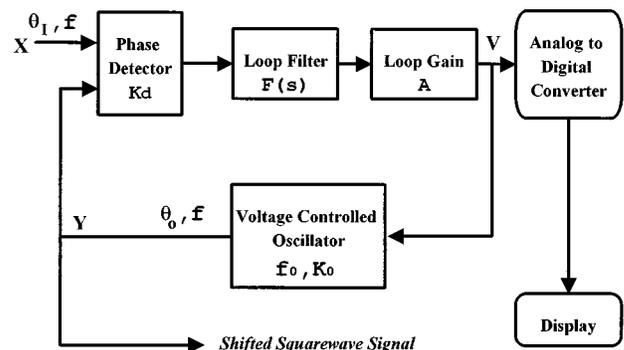


FIG. 1. Block diagram of the phase-shift generator.

tion. The output of the compactor was remaining low at locked condition that could be indicated by a light emitting diode (LED).

The parameter  $K_d$  in Eq. (3) can be defined from the PLL data sheet or it can be determined experimentally. For the value of  $K_0=0.53 [V^{-1}]$  and  $A.K_d=0.725 [V/rad]$  that are derived from the data sheet, Eq. (3) becomes

$$\Delta\theta=90(1+0.878V), \quad (4)$$

where  $V$  is equal to the voltage difference between the pins 6 and 7 of the LM565, and  $\Delta\theta$  is obtained in degrees. To check this relation experimentally, we have measured the variation of the phase difference with respect to the output voltage (for a constant  $f_i$ ) by changing  $f_0$  many times. With a regression we have found the empirical relation such as

$$\Delta\theta=90.4(1+0.875V). \quad (5)$$

The variation of the phase difference versus voltage  $V$  (output voltage of the amplifier  $U2$ ) is plotted in Fig. 3. As can be seen from Eqs. (4) and (5) there is a good agreement between the theory and experiment.

As far as calibrating the system, the relation between the phase shift  $\Delta\theta$  and voltage  $V$  can be obtained by performing several measurements and plotting the best calibration line by using the least square method, Eq. (5). Due to existing constructional differences in integrated circuit manufacturing, the obtained calibration line is only valid for a certain PLL chip.

However, it can be seen from Eq. (3) that for the precise measurement of the phase shift by the variation of the output voltage of the VCO, the conversion coefficient of the phase detector ( $K_0$ ) and the gain of the loop amplifier ( $A$ ) must be known exactly. The interesting feature of this scheme is that the relationship between the phase shift and the output volt-

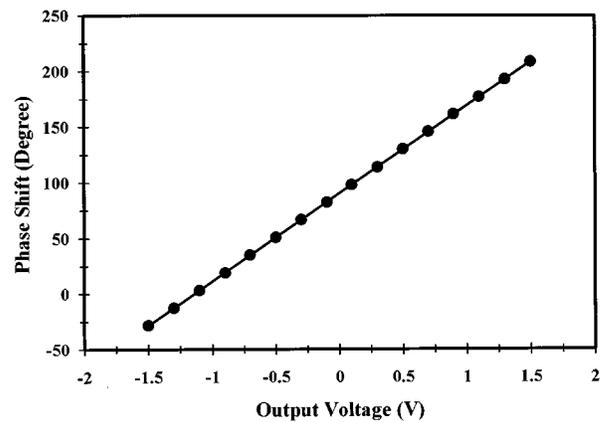


FIG. 3. Behavior of the phase shift vs the output voltage of the PLL.

age of the VCO is independent of the conversion coefficient of the VCO ( $K_0$ ), see Eq. (3). This is very important because both  $K_d$  and  $A$  can be determined by a separate circuit out of the PLL chip. Therefore, the values of  $K_d$  and  $A$  can be figured precisely. In this way we can use Eq. (3) for the phase shift measurement without needing further calibration.

In order to monitor the phase shift, the output voltage  $V$  was digitized by an 8-bit A/D (ADC0804), see Fig. 2. As can be seen in Fig. 2, the conversion process automatically proceeded by tying interrupt (INTR) and write (WR) pins together, so in this way, we have a continuous conversion. The variation of  $V$  is, for example, from 0 to 1.2 V. This range of variation corresponds to a  $90^\circ$  phase shift, so it has a resolution of 4.6 mV for  $V$  and as a result  $0.36^\circ$  for the phase shift. The resolution, however, can be improved considerably by using a 12-bit A/D.

With a potentiometer we can set the frequency  $f_0$  so that

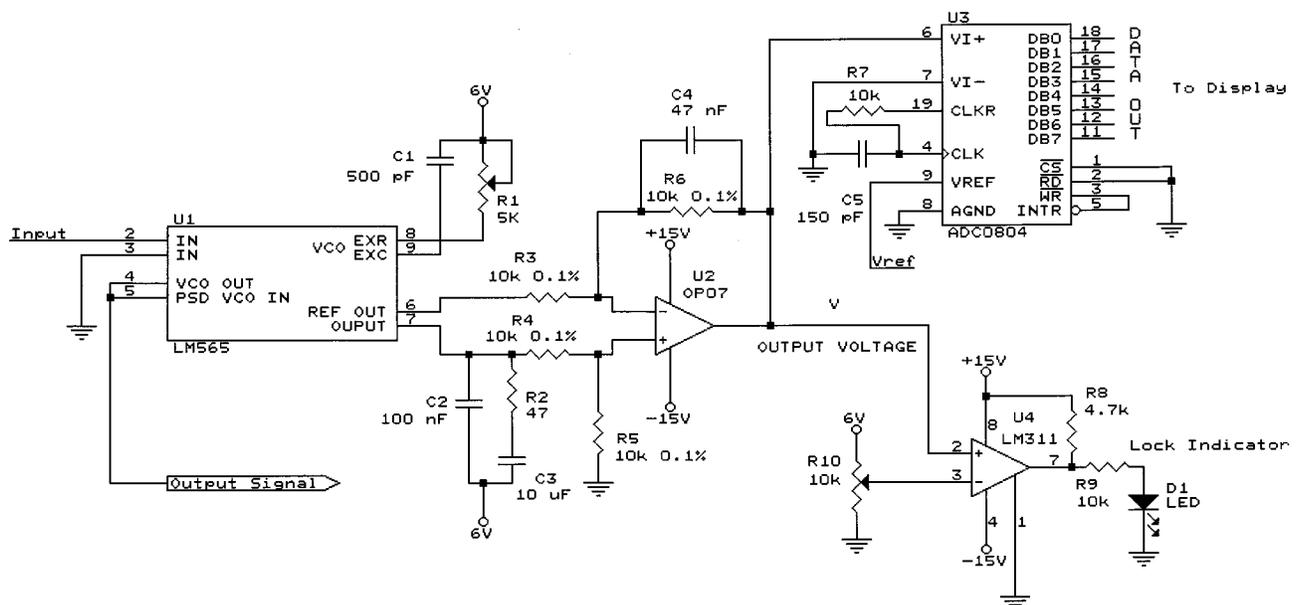


FIG. 2. Schematic representation of the phase-shift generator. Input signal is fed into the PSD of the PLL and the shifted signal can be obtained from the VCO output of the PLL. Amplified output voltage of the PSD monitors the amount of the phase shift.

the appropriate voltage is monitored on the display. Since relative error of an ADC for low output numbers is very high, it is reasonable to use a lower reference voltage for exploiting the maximum output range of A/D in order to reduce the relative error. For this purpose an auto-ranging DMM seems to be useful.

In the case that a reference square-wave signal with an appropriate phase shift relative to the input signal is needed, the circuit reported here is useful. There are applications for such a circuit in the design of lock-in amplifiers or other electronic instruments that require a shifted square-wave reference signal. Most of the sampling and averaging devices that work base on a phase detection method also require such a reference triggering signal. Another application of this scheme is in the phase-tracking lock-in amplifiers.<sup>1</sup> This can be accomplished by adding a voltage to the input voltage of the VCO ( $V$ ) for changing free-running frequency of the VCO. The obtained scheme can be named as a voltage-controlled phase shifter.

### III. CONCLUSIONS

The advantages of the reported system are the circuit simplicity, reliability, sensitivity, and the fact that the phase shift can be monitored easily and controlled precisely. Another feature of the circuit is that the locking position of the system can be checked for the case of different incoming signals. In summary, the preliminary results obtained for the circuit are satisfactory and the next goal is to implement it in a lock-in amplifier.

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<sup>3</sup>P. K. Dixon and L. Wu, *Rev. Sci. Instrum.* **60**, 3329 (1989).

<sup>4</sup>P. Shakkottai, E. Y. Kwack, and L. H. Back, *Rev. Sci. Instrum.* **60**, 3081 (1989).

<sup>5</sup>W. R. Robins, *Phase Noise in Signal Sources: Theory and Applications*, IEE Telecommunication Series 9 (Peter Peregrinus, London, 1982).