A rail-to-rail DC-enhanced adaptive biased fully differential OTA

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Abstract— **In this paper a novel rail-to-rail fully differential operational transconductance amplifier (OTA) working at low-supply voltages (1.5V) with reduced consumption and showing high DC gain is presented. An adaptive biasing circuit allows to obtain low stand-by power dissipation (lower than 0.19 mW in the rail-to-rail version), while the high DC gain (over 80 dB) is ensured by a positive feedback. The circuit, designed in a standard CMOS integrated technology (AMS 0.35 µm), has a 40 V/µs slew-rate for a capacitive load of 15 pF. The calculated values of two quality factors, named $FOM_{S/L}$ in the literature, show the validity of the proposed OTA.**

I. INTRODUCTION

The reduction of supply voltage makes difficult to implement efficient analog functions, so novel circuit architectures have to be developed [1-4]. The values of the current sources inside the amplifiers are the main responsible of quiescent power dissipation. Adaptive biasing technique boosts the bias current of the input differential pair when large signals are applied, so increasing circuit dynamic characteristics without affecting stand-by dissipation [5-12].

In this paper we propose a novel rail-to-rail fully differential OTA, showing low-voltage low-power characteristics, where DC gain has been enhanced by a suitable technique which increases the output impedance of the OTA input stage through a positive feedback [13-14]. The proposed OTA has been developed in a standard *CMOS* technology (AMS 0.35 µm), in *nMOS*, *pMOS* and rail-to-rail versions, showing very good characteristics. In the following sections, the OTA design techniques, the amplifier structure and the main simulation results are reported.

II. DESIGN TECHNIQUE STEPS

In the following we will describe the design steps followed in the development of the proposed OTA.

a. OTA topology choice

In order to obtain a fully differential characteristic from a relatively simple circuitry architecture, a classical symmetrical OTA structure has been considered (see Figure 1).

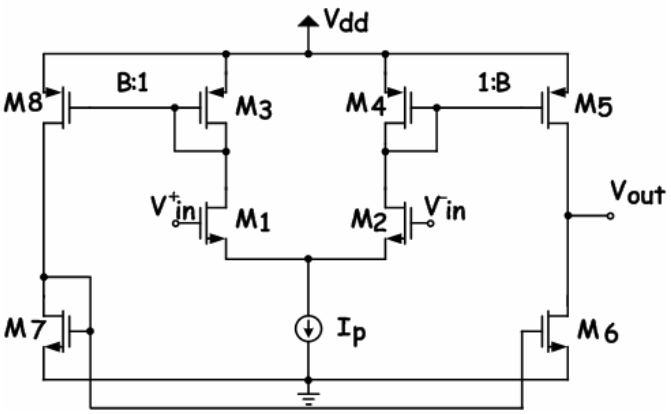

Fig. 1 Symmetrical OTA

As reported in the literature [15], in order to enhance the OTA slew rate *SR* (so improving the amplifier performance) without changing the gain-bandwidth *GBW*, biasing current must be increased but this needs a power consumption enhancement. For this reasons, the use of the adaptive biasing technique helps to reduce stand-by power without degrading the circuit dynamic performances.

b. Adaptive Biased OTA

In the literature, many adaptive biasing circuits, which add current at the circuit input stage only if a differential input is applied, have been proposed. One of these is based on the well known current subtractor proposed in [7] and shown in Figure 2. In this work, it has been applied to the symmetrical OTA of Figure 1. The current given by the subtractor is equal to:

$$I_p + A\left|I_2 - I_1\right|, \tag{1}$$

where the gain current *A* (considering Figure 2) is equal to:

$$A = \frac{(W/L)_4}{(W/L)_{1,2,3}}. \tag{2}$$

The output current I_{out} and the bias current I_p are related together according to the following equation (see Figure 3):

$$I_{out} = B(I_1 - I_2) = \frac{BI_p(e^{V_{in}/nV_T} - 1)}{(1+A) - (A-1)e^{V_{in}/nV_T}} \quad (3)$$

and, in the case of unitary gain *B* between output mirrors, for *A* typically in the range 0-0.9, the output maximum current is $\frac{I_p}{1-A}$. If *A*=0.9, the output current and, consequently, *SR* increase by a factor of 10.

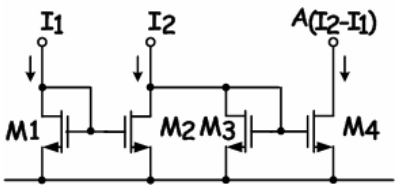

Fig. 2 Current subtractor

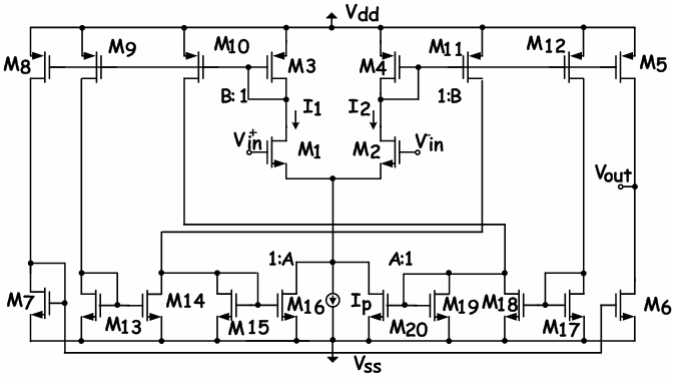

Fig. 3 Symmetrical OTA with adaptive biasing

c. Fully differential solution

A fully differential version of the proposed OTA has been developed through the elimination of the diode connection in *M7* transistor. A *CMFB* error amplifier has been added (see in Figure 7, R_1, R_2, M_{21}, M_{22}, M_{25}, M_{26}, I_{P1}, V_{ref}).

d. DC gain enhancement technique

By placing a negative resistance R_n in parallel with the output resistance of the amplifier (see Figure 4), the voltage gain is equal to [14]:

$$A_V = \frac{V_0}{V_{in}} = \frac{-g_{m1}}{g_{ds1} + 1/R + 1/R_n}. \quad (4)$$

If the following relation is satisfied :

$$\frac{1}{R_n} = -\left(\frac{1}{R}\right) + g_{ds1}, \quad (5)$$

the voltage gain is ideally infinite and it is possible to obtain a DC gain enhancement also for low-voltage applications. This methodology can be applied to the symmetrical OTA according to the topology shown in Figure 5, where the gates of *M23* and *M24* are connected to the drains of *M3* and *M4*. In this manner, at *A* and *B* nodes, a parallel resistance ($1/g_{m23,24}$) has been added. Transistors *M1*,*M2*,*M23*,*M24* constitute a positive feedback loop, where the direct path is characterized by A_d voltage gain and the feedback loop, formed by *M23*, *M1* and *M3* (*M24*, *M2* e *M4*), has a gain equal to β. The overall gain is given by :

$$A = \frac{A_d}{1 - A_d\beta} = \frac{A_d}{1 - G_{loop}}, \quad (6)$$

where G_{loop} is the loop gain equal to $A_d\beta$. The gain A_d is equal to :

$$A_d = \frac{g_{m1}}{g_{m3} + g_{ds23} + g_{ds3} + g_{ds1}}. \quad (7)$$

In order to calculate the loop gain G_{loop}, the input voltage has to be grounded and a signal has to be forced in an arbitrary node inside the same loop. G_{loop} is the ratio between the signal processed by the loop and the forced signal. Figure 6 shows the feedback branch structure. From the small-signal analysis we can write:

$$G_{loop} = \frac{V_{out}}{V_{in}} = \frac{g_{m23}}{g_{m3} + g_{ds23} + g_{ds3} + g_{ds1}}. \quad (8)$$

From eq.(8) we have that G_{loop} is lower than 1 (so stability in assured) if g_{m3} is close to g_{m23}. In this case, since the overall gain *A* can be expressed as:

$$A = \frac{g_{m1}}{g_{m3} - g_{m23} + g_{ds23} + g_{ds3} + g_{ds1}} \approx \frac{g_{m1}}{g_{m3} - g_{m23}} \quad (9)$$

a condition on g_{m3} and g_{m23} values can be deduced. In particular, in order to avoid that the gain *A* becomes infinite or changes its sign, g_{m3} value has been designed lower than 94% of g_{m23} value.

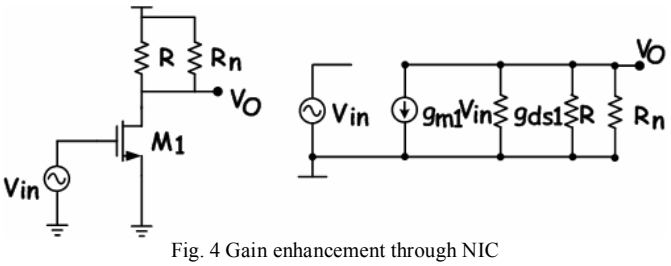

Fig. 4 Gain enhancement through NIC
(left: considered architecture; right: small-signal equivalent circuit)

III. COMPLETE AMPLIFIER ARCHITECTURE

The complete amplifier architecture, implemented in its *nMOS*, *pMOS* and rail-to-rail versions, according to the type of the input transistors, is described in the following.

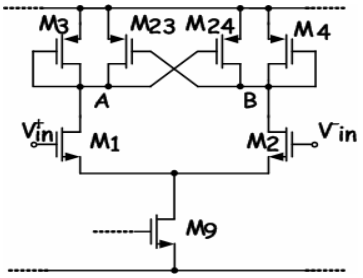

Fig. 5 Negative compensated OTA

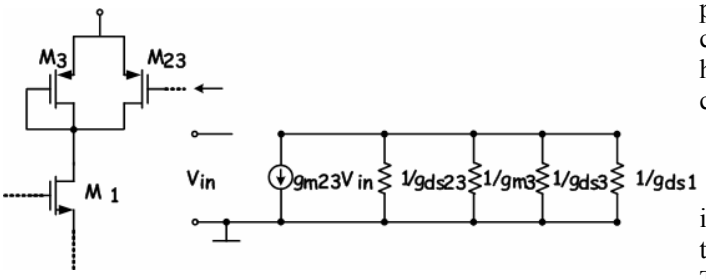

Fig. 6 Feedback branch structure
(left: considered architecture; right: small-signal equivalent circuit)

1. N-MOS OTA architecture

The designed *nMOS* version adaptive-biased DC-enhanced fully differential symmetrical OTA is shown in Figure 7. *M1-M8* constitute the transistor of the original symmetrical OTA, while adaptive biasing is formed by *M13-M16* and *M17-M20* current subtractors and by *M3-M9, M3-M10, M4-M11* and *M4-M12* current mirrors. Transistors *M23* and *M24* allows to perform the DC enhancement, while *R1,R2* (1MΩ valued), *M21, M22, M25*, *M26,* I_{p1} and V_{ref} form the common mode feedback (CMFB) circuit.

2. N-MOS OTA stability

For the amplifier compensation it has not been applied a classical Miller compensation because the right half plane zero has not been nulled but has been designed at a frequency close to that related to the non-dominant pole, so to benefit of the lead effect. The choice of C_M=3 pF and R_M= 40 kΩ allows to have a negative real part zero, so to have a partial compensation of non dominant pole effects on module and phase response. It can be demonstrated that the dominant and first non-dominant pole are given respectively by:

$$f_{p1} = \frac{1}{2\pi g_{m5} R_i R_u C_m}, \quad f_{p2} \approx \frac{g_{m5}}{2\pi C_u}, \tag{10}$$

being C_u the second-stage output capacitance, R_i the output resistance of the differential stage and R_u that at amplifier output while zero occurs at frequency:

$$f_z = \frac{g_{m5}}{2\pi C_m \left(R_m - \frac{1}{g_{m5}} \right)}, \tag{11}$$

so, knowing the operative values of conductances and transconductances of the main transistors, stability can be easily obtained. Simulations confirm that the presence of positive feedback loops in the circuit does not introduce significant latching and stability problems.

3. Rail-to-Rail Configuration

We have designed the *pMOS* version of the amplifier (through the implementation of the complementary circuit of the *nMOS* OTA) and, then, the rail-to-rail configuration placing in parallel the *nMOS* and *pMOS* stages. This latter circuit has the complete input and output dynamic range, a higher Slew-Rate (*SR*) and the complete common-mode control, even if stand-by power dissipation is higher.

IV. Simulation Results

The three designed OTA topologies have been simulated in a standard *CMOS* technology (*AMS* 0.35μm), having threshold voltages of 0.47V (nMOS) and -0.62V (pMOS). The circuits have been supplied at ±0.75V while load capacitance is 15pF, even if it is possible to drive capacitive loads up to 100pF (in the rail-to-rail version). Figure 8 shows the *SR* behaviour with and without the adaptive biasing for the rail-to-rail solution, showing a *SR* improvement, due to adaptive biasing application, of a factor of about 30. Table I shows the main simulation results, for single-ended ('s' subscribe) and differential ('d' subscribe) outputs. In Table II two significant quality factors (*FOM,* Figures of Merit) for both small (FOM_S) and large (FOM_L) signals, are reported and compared with other topologies presented in the literature, confirming the validity of the proposed solution.

Parameter	nMOS	pMOS	Rail to Rail
Static power dissipation	85 μW	84 μW	166 μW
$(DC\text{-}gain)_s$ $(DC\text{-}gain)_d$	73 dB 79 dB	76 dB 82 dB	75 dB 81 dB
GBW_s GBW_d	2.5 MHz 4.7 MHz	3.5 MHz 6.8 MHz	4.6 MHz 9.2 MHz
Phase-margin	74°	81°	89°
SR_d+/– [V/μs]	17	25	40
CMRR	142 dB	136 dB	132 dB
PSRR+ PSRR–	107 dB 114 dB	114 dB 109 dB	147 dB 150 dB
Settling time (0.25%)	390 ns	410 ns	310 ns

Table I Main simulation results, for single-ended (s) and differential (d) outputs.

V. Conclusions

We have designed an adaptive-biased fully-differential low-voltage low-power OTA topology with DC-gain enhanced characteristic. The proposed circuit can be utilized in applications such as biomedicals and sensor interfaces, where power dissipation is a fundamental requirement for life time battery. Moreover, thanks to high *SR* and low settling time values, this solution is also suitable for applications that require good velocity and precision.

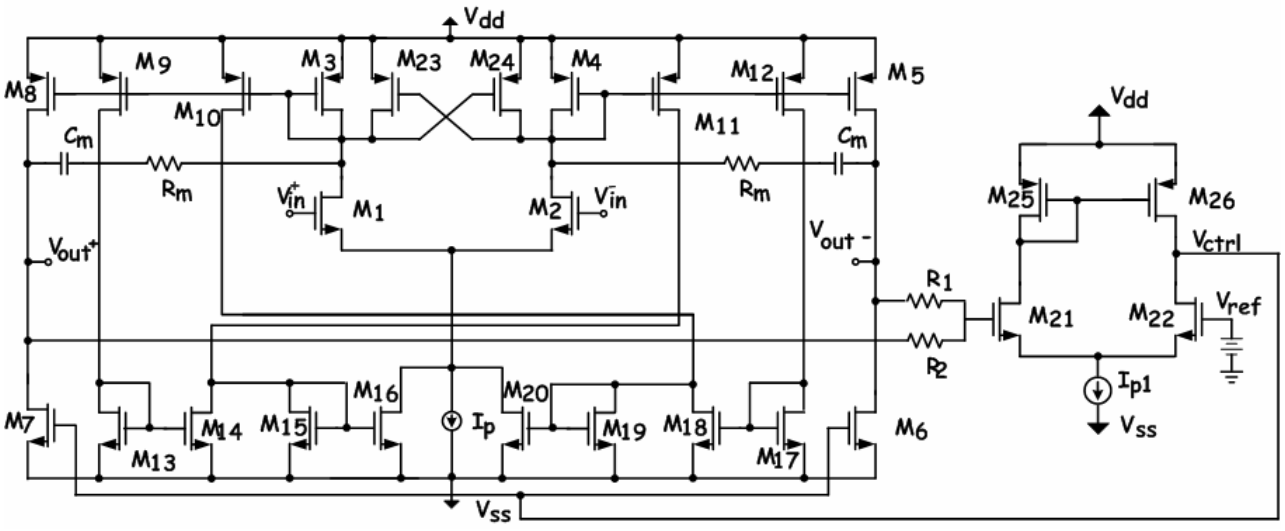

Fig. 7 Fully differential amplifier with adaptive biasing and enhanced DC-gain topology (*nMOS* version)

	FOM_S GBW*Cload/Power [(MHz*pF)/mW]	FOM_L SR*Cload/Power [(V/µs*pF)/mW]
This work nMOS	825	2985
This work pMOS	1217	4474
This work rail to rail	831	3614
[5]	800	2400
[6]	50	135
[11]	271	500
[12]	652	4000
[16]	272	400
[17]	1350	447

Table II FOM parameters comparison.

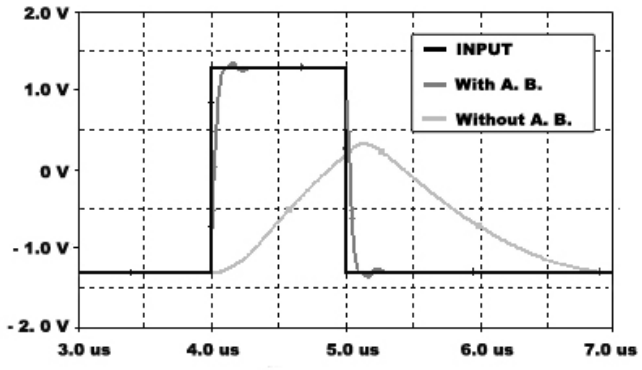

Fig. 8 SR behaviour with and without the adaptive biasing for the rail-to-rail solution

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