Figures 2.8g–l relate to *negative*-edge triggered FSMs. Figure 2.8g highlights the facts that the machine operates at the negative clock edge and that *ena* is just one of its outputs. Again, *ena* must stop the clock when low, replacing it with a zero.

The first solution, shown in figure 2.8h, is the same as that in figure 2.8b. However, as depicted in the timing diagrams of figures 2.8i–j, the output is now fine (glitch-free) when the edge of *ena* reaches the gater *after* the edge of *clk* does, which is what normally occurs, so this solution is generally fine. Recall, however, that *ena* must be glitch-free.

The second solution, shown in figure 2.8k, is fully synchronous, so occasional glitches in *ena* are automatically filtered out. Also, note that in figure 2.8l the output is fine regardless of the delay (positive or negative) between *clk* and *ena* (two DFFs are needed here to guarantee that condition). This solution has the same drawback as that of figure 2.8e; that is, *ena* = '0' must be produced in the *previous* clock cycle (see gray shades in figure 2.8l), thus requiring a greater attention when developing the state transition diagram.

As a final comment, it is important to mention that in many applications the occurrence of metastability is not a problem, either because the metastable state cannot cause a malfunctioning or because the application itself is not critical.

2.4 Pulse Detection

Because many FSMs have asynchronous inputs, the duration of such inputs must be considered in the design. If an input pulse lasts at least one clock period ($T_{pulse} \geq T_{clk}$), its detection by the machine is guaranteed because at least one (positive) clock edge will occur while the pulse is present. On the other hand, if the pulse might last less than that, its detection is no longer guaranteed. Both cases are illustrated in figure 2.9a, where only the first of the two pulses is detected by the circuit. Note the small

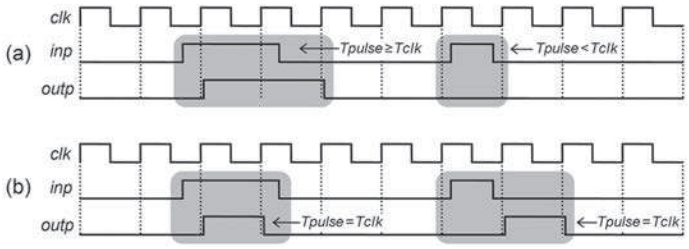

Figure 2.9
(a) Only input pulses with duration $T_{pulse} \geq T_{clk}$ are guaranteed to be detected, and the output duration is proportional to the input duration. (b) Any pulse is detected, and the output duration is always T_{clk}.

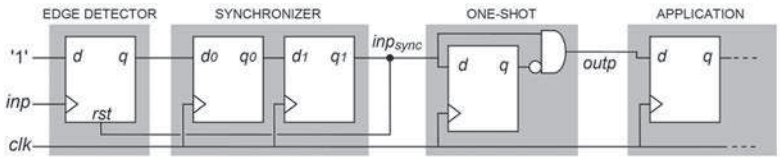

Figure 2.10
Circuit capable of detecting pulses of any width, producing a pulse with fixed length (one clock period) at the output (*outp*).

propagation delays left intentionally between the clock transitions and the corresponding responses in *outp* in order to portray a more realistic situation.

In some cases, the pulse (of any duration) must be detected and converted into a pulse whose duration is one clock period. This is illustrated in figure 2.9b, where both pulses are detected, and each produces an output pulse with duration T_{clk}.

A circuit that shortens the output pulse down to a predefined length (T_{clk} in the present case) is called a *one-shot* circuit, whereas one that detects short pulses is called an *edge detector*. Both are present in the example of figure 2.10, so pulses of any length can be detected and converted into pulses with one-clock-period duration.

The first circuit in figure 2.10 is the edge detector, which consists simply of a DFF plus a reset mechanism. Note that to be able to detect short pulses, *inp* is connected to the clock port instead of the data port. Because the data input is connected to V_{DD} ('1'), the output goes immediately to '1' when a positive edge occurs in *inp*. Some time later (see exercise 2.4), this '1' reaches inp_{sync}, resetting the input DFF, which will remain so until a new positive transition occurs in *inp*.

The second circuit in figure 2.10 is the synchronizer, already seen in the previous section.

The third and final circuit before the application is the one-shot circuit. Because of the AND gate, as soon as inp_{sync} goes to '1', *outp* goes to '1'. However, at the next (positive) clock edge, this value of inp_{sync} crosses the DFF, bringing *outp* back to '0', which it will remain until another pulse occurs at the input and the whole procedure is repeated. This one-shot circuit, however, works well only when the input is synchronous (see exercise 2.3), which is the case here.

Another circuit with the same purposes as that in figure 2.10 is discussed in exercise 2.5. In the chapters ahead, examples employing this kind of circuit are seen.

2.5 Glitches

Glitches are short voltage (or current) pulses produced involuntarily by combinational circuits. It is said that a hazard exists when the possibility of glitches in the circuit exists.