Passive and Parasitic Devices in CMOS

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PASSIVE COMPONENTS AND PARASITIC EFFECTS

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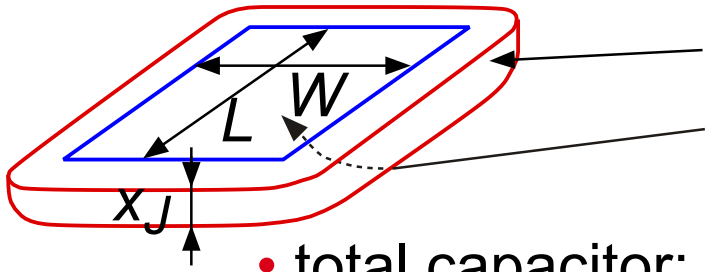
- Capacitors.
- Resistors.
- MOS transistor as a pseudo-resistor.
- Diodes.
- Parasitic channels.
- Latch-up.
- Gate protection.

JUNCTION CAPACITORS

- Seldom used as functional devices, but... always present as parasitic
- Associated with a leakage current (generation in depleted region)
- Voltage dependent.

- Source and drain diffusions: p^+n or n^+p
  - unilateral abrupt junction: $C \sim (V+\Phi_B)^{-1/2}$



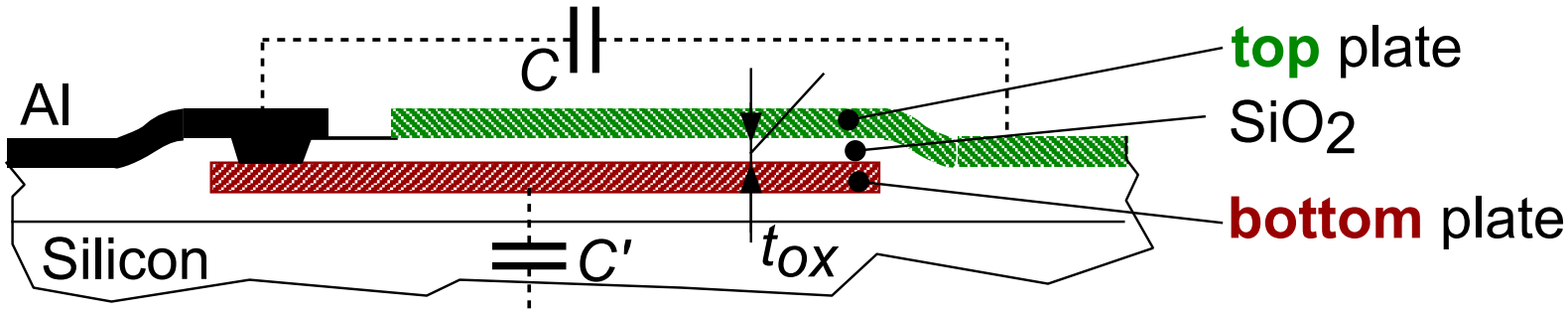
periphery capacitor C_{jp} [fF/µm]

bottom area capacitor; C_{ja} [fF/µm^2]

  - total capacitor: $C = WLC_{ja} + 2(W + L)\,C_{jp}$

- Well-substrate capacitor
  - gradual junction: $C \sim (V+\Phi_B)^{-1/3}$
  - parasitic only for "moving wells":
    - separate floating well e.g.: S-follower, differential pair.
    - CB capacitor of vertical bipolar transistors.

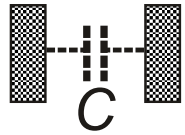
CONDUCTIVE LAYERS - OXIDE CAPACITORS



- always associated with a parasitic capacitor C' with respect to substrate (or any lower plate)
- negligible leakage current
- not or only slightly voltage-dependent
- small temperature dependency

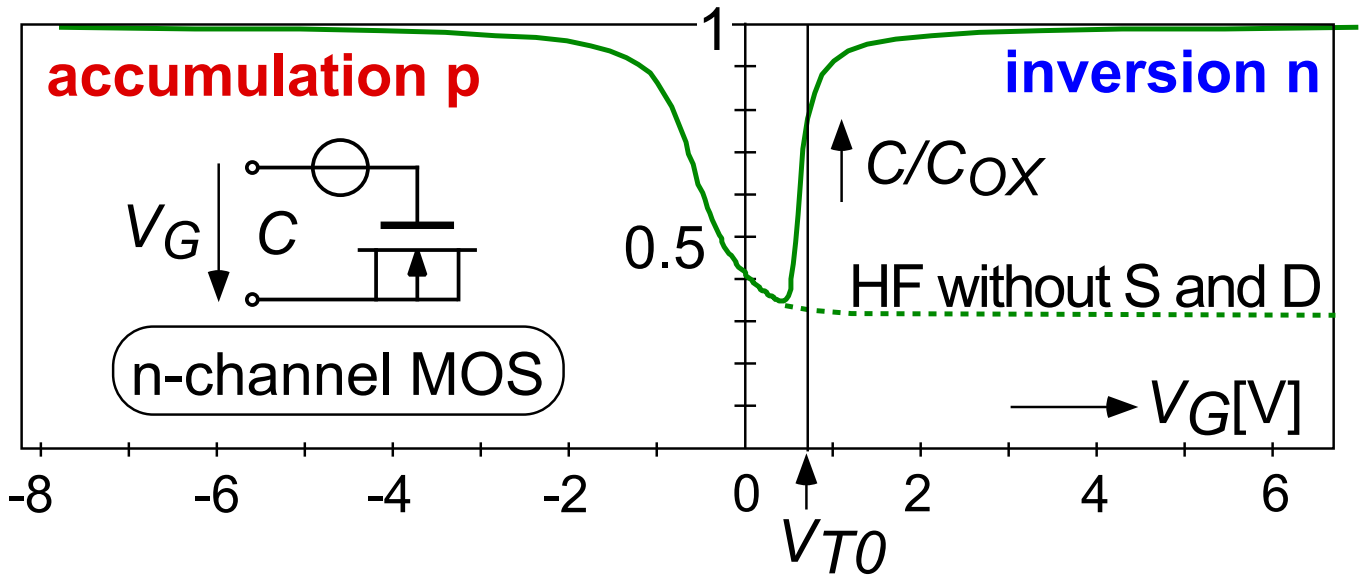
- Metal-Polysilicon capacitor:
  - only possible structure in basic Si-gate
  - good control of ratios (matching)
- Double polysilicon capa.:
  - standard solution for analog processes
  - requires special added poly layer
  - small mismatch ($<10^{-3}$ feasible)
- Metal-metal capacitor:
  - uses one pair of interconnect layers
  - as parasitic capacitor: dominated by lateral fields in submicron processes.

schematic cross-section:



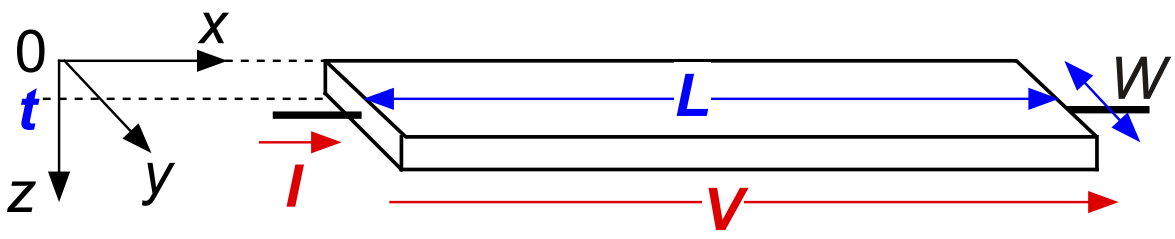
GATE-OXIDE CAPACITOR

- Transistor structure used for its gate capacitance



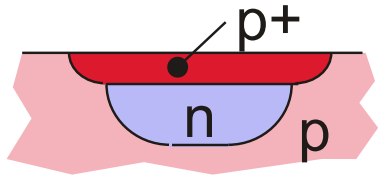
- large value of specific capacitor (0.3 to 10nF/mm^2)
- available in any CMOS process
- at least one D or S **diff. needed** to permit fast modulation of inversion layer
- the dip in the $C(V_G)$ curve must be avoided by:
  - gate bias for **inversion** or
  - gate bias for **accumulation**: use p-channel in n-well connected to *V-*
  - using additional p+ or n+ diffusion under the gate (additional step in process)
- always somewhat voltage dependent (except with p+ or n+ diffusion)

RESISTORS



- Drift current of maj. carriers, local conductivity $\sigma(z) = q\mu_n n_n$ or $q\mu_p p_p$
- If $L \gg W, t$, then: $I = W\int_0^t J_X\,dz = W\int_0^t \sigma(z)E_X\,dz = W\frac{V}{L}\int_0^t \sigma(z)\,dz$
- thus: $V/I = R = \frac{L}{W}R_S$ with $1/R_S = \int_0^t \sigma(z)dz$
- layers characterized by their sheet resistivity R_S
- associated with a distributed parasitic capacitor

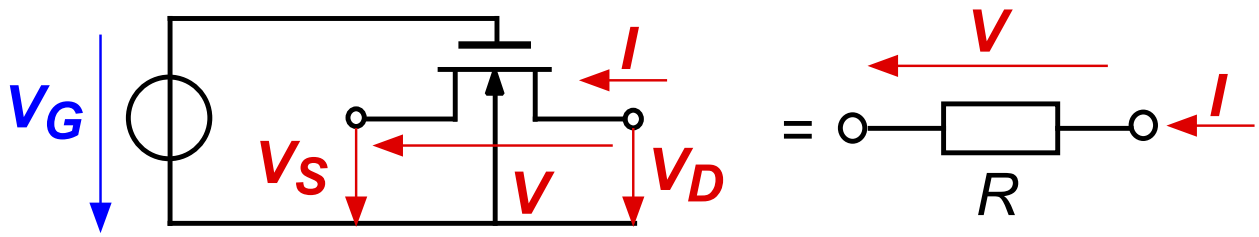
- Diffused layers: isolated by a pn-junction: leakage and parasitic capa.
  - non salicided n+ or p+ (S and D) layer: R_S=10 to 100 Ω
  - well layer: slightly nonlinear and bias-voltage dep.: R_S=0.5 to 5 KΩ
  - buried well: larger R_S but larger V-dependency and parasitic capa.



buried n-well

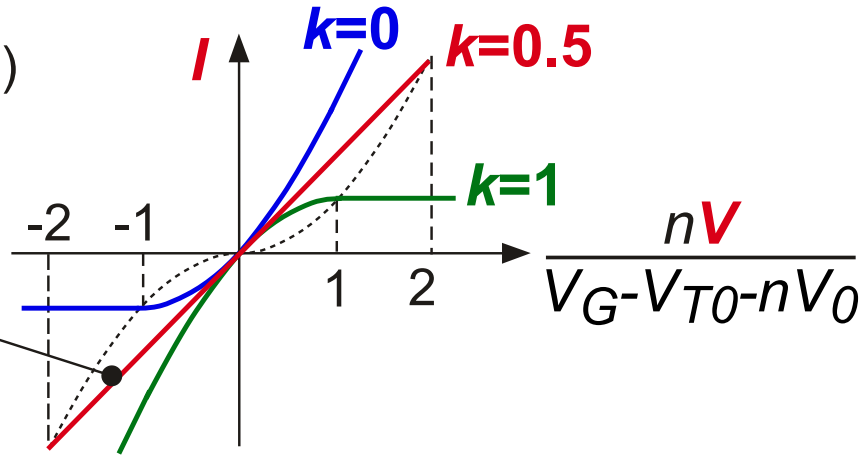
- Layers on oxide: perfect galvanic isolation
  - polysilicon (non salicided): R_S=10 to 100 Ω
  - lightly doped polysilicon: R_S > 100 K Ω
  - metal or salicided silicon: very low R_S.

TRANSISTOR USED AS A RESISTOR



In linear mode: $I = \beta(V_D - V_S)[V_G - V_{T0} - \frac{n}{2}(V_D+V_S)]$

- Define: $V = V_D - V_S$ with $V_D = V_0 + kV$ and $V_S = V_0 - (1-k)V$
- Then: $I = \beta V [V_G - V_{T0} - nV_0 + n(0.5 - k)V]$ **nonlinear term**
- Best case: k=0.5 (V_S and V_D symmetrical / V_0)
  - linear $I(V)$ for $|V|<2(V_G - V_{T0} - nV_0)/n$
  - slope $1/R = \beta(V_G - V_{T0} - nV_0)$



- Temperature variations of β and V_{T0} have opposite effects on R.
  - compensation may be calculated to occur (see TR-32) for:

$$V_G - V_{T0} - nV_0 = \frac{n-0.5}{\alpha}(V_{G0}-2\phi_F)$$ **= 0.2 to 0.4V**

MOS TRANSISTOR OPERATED AS A PSEUDO-RESISTOR

[1, 2, 3, 7, 8]

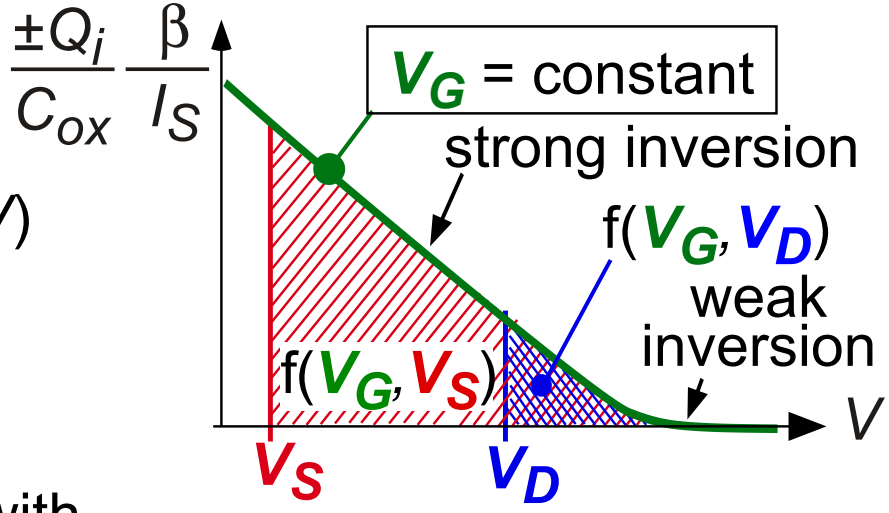
- From the transistor model : $I_{SD} = \pm(I_F - I_R) = \pm I_S\,[\,f(V_G, V_S) - f(V_G, V_D)]$

  + is for **p**-channel, **-** for **n**-channel

- Assumption: V_G=constant

- Definition: **Pseudo-voltage** $V^* = \pm V_0\, f(V_G, V)$

  where V_0 is an arbitrary positive scaling voltage



then, $I_{SD}(V_S, V_D)$ may be expressed as a

- Pseudo Ohm's law $\boxed{I_{SD} = G^*\,(V_S^* - V_D^*)}$ with...

  - **Pseudo-conductance** $G^* = 1/R^* = I_S/V_0 \propto W/L$; thus...

- Any network of MOS transistors connected by S and D with **same V_G**

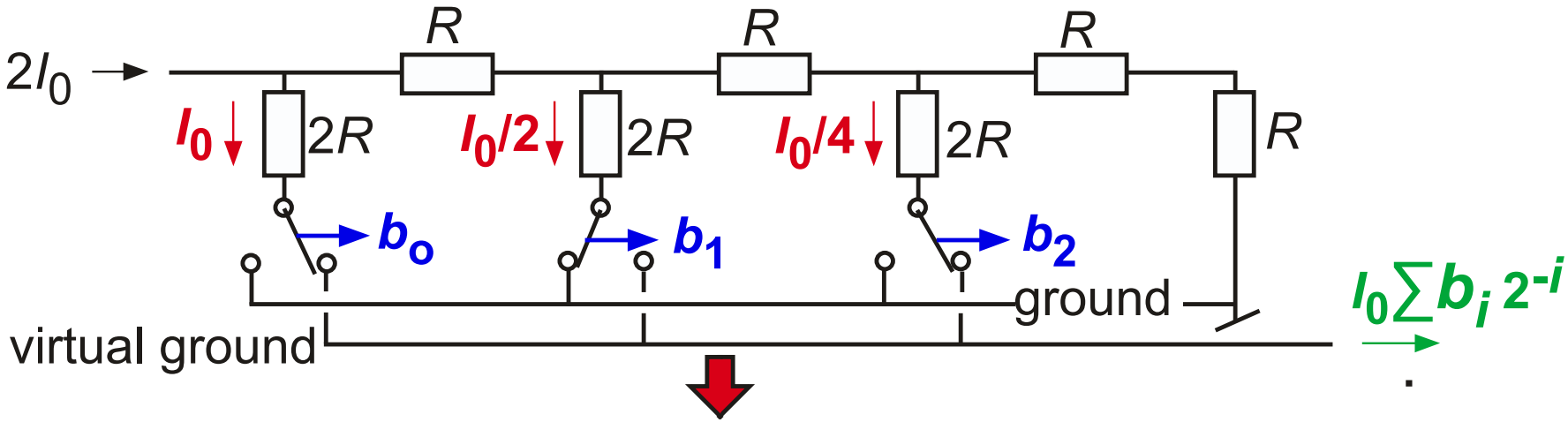
  is **linear for currents** and can replace its resistive prototype

- **Pseudo-ground** (0-ref. for V^*) for $f(V_G, V)$ negligible
  (this side of the transistor **saturated**)

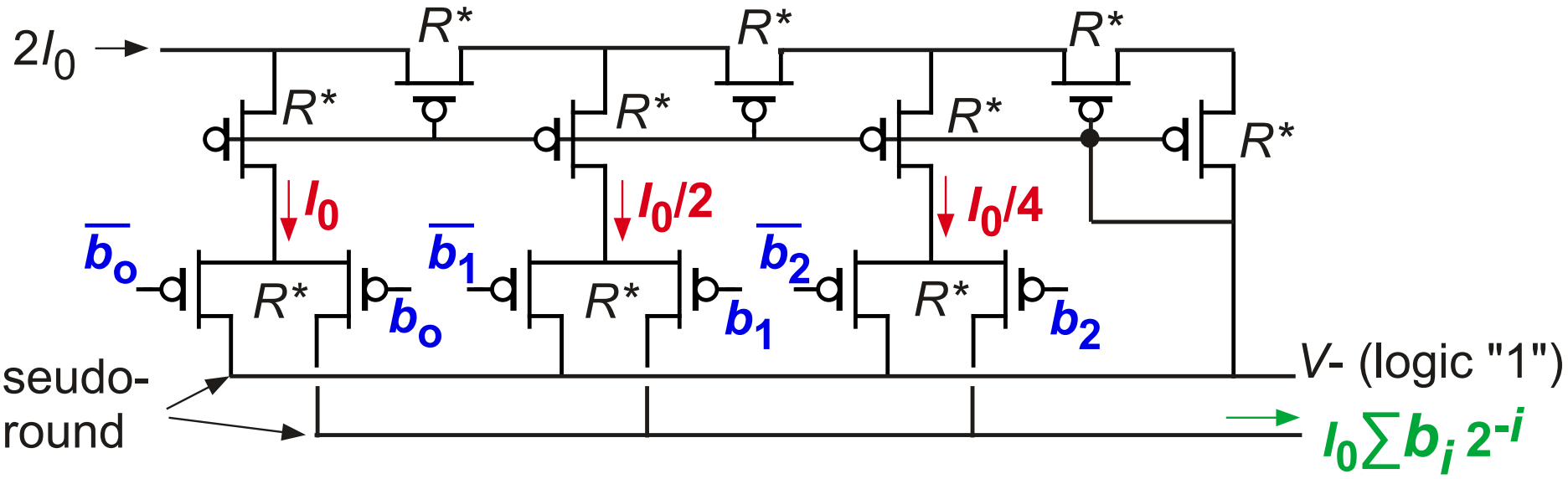
- Precision is degraded by short-channel effects.

EXAMPLE OF APPLICATION: *R*-2*R* D/A CONVERTER

- Standard resistive circuit (example for 3 bit): [4,5]



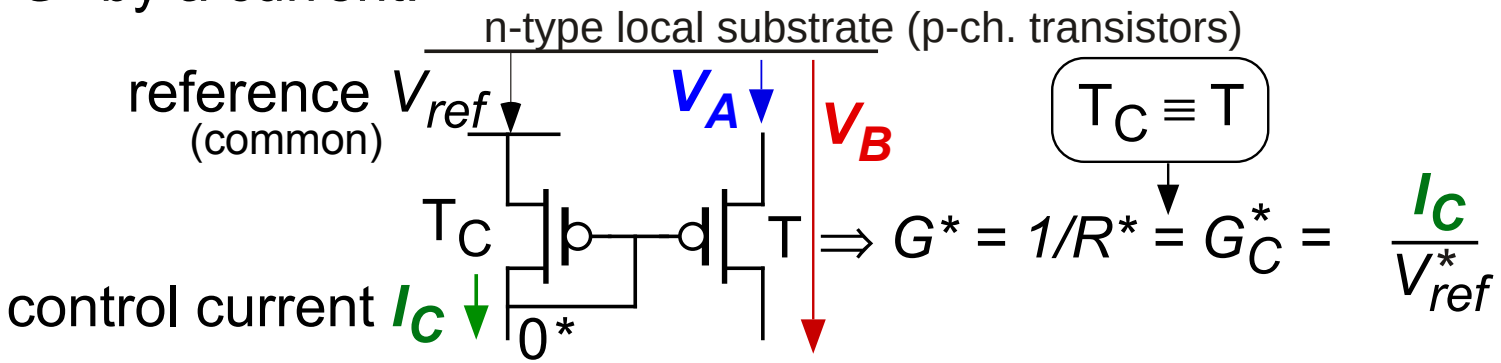
- Pseudo-resistive implementation (by p-channel transistors):



- For best precision:
  - strong inversion
  - non-saturated devices (avoid pseudo-ground)

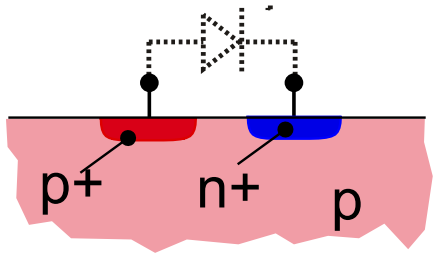
PSEUDO-RESISTORS IN WEAK INVERSION [2, 3, 7, 8]

- If $f(V_G, V) \ll 1$ at both ends of channel → weak inversion
- Then: $f(V_G, V) = \exp\frac{V_G - V_{T0}}{nU_T} \exp\frac{-V}{U_T}$ **separable** in V_G and V
- New definitions:
  - pseudo-voltage $V^* = \pm V_0 \exp\frac{-V}{U_T}$ **independent** of V_G
  - pseudo-conductance $G^* = \frac{I_S}{V_0}\exp\frac{V_G - V_{T0}}{nU_T}$ **controllable** by V_G
- G^* controllable by V_G separately for each pseudo-resistor
- Range of current: 10^3 to 10^6 for...range of voltage: 7 to $14U_T$ only.
- Control of G^* by a current:

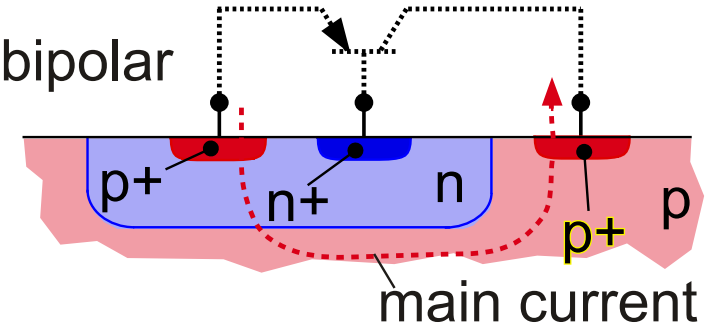


DIODES AVAILABLE IN CMOS

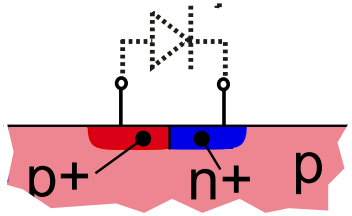
- Junction source (or drain)/common substrate
  - one grounded terminal
  - maximum reverse 2 to 20 volts



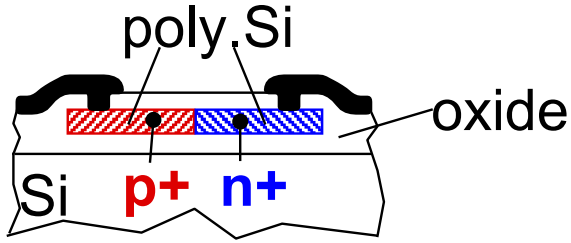
- Junction source (or drain)/local well
  - only exists as the **BE junction** of a vertical bipolar
    - collector current (p+ to p) dominates
    - one grounded terminal (p-substrate)
    - thus: **not** a **floating** p+n diode



- Lateral p+n+ junction (when allowed)
  - very low breakdown voltage
  - one grounded terminal



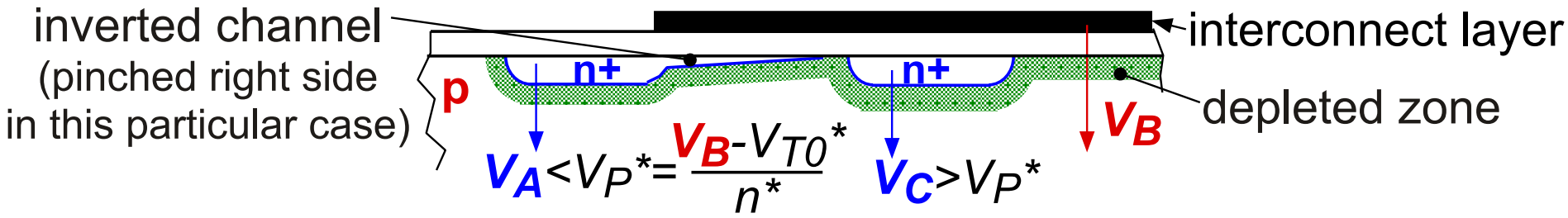
- Lateral junction in polysilicon [6]
  - non ideal *I*(*V*) characteristics
  - floating diode
  - **excellent isolation** from substrate (oxide)
  - only available in some processes (bi-doped poly)



- Well-substrate diode: largest breakdown voltage

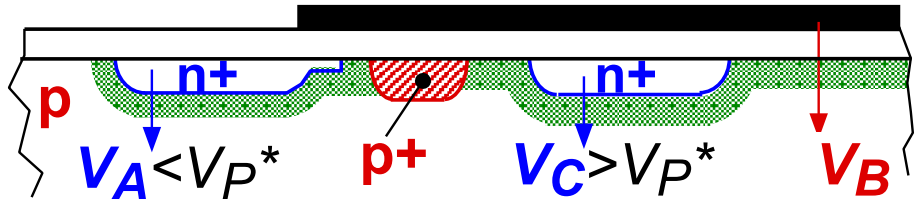
PARASITIC CHANNELS

- When the potential of some interconnection becomes too high, it may induce inverted channels underneath the thick (field) oxide:

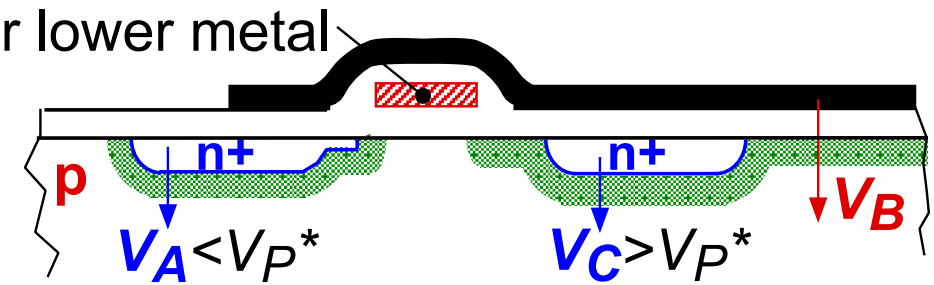


  - For V_A=0, inversion occurs for $V_B > V_{T0}^*$
  - Threshold V_{T0}^* of thick-oxide (field) MOS structures limits $V_{B\max}$
  - This limit may be overcome in two ways:

- Channel stopper: **p+** diffusion in p (or **n+** in n) to prevent inversion:

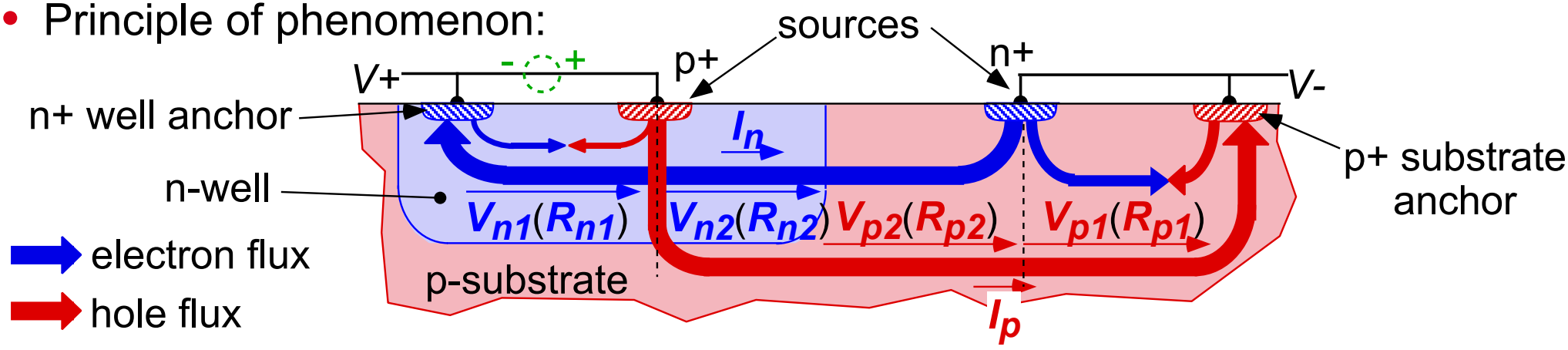


- Shielding: by lower layer connected to local substrate:



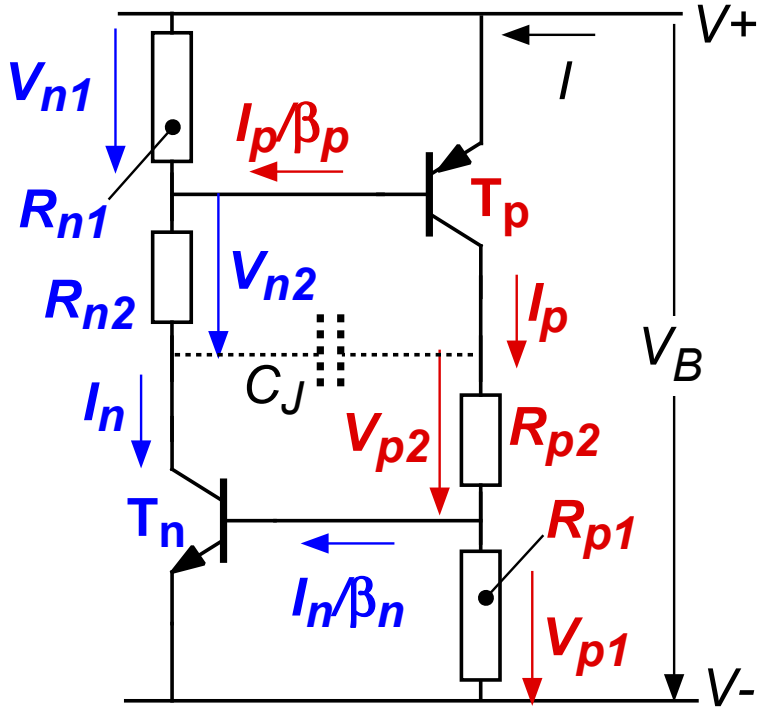
LATCH-UP

- Principle of phenomenon:



  - 4-layer structure which can latch-up to a large current if the p+n and n+p junctions are forward biased

- Equivalent circuit:



LATCH-UP: MINIMUM ("HOLD") CURRENT AND VOLTAGE

- Minimum current I: value of I corresponding to open-loop gain =1
  - Hypothesis: $V_{n1}=V_{p1}=V_J$ ("junction voltage")
  - Yields:

$$I_n > \frac{V_J}{\beta_p\beta_n-1}\left(\frac{1}{R_{p1}}+\frac{\beta_p}{R_{n1}}\right)\beta_n \quad \text{and} \quad I_p > \frac{V_J}{\beta_p\beta_n-1}\left(\frac{1}{R_{n1}}+\frac{\beta_n}{R_{p1}}\right)\beta_p$$

Thus:

$$I = I_n+I_p > \frac{V_J}{\beta_p\beta_n-1}\left[\frac{\beta_p}{R_{n1}}(\beta_n+1)+\frac{\beta_n}{R_{p1}}(\beta_p+1)\right]$$

  - Now if: $\beta_p \gg 1$, $\beta_n \ll 1$ but $\beta_p\beta_n \gg 1$ with R_{p1}, R_{n1} same order of magnitude:
  - then:

$$I_n > \frac{V_J}{R_{n1}} \quad \text{and} \quad I_p > V_J\left(\frac{1}{\beta_n R_{n1}}+\frac{1}{R_{p1}}\right)$$

- Minimum voltage V_B is increased by R_{n2} and R_{p2}:

$$V_B > \text{the larger of } R_{n2}I_{nlim}+V_J \text{ and } R_{p2}I_{plim}+V_J$$

LATCH UP: TRIGGER MECHANISMS

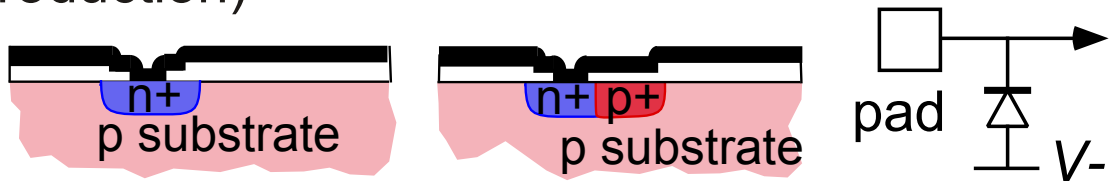
- Current across reverse-biased pn junction by
  - breakdown (breakdown voltage may be reduced at surface)
  - transient : $C_J\, dV/dt.$
- Lateral current in substrate:
  - from input protections
  - collector current of bipolar to substrate.

LATCH-UP PREVENTION

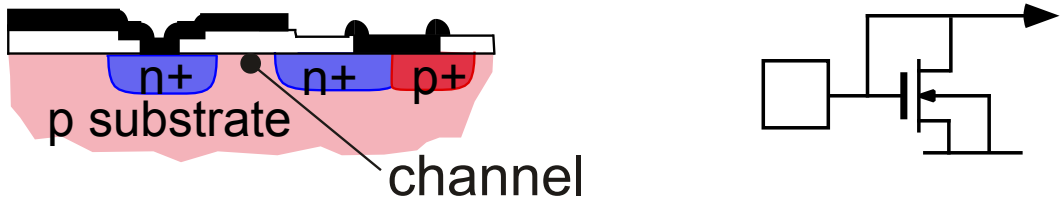
- Increase hold current I_{min}:
  - reduce R_{p1} and/or R_{n1}: - minimize distance p+n+
    - anchor diffusion all around well
    - recover I_p under well (epi. p on p+ subst.).
  - reduce of β_n: - increase distance n+ source to n-well.
- Increase V_{Bmin}: follows increase of I_{min} thus, increase R_{p2} and/or R_{n2}
- Suppress the latched-up state:
  - $\beta_p\beta_n < 1$ by increase of I_{min}.
  - limit current below I_{min}
  - limit voltage below V_{Bmin}.

GATE PROTECTIONS

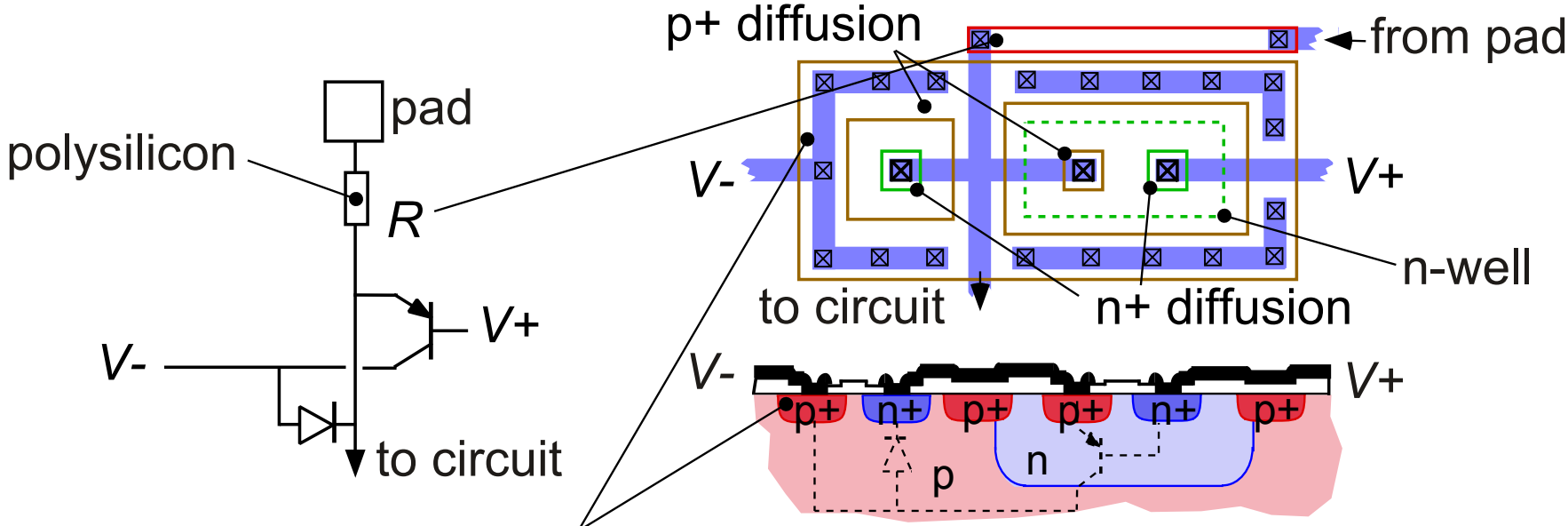
- **Mandatory** for each input (output) pad to avoid gate destruction
  (max field in SiO_2 : ~ 7.10^8V/m)
- Simple protections (not valid for production)
  - diffusion-substrate diode:
    (conduction/breakdown)



  - thick-oxide transistor
    (conduction junction/channel)



- Full industrial protection:(example):



  - p+ ring connected to V- to collect substrate current

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